Homework #3 (due May 25, 2017 in class)

1. Given a net \( n \) with the four pins \( p_1 = (20, 2) \), \( p_2 = (8, 18) \), \( p_3 = (3, 10) \), and \( p_4 = (12, 4) \), let the estimated wire lengths by using the HPWL approximation, the minimum cost spanning-tree one, the minimum cost Steiner tree, Squared Euclidean distance (with \( \gamma_{ij} = 1 \)), the log-sum-exp model (use the expression with \( \ln \) and let \( \gamma = 10 \)), and the weighted-average (WA) wirelength model (with \( \gamma = 10 \)) be \( m, n, p, q, r, \) and \( s \), respectively. Find \( m, n, p, q, r, \) and \( s \).

2. You are asked to place a cell \( i \) on a chip. The cell \( i \) connects to four other pads \( a, b, c, \) and \( d \) at the coordinates \( (2, 18), (18, 1), (3, 16), \) and \( (15, 8) \) with the weights 1, 3, 5, and 7, respectively. Find an appropriate position to place the cell \( i \) by using the force-directed method.

3. Consider the placement of the modules shown below.
   (a) Give the MP-tree for the module placement.
   (b) Discuss how you can utilize only two contours (could be a horizontal or a vertical contour) to pack the modules into the four corners. Show your packing step by step. What is the time complexity of your packing scheme?

4. Exercise 11.13 of the W&C&C book (pages 681–682). This question analyzes the error of the log-sum-exponential function defined in class as an approximation of the maximum function. The error function is defined as:
   \[
   err_\gamma(z_1, \ldots, z_n) = LSE_\gamma(z_1, \ldots, z_n) - \max(z_1, \ldots, z_n),
   \]
   where
   \[
   LSE_\gamma(z_1, \ldots, z_n) = \gamma \times \ln \sum_{i=1}^n e^{z_i/\gamma}
   \]
   and \( \max(z_1, \ldots, z_n) \) gives the maximum value over \( z_1, \ldots, z_n \). Derive an upper bound and a lower bound of \( err_\gamma(z_1, \ldots, z_n) \) over all possible values of \( z_1, \ldots, z_n \) as functions of \( n \) and \( \gamma \).
5. Consider the example shown below. Assume all nets have a weight of 1. For the three fixed modules, module 4 is at (15, 5), module 5 is at (0, 30), and module 6 is at (40, 20). Determine the locations of the movable modules such that the total weighted quadratic wirelength is minimized.

![Diagram](image)

6. Give an instance of large-scale hierarchical mix-sized cells and macros as shown below, in which there are multiple mixed-size domains (e.g., four in the figure below) whose rectangular outlines are fixed, the size difference between the smaller cells and the larger macros in each domain can be more than 1,000 times, some macros are preplaced at fixed locations, and some pins of the cells and macros are connected to I/O pads along the chip boundary and also to the cells and macros in other domains.

(a) Sketch an approach to place the instance in a chip with a fixed outline.
(b) Discuss the strengths and weaknesses of your approach in handling this instance in terms of (1) placement quality for sparse and dense designs and (2) legality (how easy it is to legalize a design).

7. HPWL wirelength model for high-degree nets.

(a) Given a net n₁ with the four pins \( p₁ = (0, 0), p₂ = (12, 0), p₃ = (12, 6), \) and \( p₄ = (24, 0) \), let the estimated wire lengths by using the HPWL approximation and the minimum cost Steiner tree be \( a \) and \( b \). Find the error rate, i.e., \( \frac{|a-b|}{b} \times 100\% \).
(b) Given a net \( n₂ \) with the five pins \( p₁ = (0, 0), p₂ = (12, 0), p₃ = (12, 6), p₄ = (24, 0), \) and \( p₅ = (6, 6) \), find the error rate for the HPWL approximation with respect to the minimum cost Steiner tree.
(c) How about the error rate for \( n₃ \) with the six pins \( p₁ = (0, 0), p₂ = (12, 0), p₃ = (12, 6), p₄ = (24, 0), p₅ = (6, 6) \) and \( p₆ = (18, 6) \)?
(d) What is your observation for the error rate of the HPWL wirelength approximation with respect to the minimum cost Steiner tree for high-degree nets? Can you provide a better approximation method to consider the cases with high-degree nets?
8. You are asked to work on an emerging mixed-cell-height legalization problem, arising from modern design needs with larger drive strength and pin access spaces. Given a chip with a global placement of \( n \) standard cells \( C = \{ c_1, \ldots, c_n \} \), where each cell \( c_i \) has the width \( w_i \), the height \( h_i \) (could be single-row height or double-row height), and the coordinate (bottom-left corner) \( (x'_i, y'_i) \), \( \forall i, 1 \leq i \leq n \), and each double-row-height cell has a boundary power-rail type Vdd or Vss, the mixed-cell-height legalization problem places each cell \( c_i \) to the coordinate \( (x_i, y_i) \) and align its cell boundaries to corresponding power rails such that no two cells overlap with each other, and the total cell displacement is minimized.

The objective function is given by

\[
\min \sum_{i=1}^{n} (|x_i - x'_i| + |y_i - y'_i|),
\]

while the constraints are described in more detail as follows:

1. Cells must be non-overlapping and inside the chip region.
2. Cells must be aligned in the rows.
3. Cell boundaries must match the Vdd/Vss power rails: The Vdd/Vss power rails are routed horizontally between the rows, each standard cell has power rails running through its two cell boundaries and also row intersection(s) for a double-row-height cell; see the figure below for an illustration. Specifically, single-row-height standard cells must be placed to match the correct Vdd/Vss power rail, possibly by vertical cell flipping. For a double-row-height cell, however, its two boundaries are designed for either Vdd or Vss. Accordingly, we must match the correct power rail for a double-row-height cell. See the figure below for an example.

Sketch a legalization approach to the problem with single-row-height and double-row-height standard cells. Please also address how you consider the cost due to white spaces.

![Image of mixed-cell-height legalization](image_url)


(a) For the Soukup maze router, there is no guarantee that we can find the shortest path if such a path exists. Give an example routing configuration for the situation.

(b) For the Hightower line-search router, there is no guarantee that we can find a path if such a path exists. Give an example routing configuration for the situation.

10. Extend maze routing algorithm such that it generates a shortest path from source to target with the minimum number of bends.

11. Find the path from S to T by the A*-search routing for the instance shown below by defining \( g(p) \) to be the label from the source S to the current node of \( p \) and \( h(p) \) to be the Manhattan distance between
p and the target T, where the cost function is given by \( f(p) = g(p) + h(p) \). Break the tie by picking the grid cell on the right of the current position. \((\text{Please show you work and labels step by step.})\)

12. (DIY Problem) For this problem, you are asked to design a problem set related to the course content covered so far and give a sample solution to your problem set. Grading on this problem will be based upon the quality of the designed problem as well as the correctness of your sample solution.