Status Quo and future of IC technologies

IC/semiconductors(Logic/Memory/Analog/Micro +OSD)

3D x3D x3D

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http://nanosioe.ee.ntu.edu.tw

High mobility/high K/FinFET

PPACR (performance/power/area/ cost/reliability)

Google Scholar Page

Citation :8305/ H index:41

i10 index:201

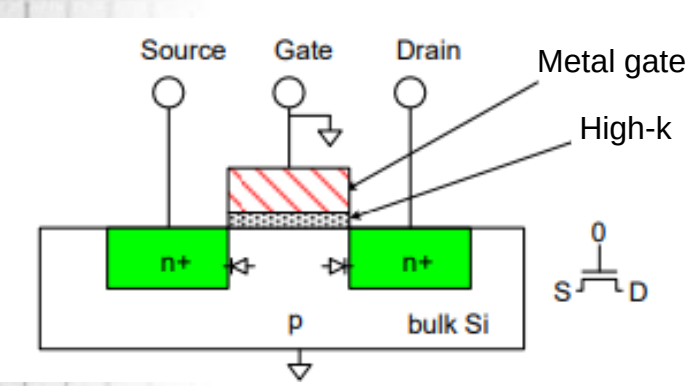
IC Process For Beginners: From Sands to Chips (點砂成晶)

- https://www.youtube.com/watch?v=ytBJHksswkU&ab_channel=%E5%8F%B0%E7%A9%8D%E5%89%B5%E6%96%B0%E9%A4%A8TSMCMuseumofInnovation
- https://www.youtube.com/watch?v=Bu52CE55BN0&ab_channel=SamsungSemiconductorNewsroom
- https://www.youtube.com/watch?v=_VMYPLXnd7E&ab_channel=Intel

Prof. Chee Wee Liu, He-Wen Shen, Yu-Chieh Lee

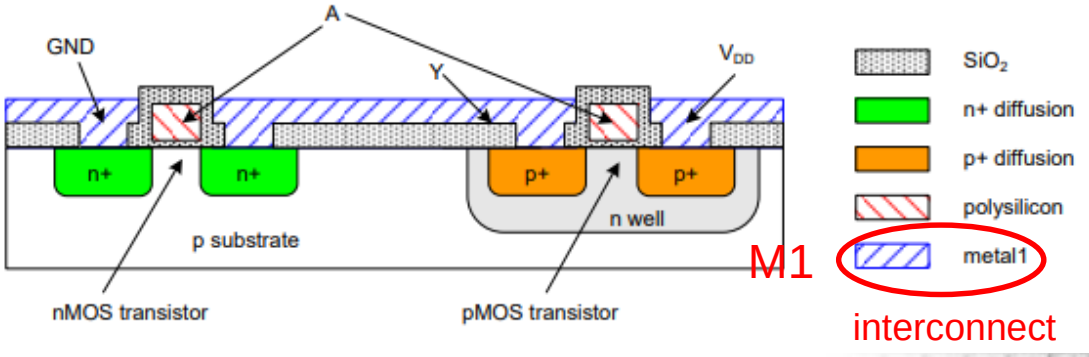
IC = Front-end + Back-end

Front-end



- A transistor (NMOS)

Back-end

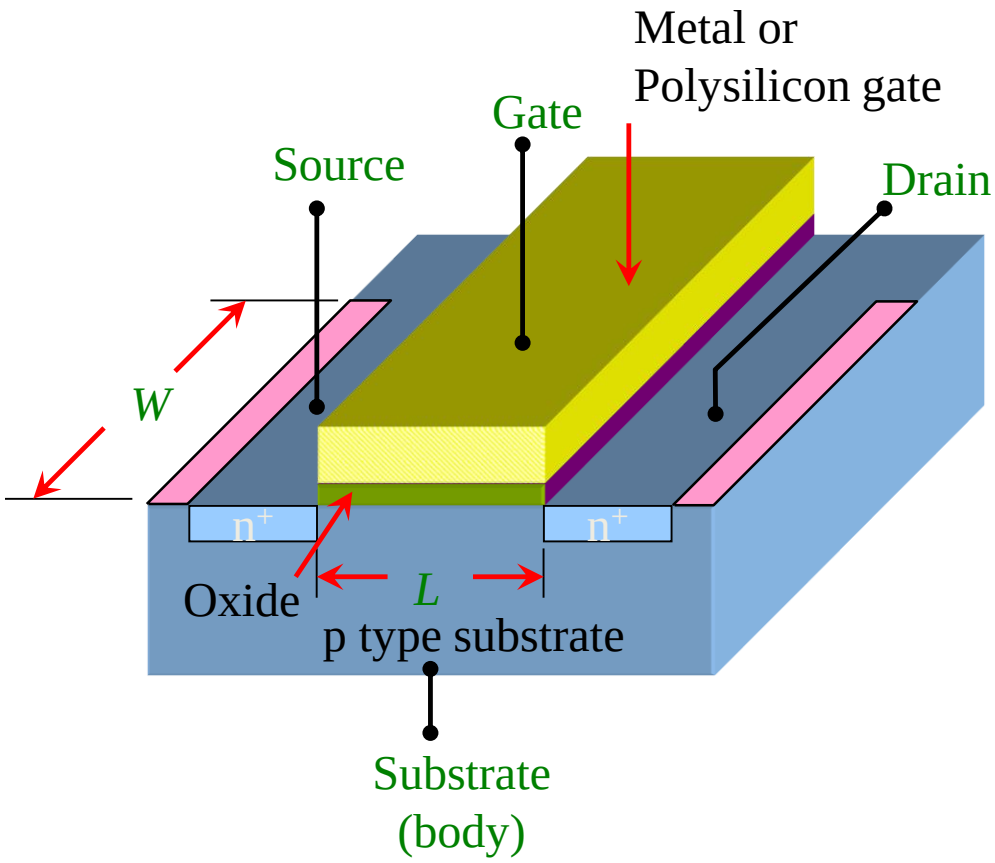


Ref. : CMOS VLSI Design 4th Ed.

- An inverter

Planar MOSFET structure upto 20/22nm

Smallest dimension?



Historically, L is the technology node up 250 nm/350 nm

Moore's Law

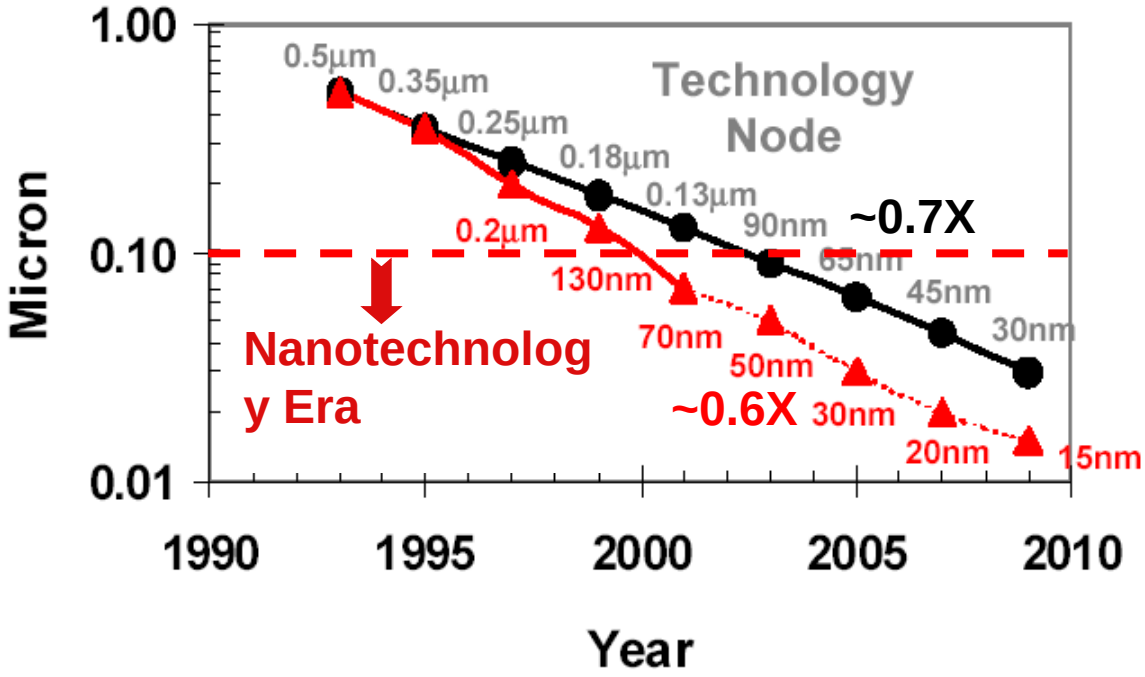
Density 2x/generation(18 month/2 yrs/depends)

from n node to n+1 node

- Device/SRAM footprint (next generation) =Linear dimension (current generation) x 0.7

- 5nm has ~2x density of 7 nm
- Node name is density marker

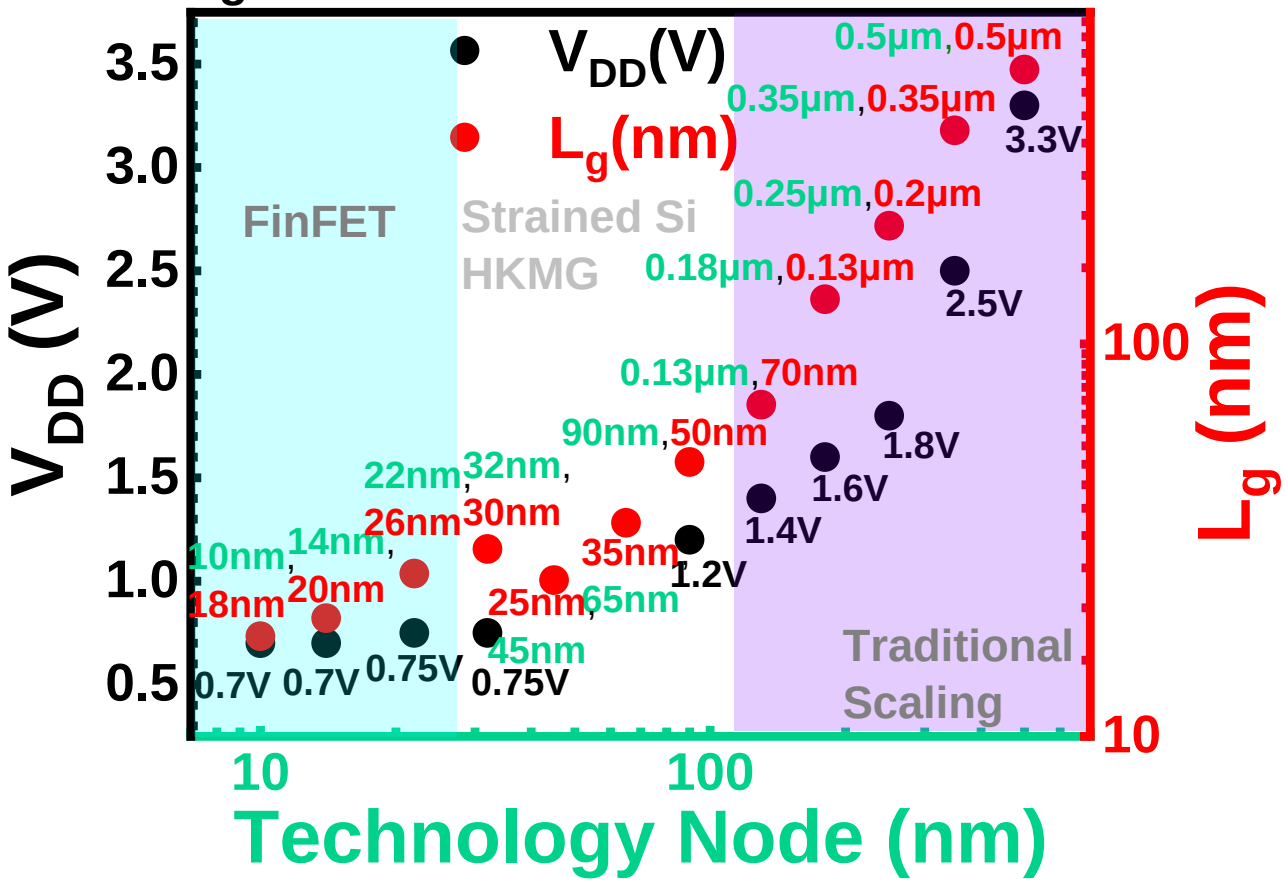
Node name is NOT gate length
Evolution in Channel Length



Nanotechnology is in production today

(~20 yr ago)

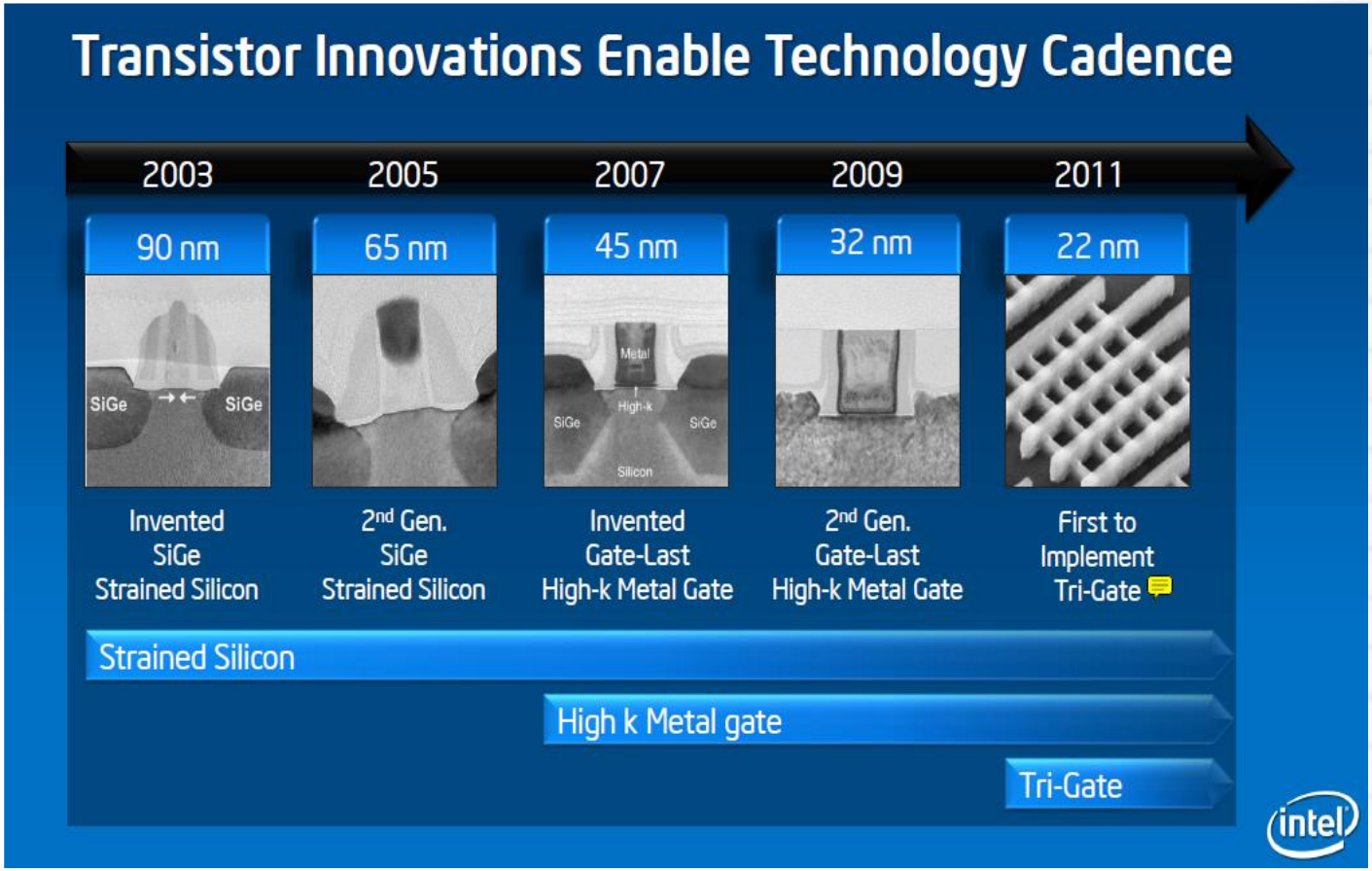
V_{DD} and L_g Scaling Trend vs Technology Node



- V_{DD} not available for 65nm and 45nm node

Intel technology node

Strained Si starting from 90 nm node



- Enabling technologies: high mobility, high-k/metal gate, 3D transistor

I_{ON} Improvement by technologies

$$I_d = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs}-V_t)^a \times \text{stacking number (floor numbe}$$

→ Nanosheet (2nm)

FinFET (16nm) : $2H_{FIN}+W_{FIN}$

Intel : 22nm

High mobility $\frac{\varepsilon_{ox}}{t_{ox}} \rightarrow HK(45nm\ node)$

$$\frac{\varepsilon_{ox}}{t_{ox}} = \frac{\varepsilon_{HK}}{t_{HK}} = \frac{\varepsilon_{ox}}{EOT} \qquad \varepsilon = k\varepsilon_0$$

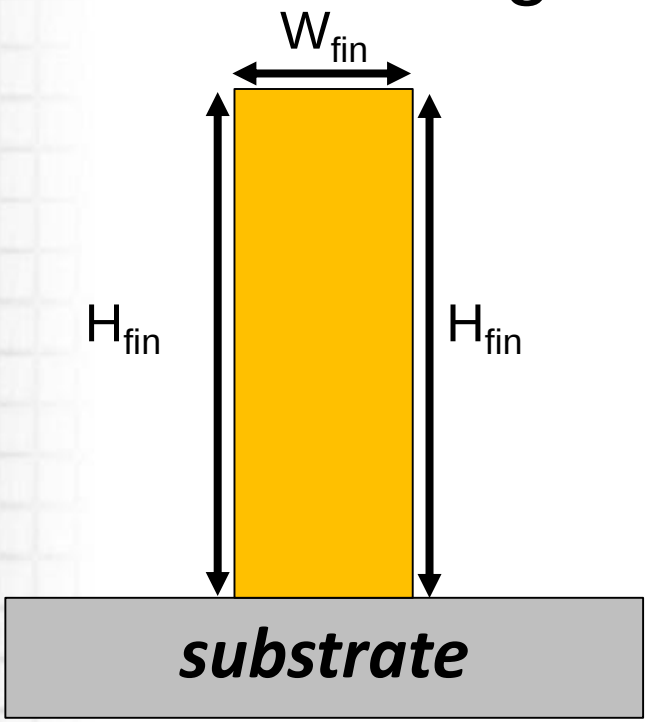
t_{ox} >1nm. Otherwise, I_g is significant

1. Strained Si (90nm)
2. High mobility channel (5nm SiGe p-channel)

Make your FinFET/GAA/Nanosheet

I_{ON} Improvement -- W_{eff}

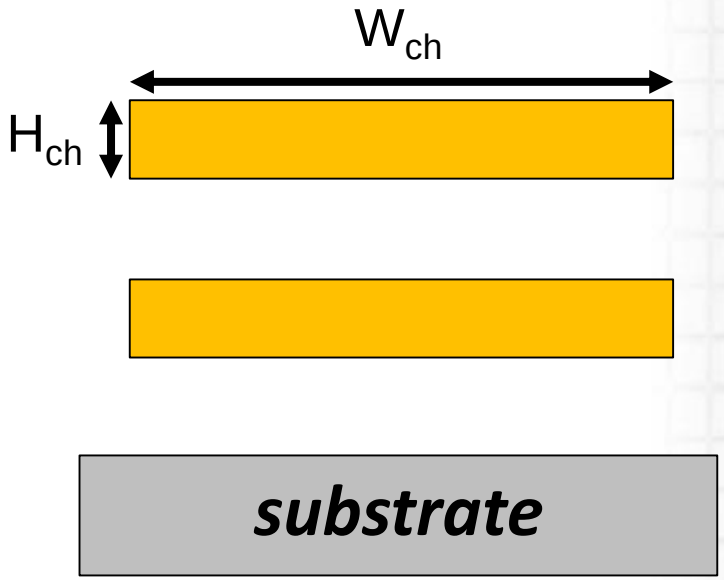
FinFET = Tri-gate



$W_{eff} = 2H_{fin} + W_{fin}$

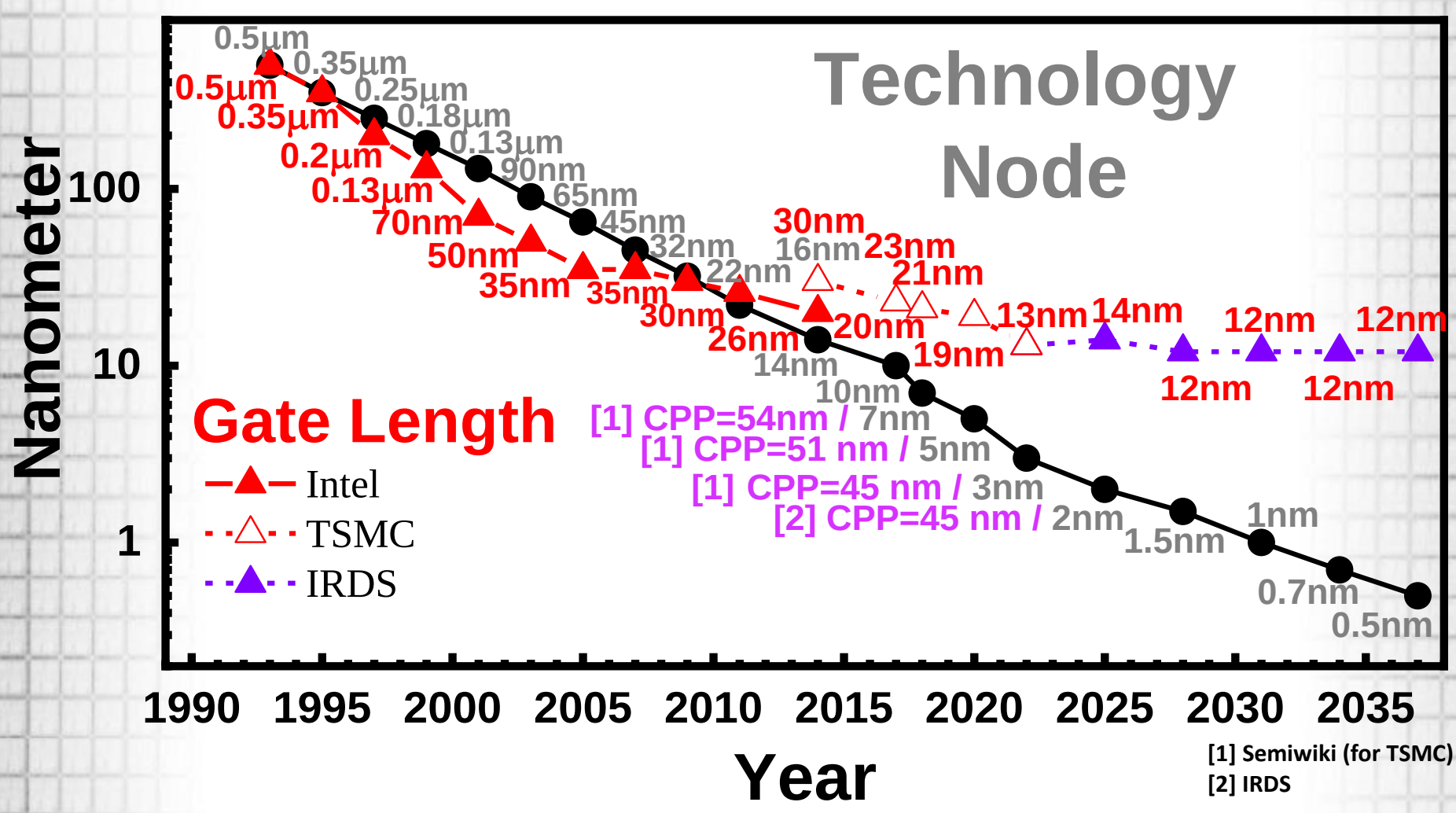
Footprint = W_{fin} x L

Nanosheet/nanoribbon/
Multi bridge channel = GAA



$W_{eff} = (2H_{ch} + 2W_{ch})$ x floor number

L_g scaling with different nodes

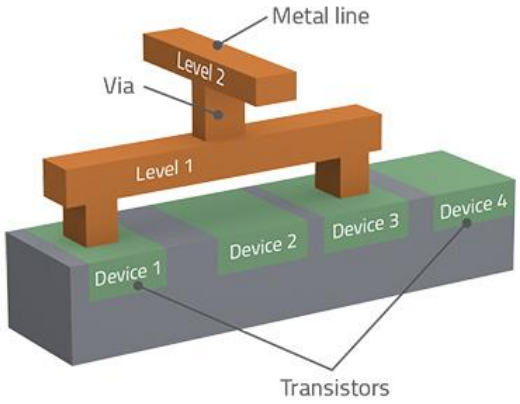


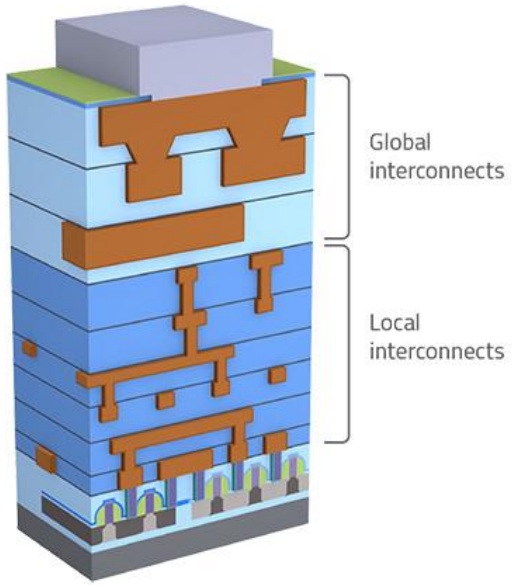
[1] Semiwiki (for TSMC)
[2] IRDS

- L_g can be larger than node name due to narrow width in footprint

Back End :Interconnect

- Create a path for electricity to pass through by depositing a thin metal film using materials such as aluminum, copper, titanium, or tungsten





Ref. : https://www.google.com/url?sa=i&url=https%3A%2F%2Fsemiengineering.com%2Fall-about-interconnects

Heterogeneous(Homogeneous) Integration

- Heterogeneous (Homogeneous) integration/3DIC/Advanced package

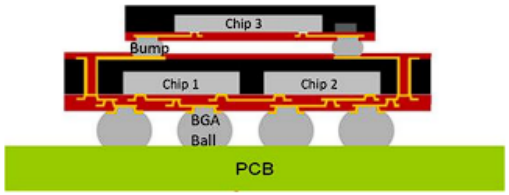
= IC + IC + IC …

+: hybrid bond / TSV / bump /interposer…

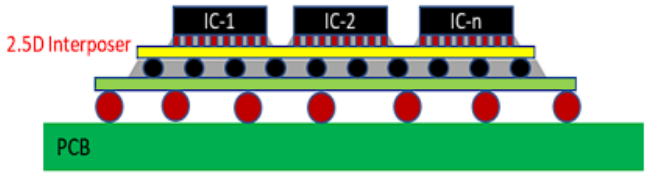
Heterogeneous Integration Platforms

Heterogeneous Integration Platforms

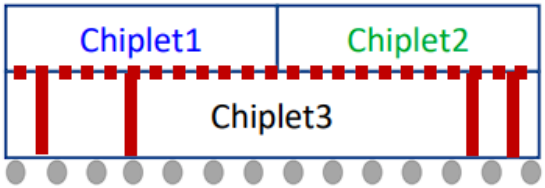
Embedded High Density Fan-Out WLP

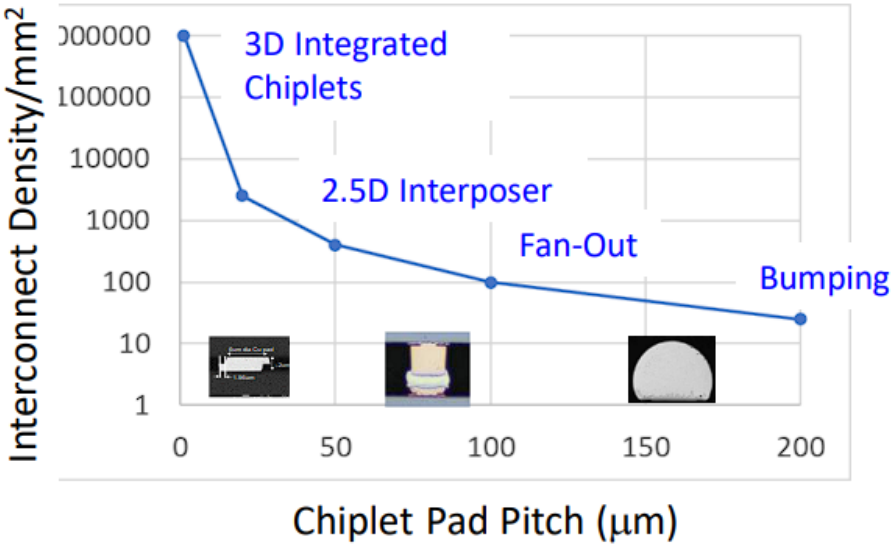


2.5D Interposer



3D-Integrated Chiplets





Inter-chiplet wiring density increases

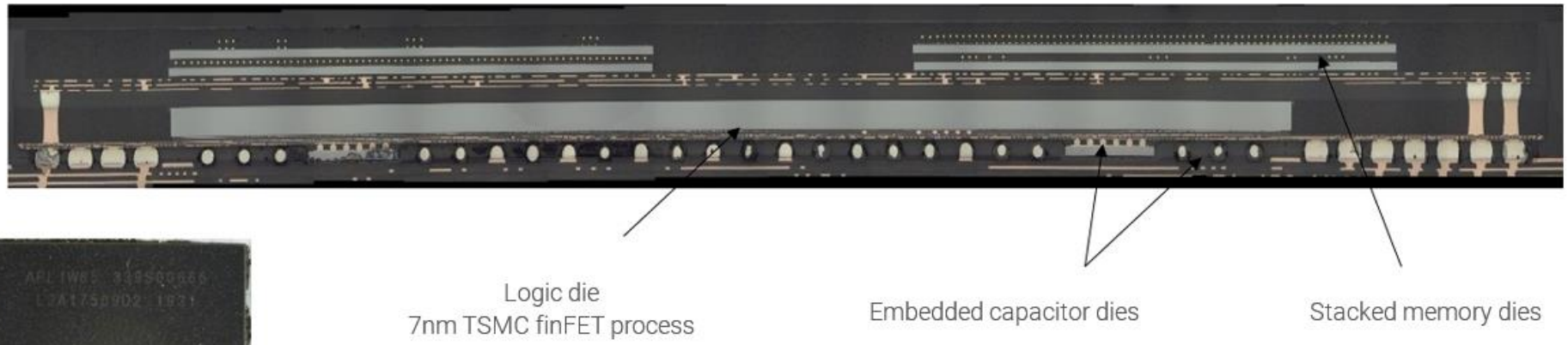
- 5x-10x from Bumping to FOWLP
- 10x from FOWLP to 2.5D Interposer
- >100x from 2.5D Interposer to 3DIC (hyb. Bonded)

CHALLENGES: Package Architecture, Design, Materials, Process Optimization

Ref: VLSI plenary, 2023

Integrated Fan-Out (InFO)

Apple A13 designed by Apple (2019)
(manufactured by TSMC, 7 nm finFET process and packaged by TSMC's InFO technolgy)

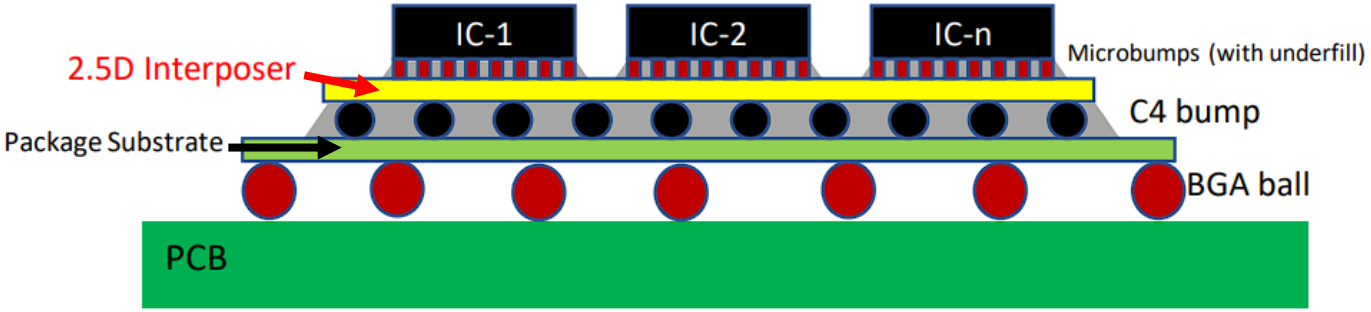


- A13 processors use Integrated Fan-Out.

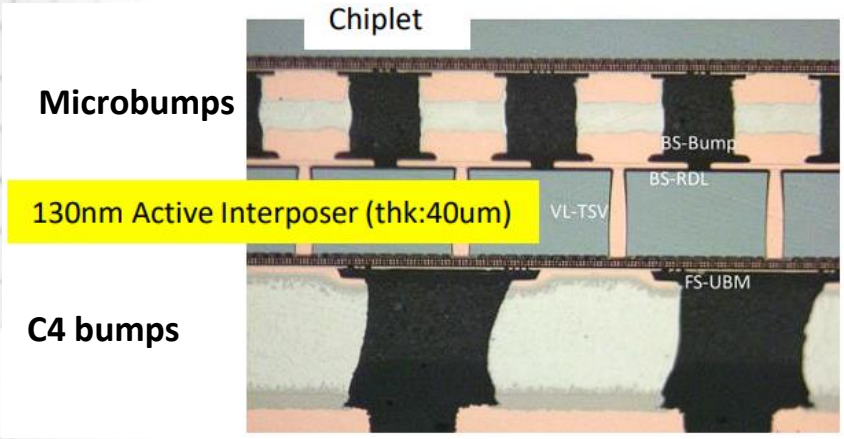
Ref: Tech Insights

2.5D Interposer Packaging (CoWoS)

CoWoS: Chip on Wafer on Substrate

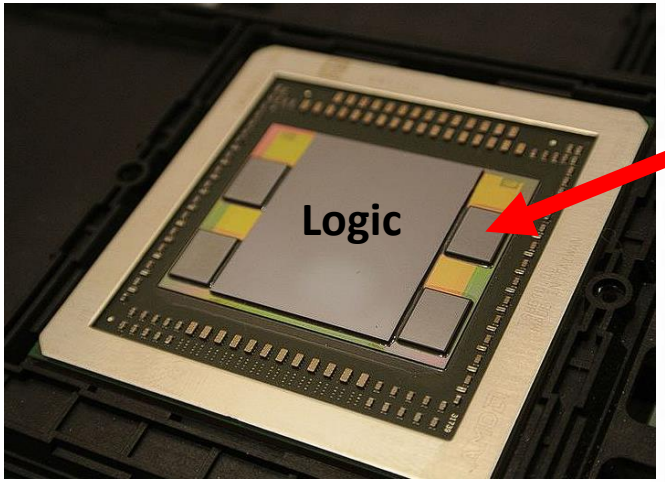


TEM



Ref: VLSI plenary, 2023

AMD GPU



Ref: AMD

Semiconductor manufacturing process

01 Wafer manufacturing

02 Oxidation/ALD

03 Photolithography /EUV

04 Etch

05 Deposition (PVD/Epi) & Ion implantation

06 Interconnect/CMP

07 Testing

08 Packaging

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Wafer Manufacturing

- Most wafers are made of silicon extracted from sand.
- Sand is heated until it melts into a high purity liquid, and then gets solidified by crystallization.

Ref. :
https://media.wired.com/photos/5b6902bff6d47809bff3a57c/4:3/w_2400,h_1800,c_limit/sand-78417588.jpg

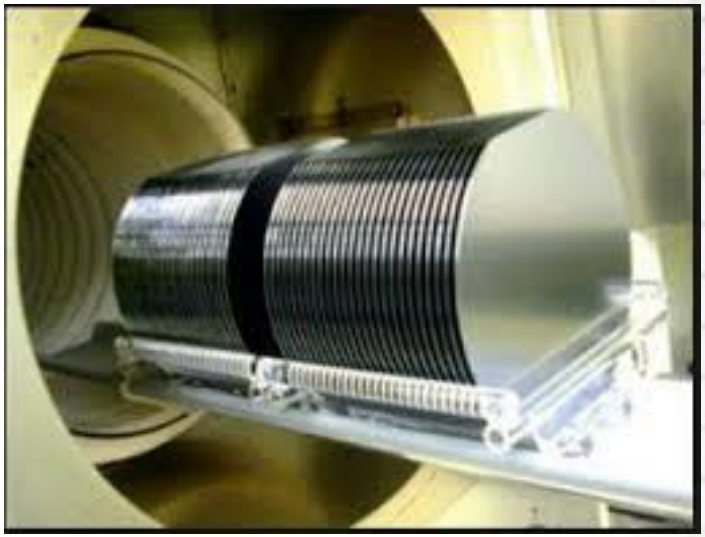
Wafer Manufacturing

- The resultant silicon rod is called and “ingot”. The ingots are sliced into a disc thinly sliced wafers.

Ref. :
https://www.google.com/url?sa=i&url=https%3A%2F%2Fsolarmuseum.org%2Fcells%2Fsilicon-ingot

Wafer Manufacturing

- The surface of sliced wafers is rough and contains defects.
- Polishing machines are used to polish the surface of a wafer.



Ref. :
https://www.google.com/url?sa=i&url=https%3A%2F%2Fhncrystal.en.made-in-china.com

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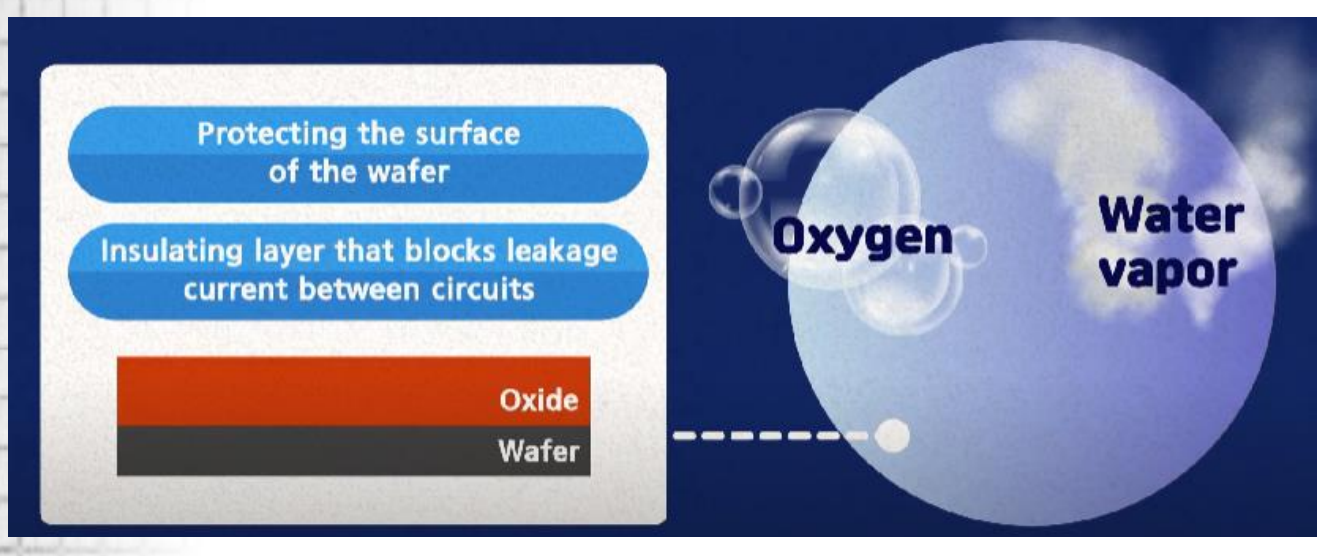
Oxidation

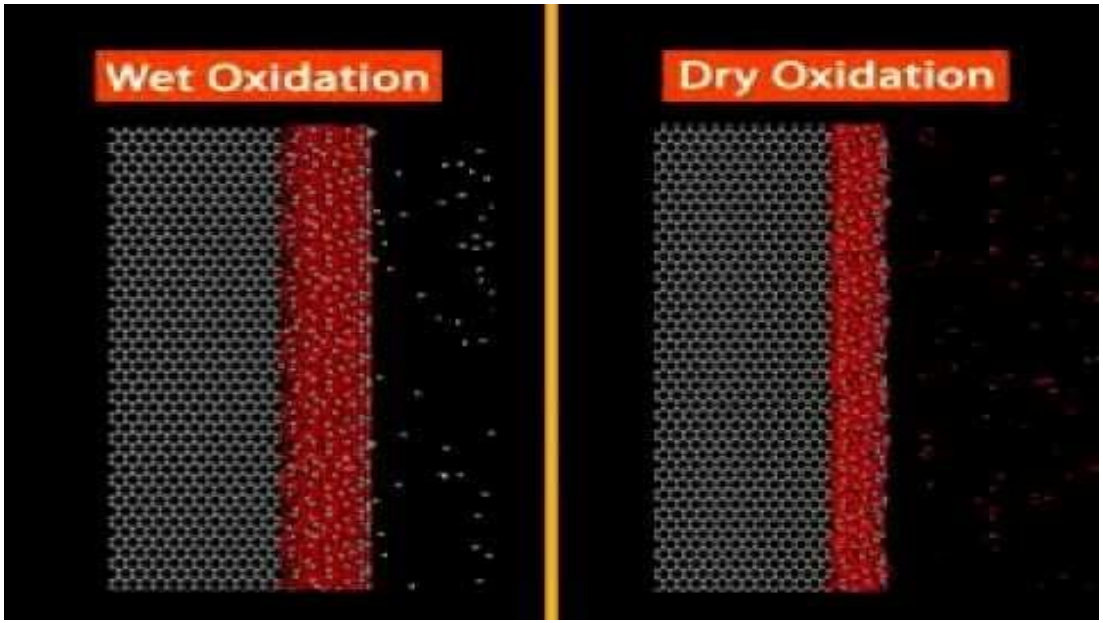
- Oxygen or water vapor is sprayed on the wafer surface to form a uniform oxide film, which protects the wafer surface during the following processes & also blocks current leakage between circuits



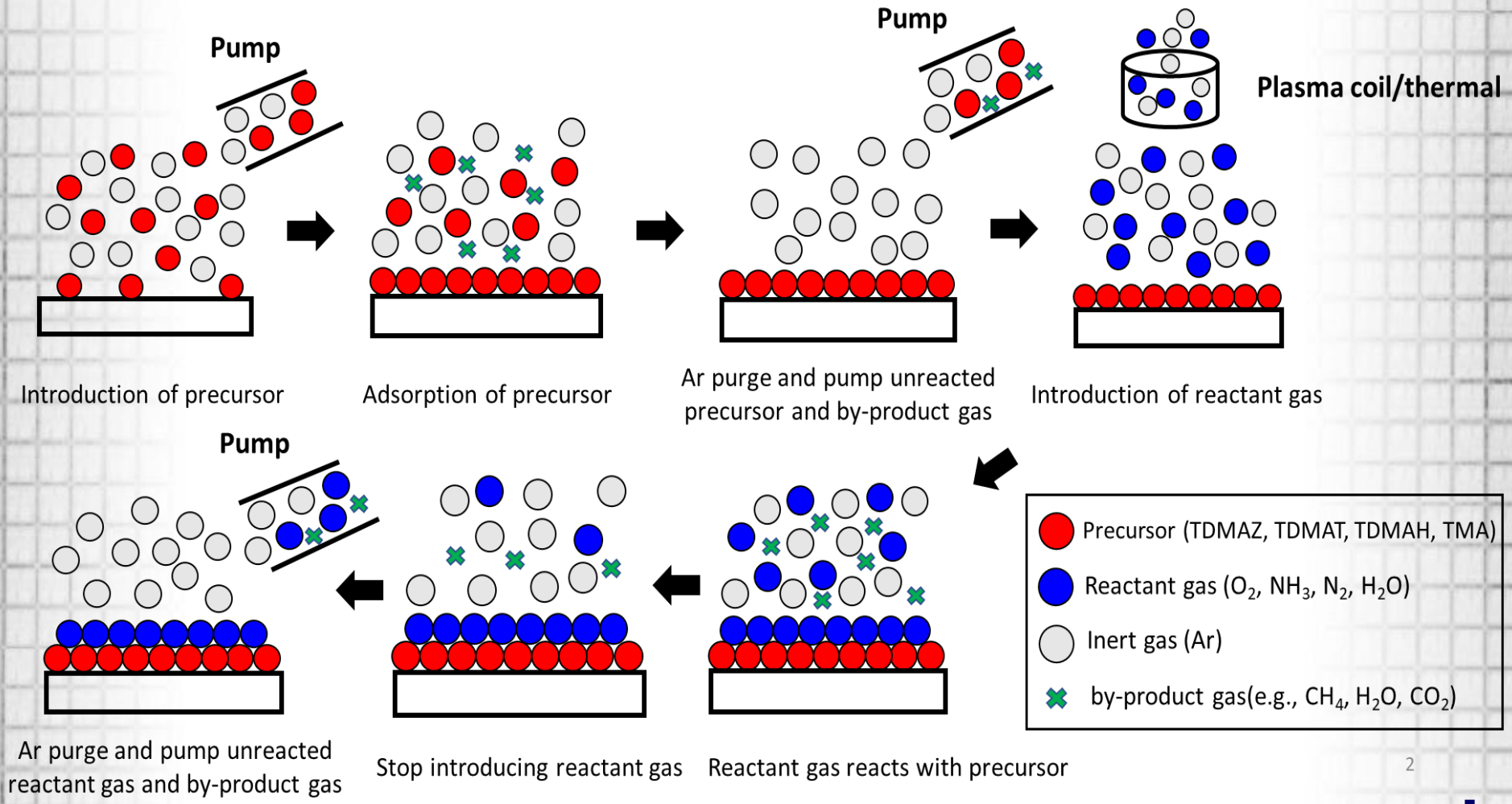
Ref. :
https://www.youtube.com/watch?v=Bu52CE55BN0&ab_channel=SamsungSemiconductorNewsroom

Oxidation

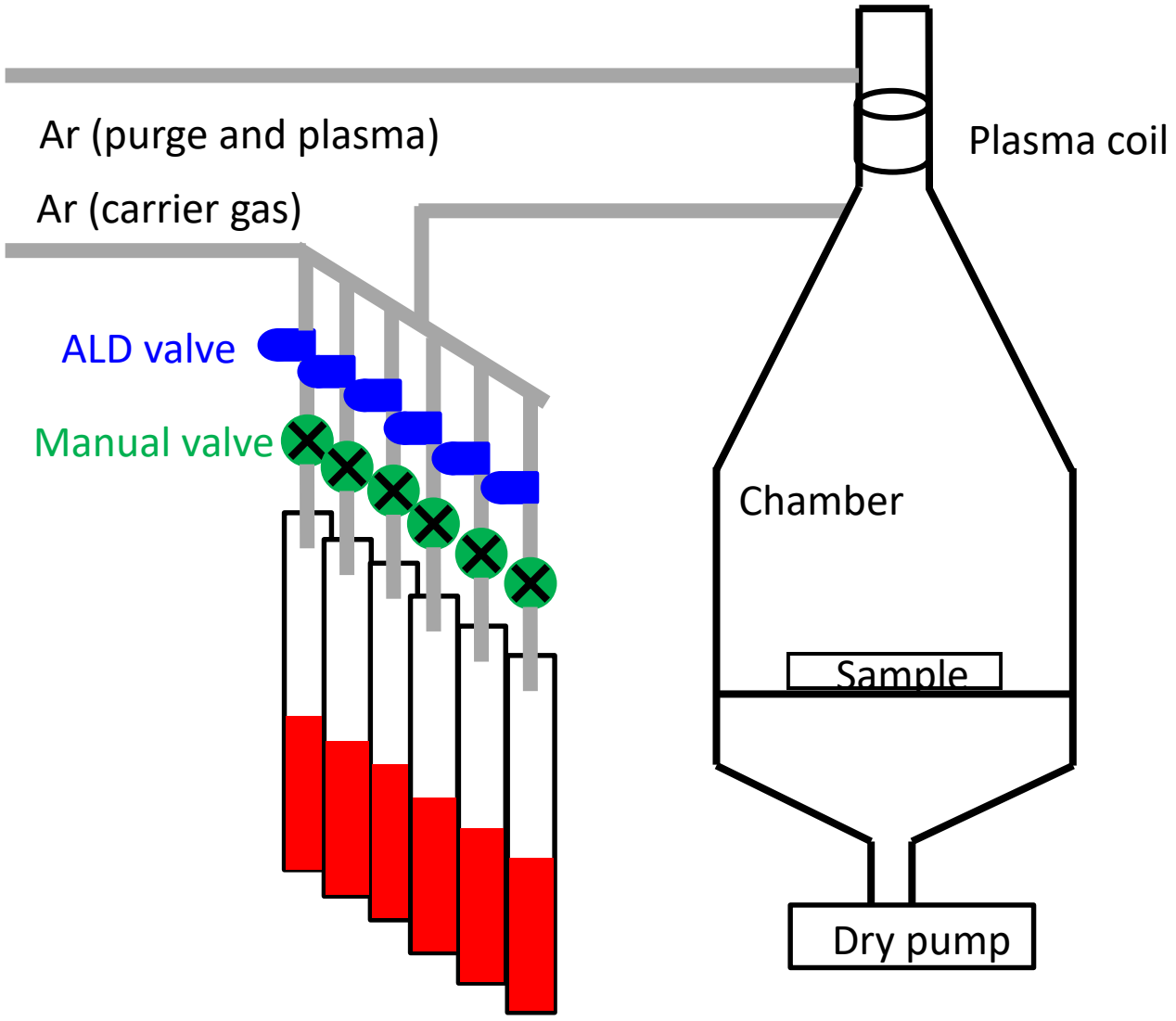
- Different ways of oxidation:
  - Dry oxidation
  - Wet oxidation



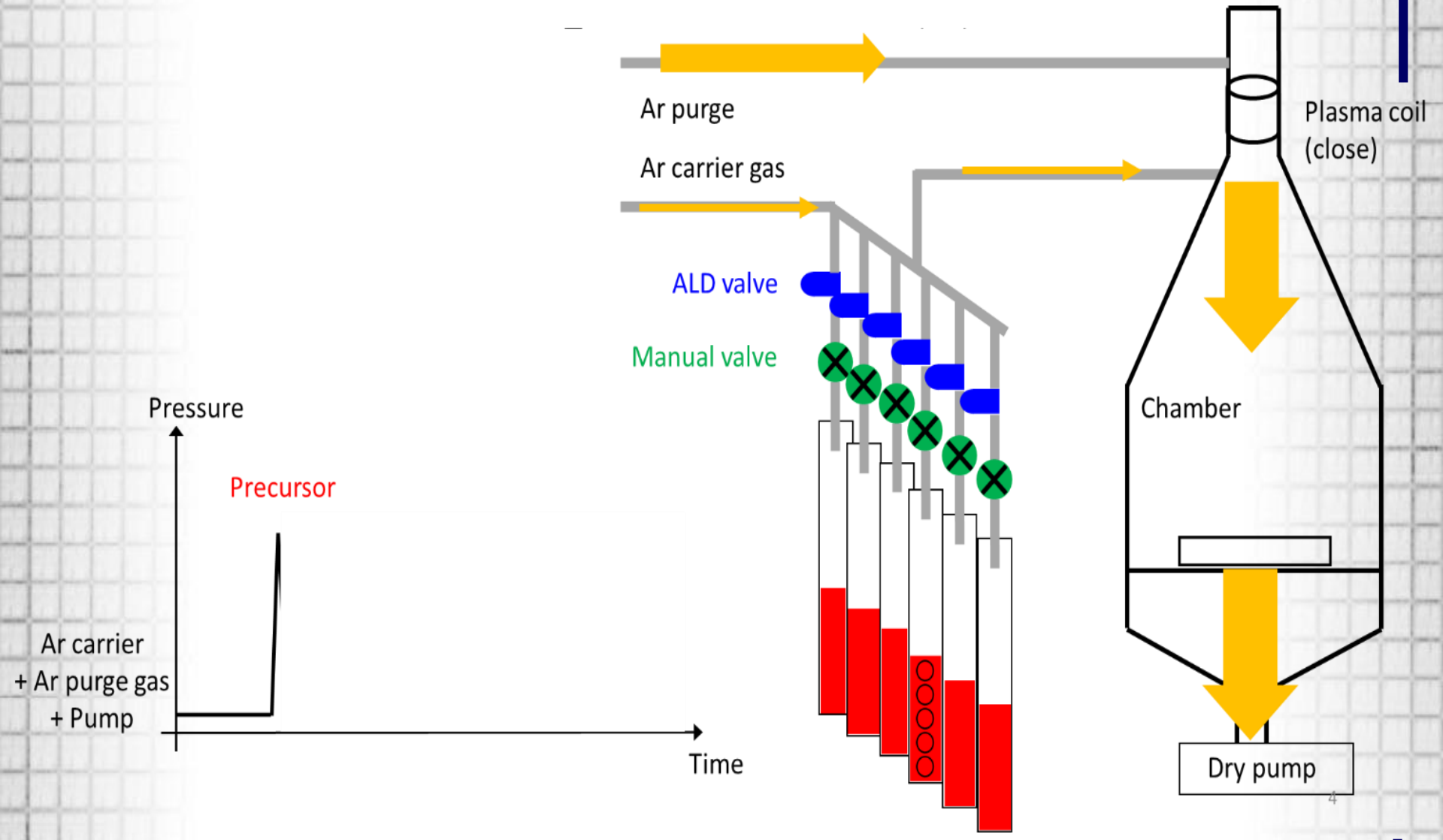
Principles of ALD (Atomic Layer Deposition)



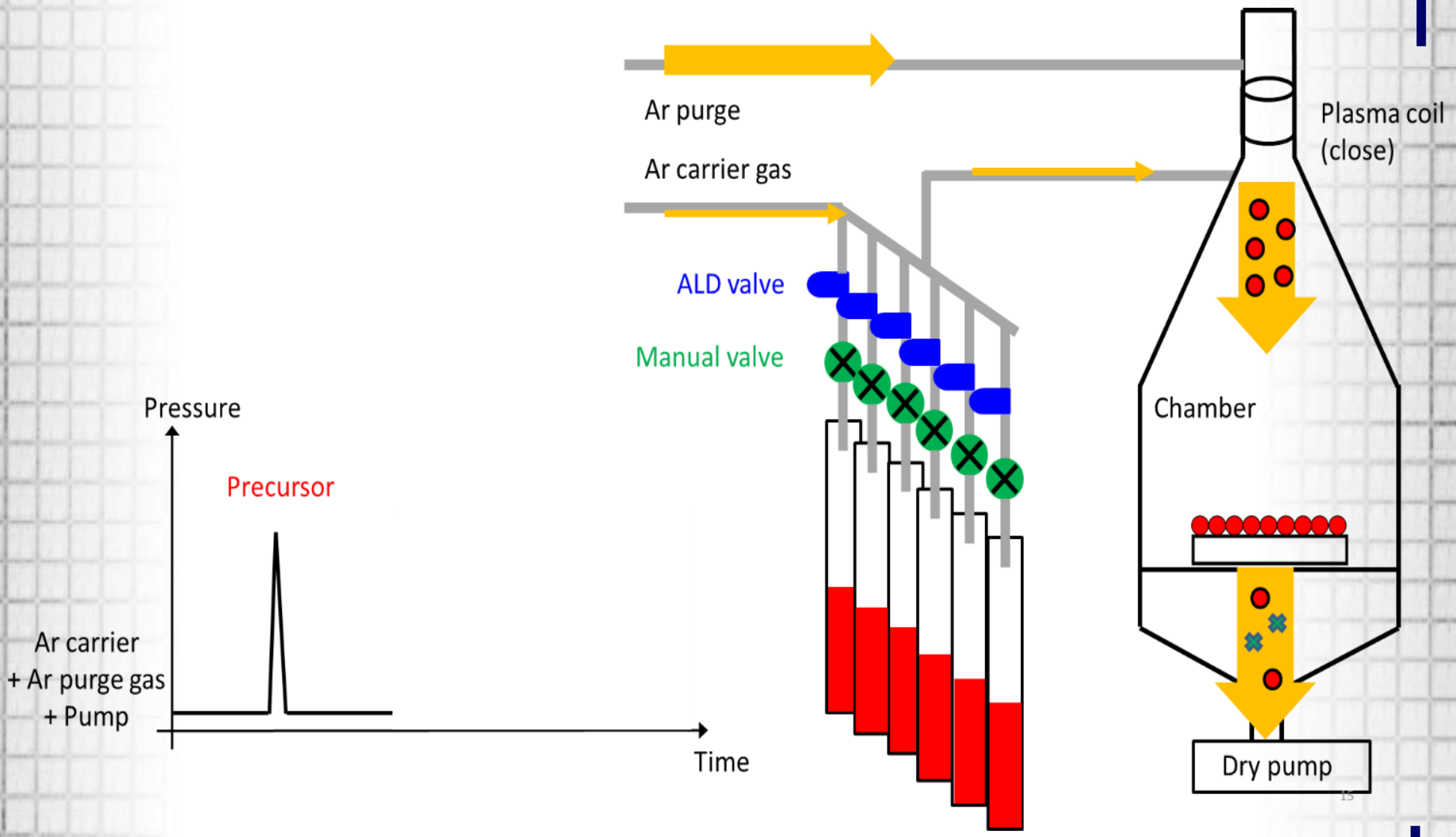
Structure of ALD



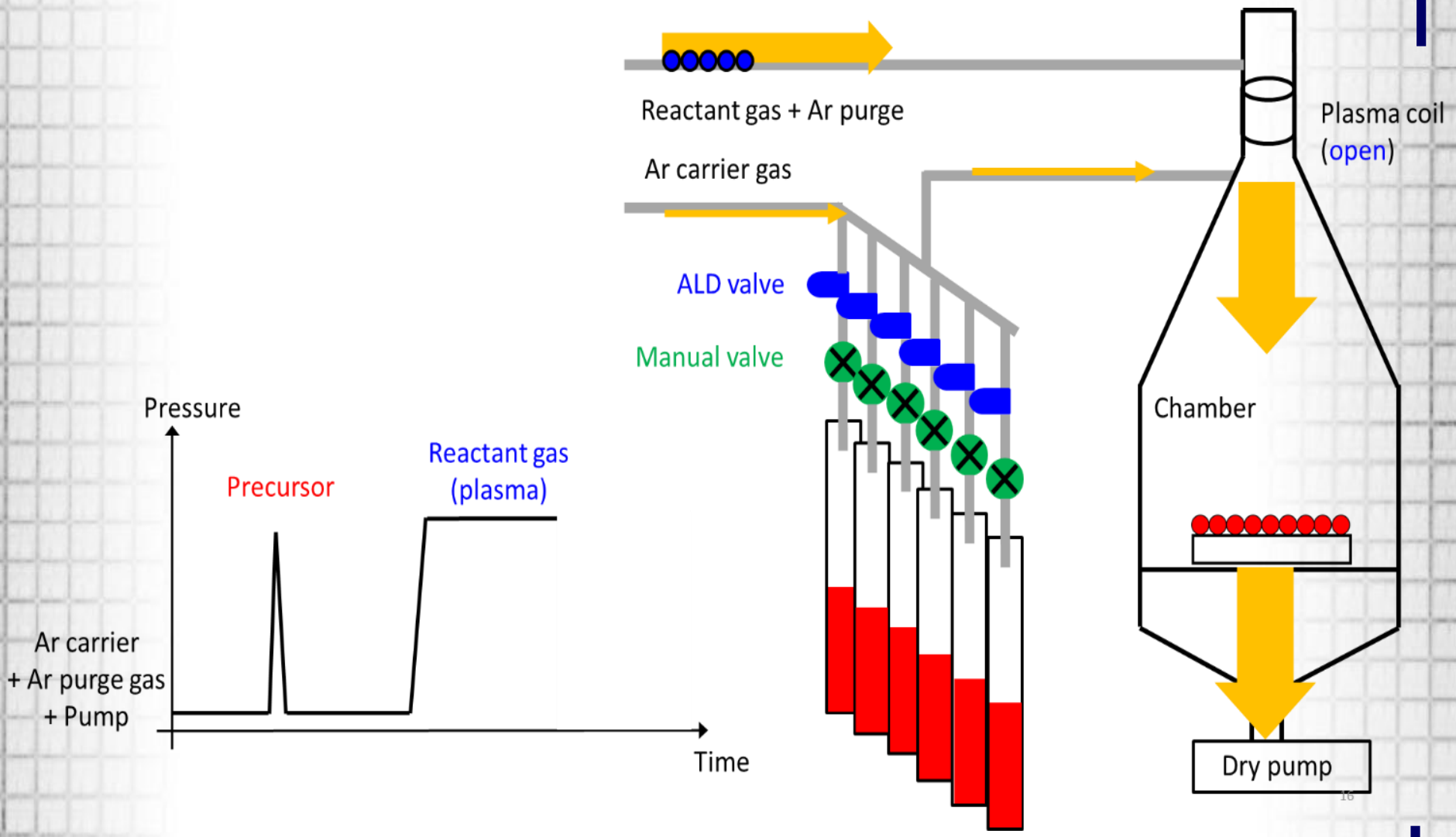
Steps of ALD (1)



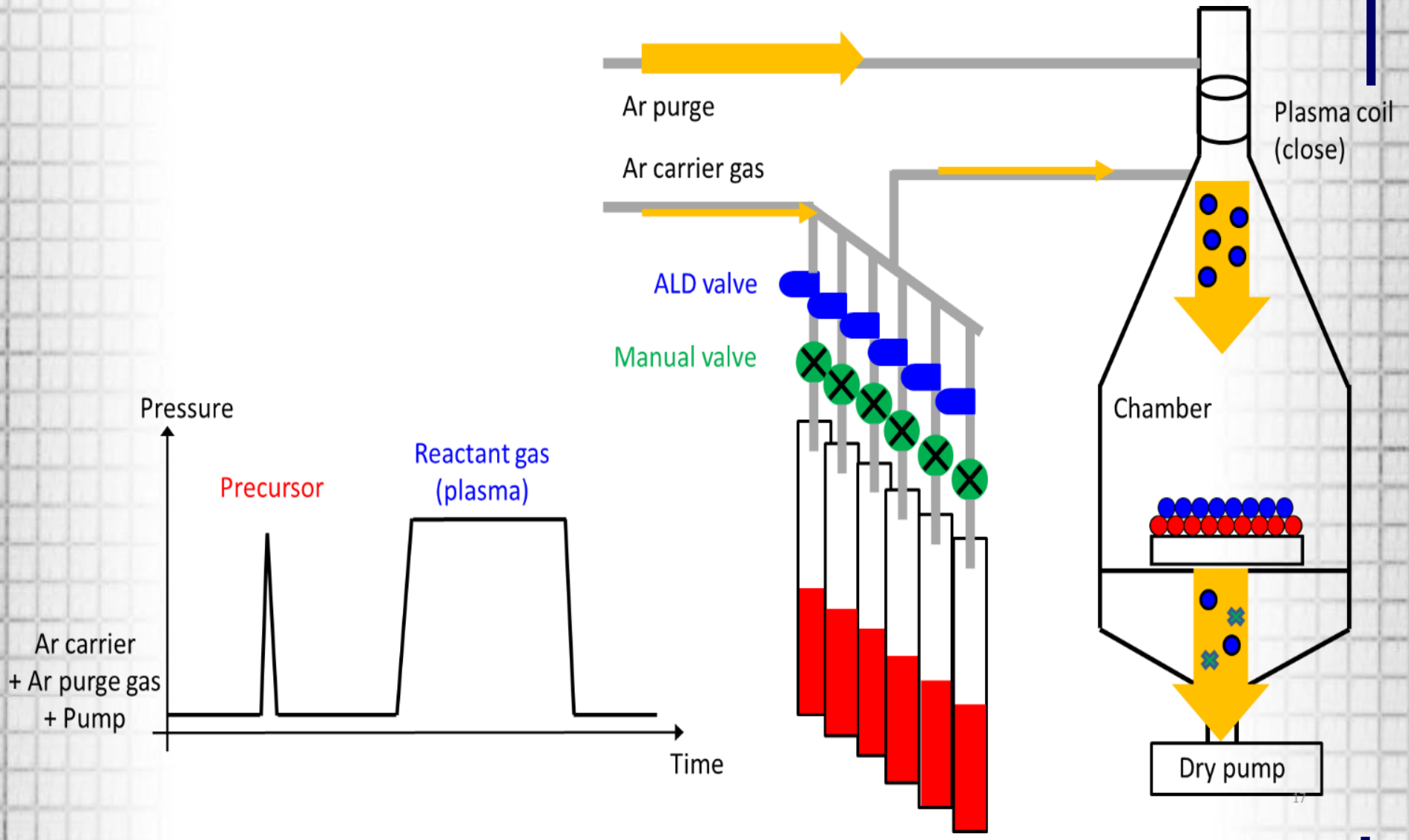
Steps of ALD (2)



Steps of ALD (3)



Steps of ALD (4)



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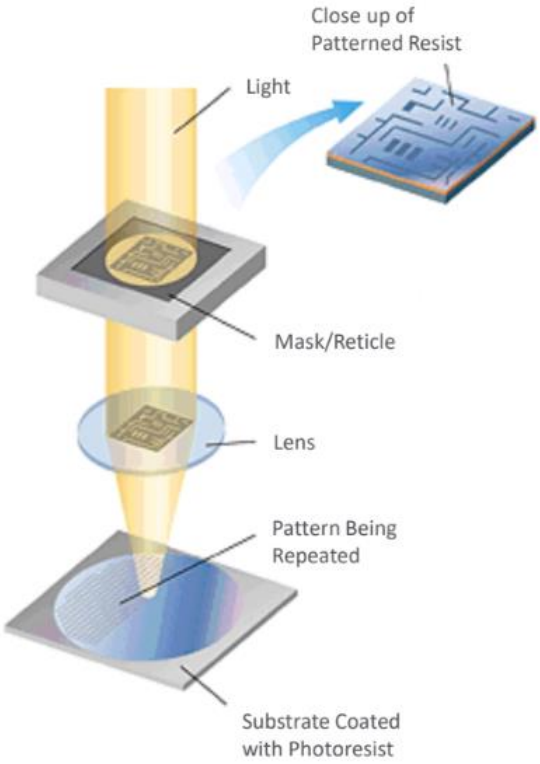
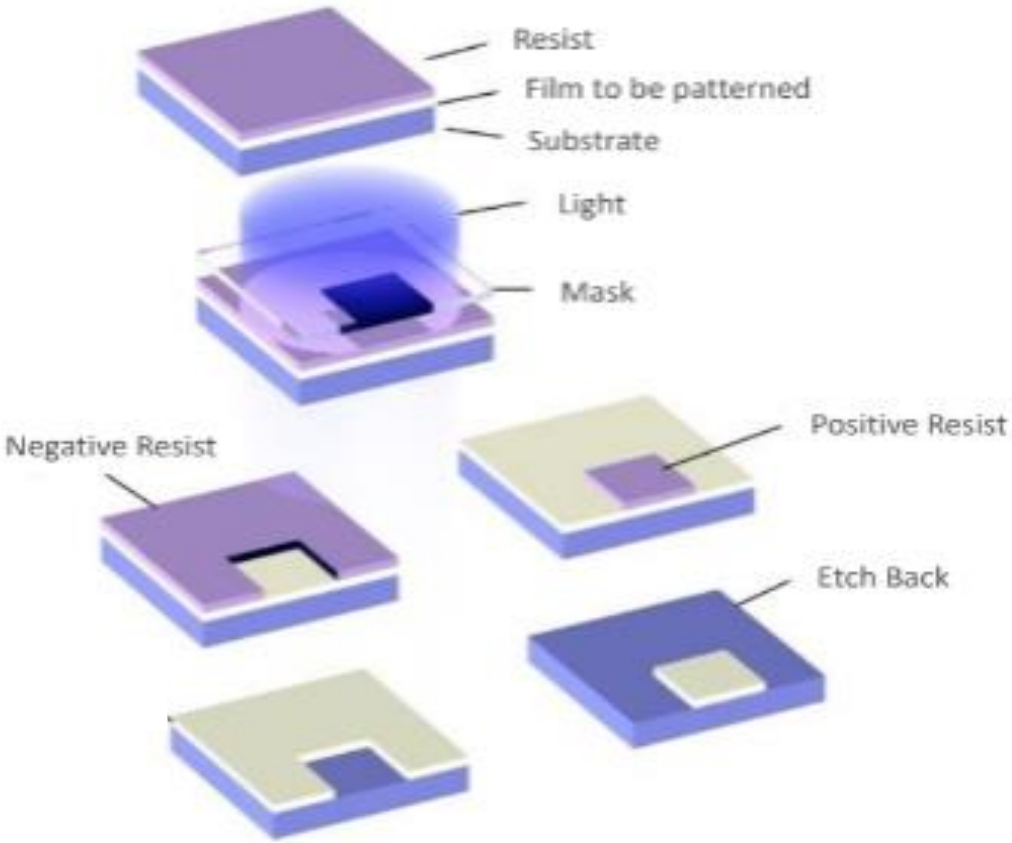
Photolithography



Ref. : AMAT, 2022

- Mask : a glass substrate with a computer-designed circuit pattern
- Photoresist : a material that responds to light, is applied thinly and evenly on the oxide film previously placed on the wafer
- When light transfers the patterned mask, the circuit is drawn on the wafer surface

Two Types of Resists



Ref. : http://britneyspears.ac/physics/fabrication/photolithography.html

Two Types of Resists

Negative Resist

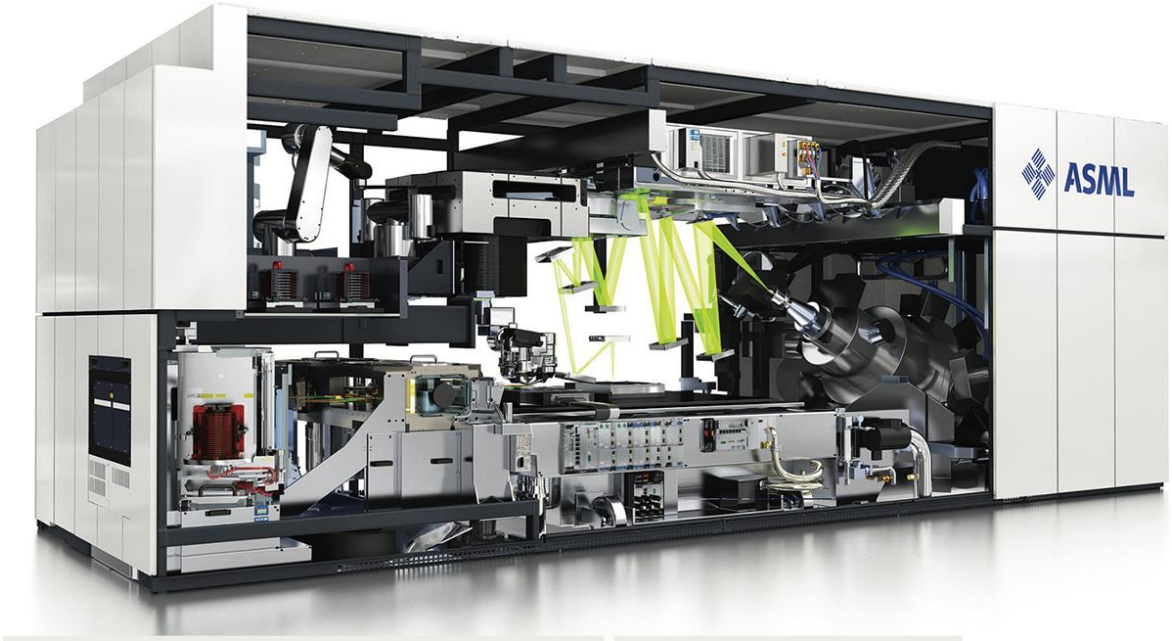
- Pattern to "open" area on mask
- Exposed portion is retained
- Profile is undercut

Positive Resist

- Pattern to "blocked" area on mask
- Exposed portion is removed
- Profile is tapered

Ref. : http://britneyspears.ac/physics/fabrication/photolithography.html

EUV



Ref. : ASML

- The Twinscan EXE:5000-series made by ASML costs around 270 million euros.

Evolution of lithography systems at ASML

In ~40 years:

From >1 μm to <10nm resolution → >100x reduction

Steppers → **Scanners**

	1984	1985-89	1990s	2000s	2010s
	PAS 2000	PAS 2500/5000	PAS 5500	NXT TWINSCAN	NXE EUV scanners
CD:	1.2 - 0.7 μm	< 500 nm	400-90 nm	100 to <40 nm	50 to <15 nm
Overlay:	250 nm	100 nm	100-12 nm	20 - 2 nm	3 to <2 nm
λ:	436, 365 nm	365, 248 nm	365, 248, 193 nm	365, 248, 193 nm	13.5 nm

Ref. : VLSI short course, 2023

Evolution of lithography systems at ASML

With the arrival of High NA EUV scanners the size gets even bigger

2020s

EXE EUV scanners

CD: 20 to <10 nm

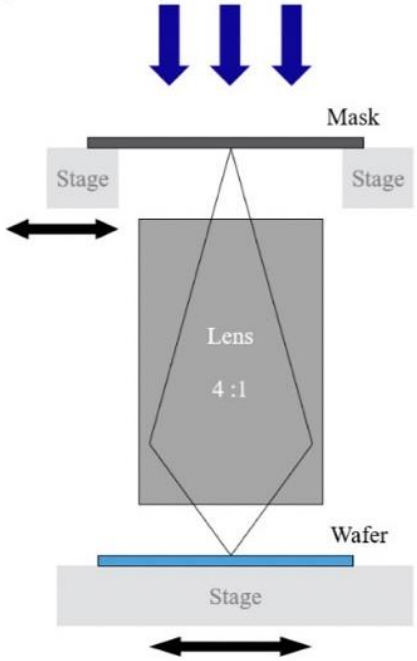
Overlay: 2 to <1 nm

λ: 13.5 nm

Ref. : VLSI short course, 2023

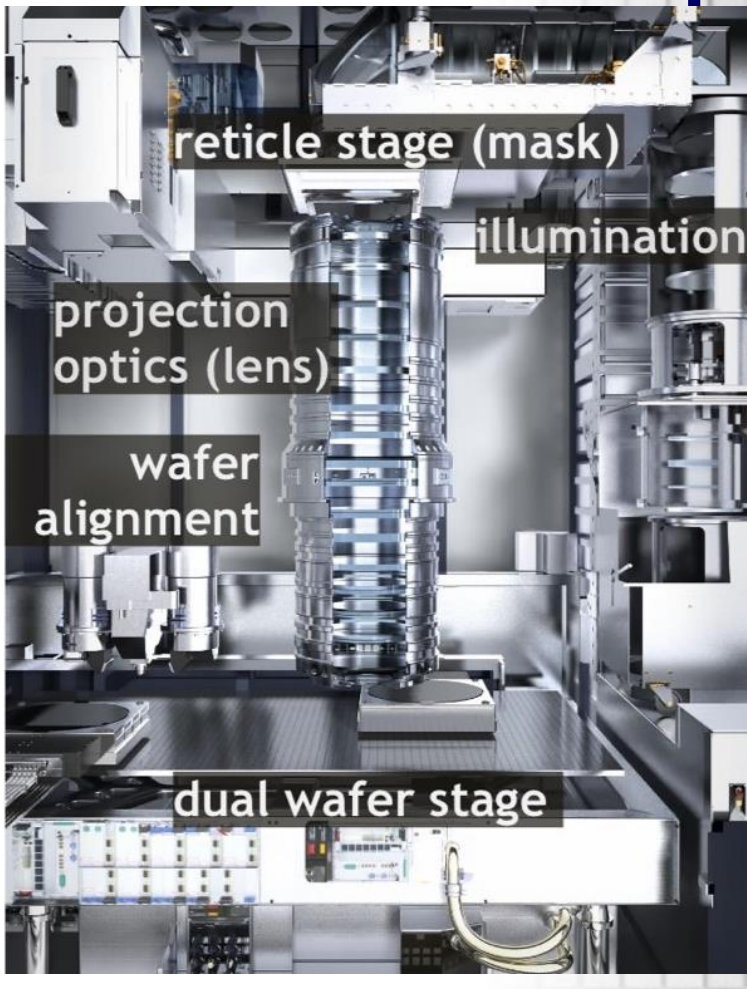
Photolithography in Action

How circuit patterns are printed on the wafer



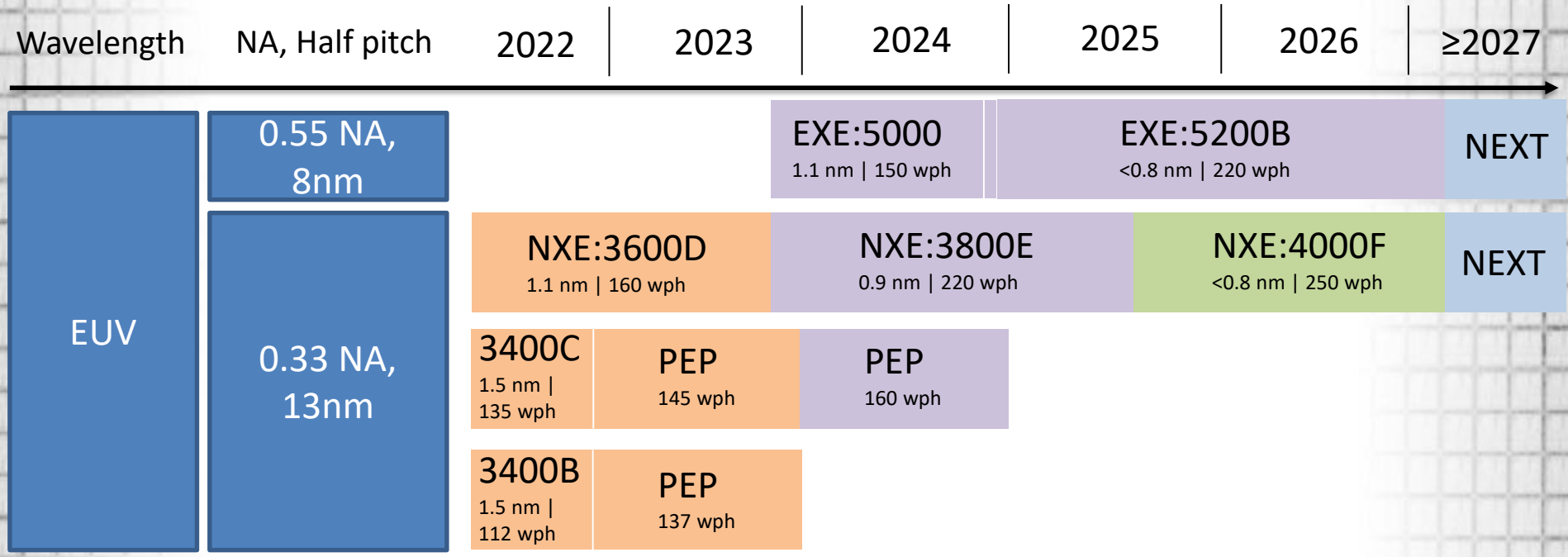
Min. Half-Pitch $= k_1 \frac{\lambda}{\mathrm{NA}}$

- λ: exposing wavelength
- NA: numerical aperture of the lens
- k_1 depends on resist, mask, illumination
- $k_1 \geq 0.25$



Ref. : VLSI short course, 2023

EUV Product Roadmap



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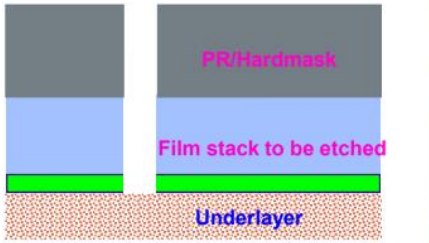
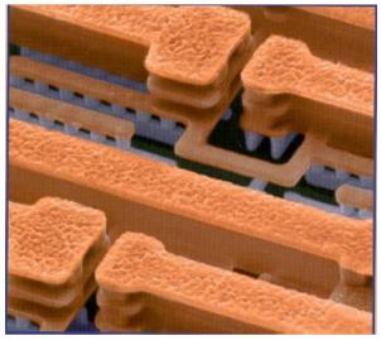
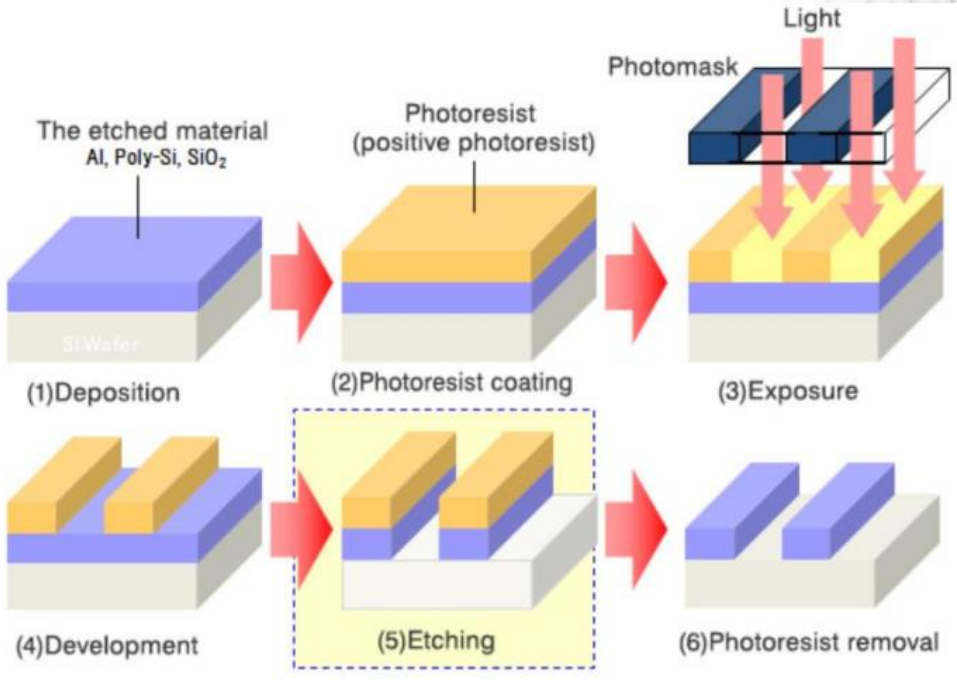
Etch



Pro. 2000 IITC, Cover ->



Cu BEoL



Ref. : https://www.hitachi-hightech.com/global/products/device/semiconductor/etch.html

- Etching is a selective pattern transfer or micromachining.

Anisotropic v.s. Isotropic

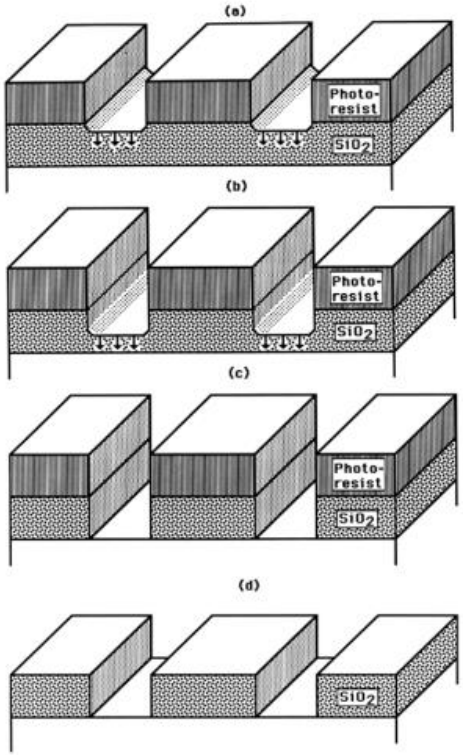
Pattern resist mask

Etching thin film

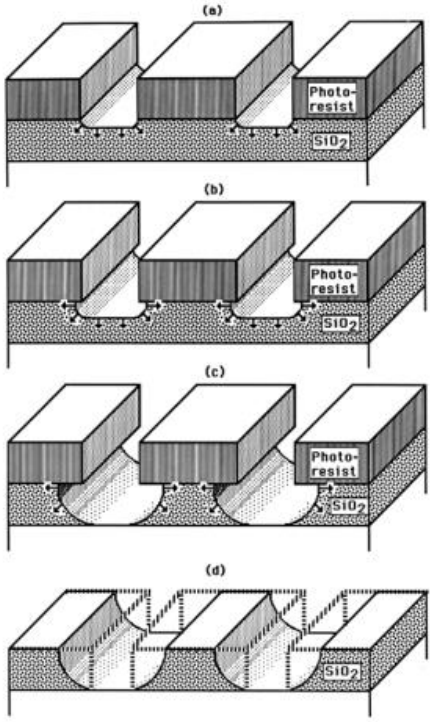
Etching completed

Remove resist mask

Processing Temperature
Ambient



Anisotropic
(e.g. Reactive Ion Etching)

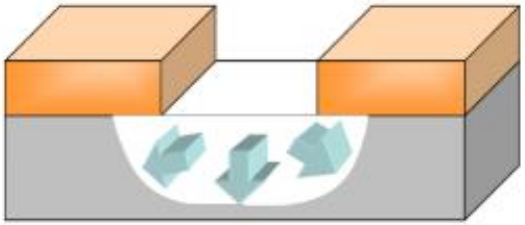


Isotropic
(e.g. Wet Etching)

Ref. :
Prof. Nathan Cheung,
U.C. Berkeley

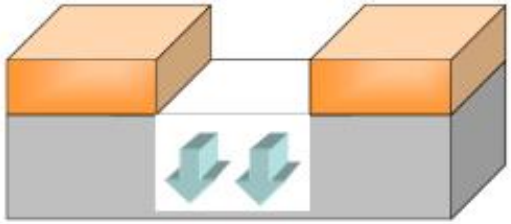
Wet Etching v.s. Dry Etching

Wet Etching
- by Wet chemical solution
- Isotropic etching



Vertical E/R ≒ Horizontal E/R
Pure Chemical Reaction
High Selectivity
CD Loss or Gain

Dry Etching
- by Plasma
- Anisotropic etching



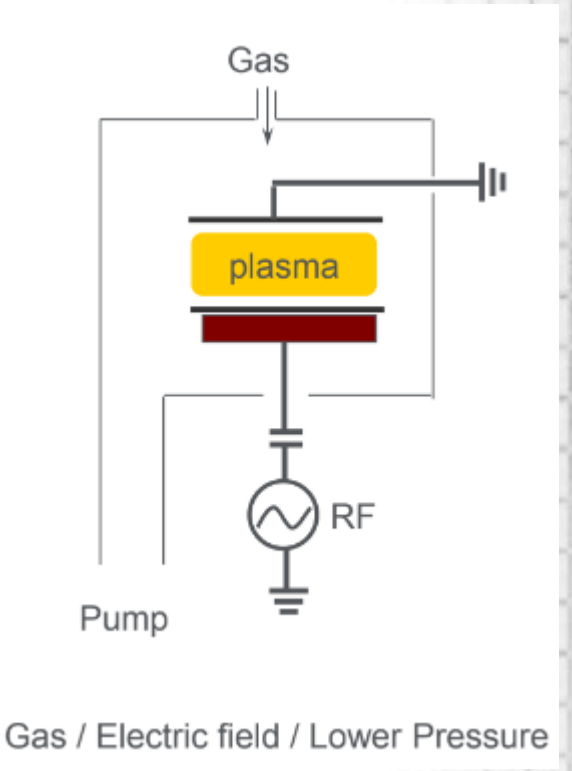
Vertical E/R >> Horizontal E/R
Ion assisted
Relatively low Selectivity
No CD bias

Ref. : AMAT, 2022

- Etching removes unnecessary materials so that only the designed pattern remains

Basic Plasma Concept

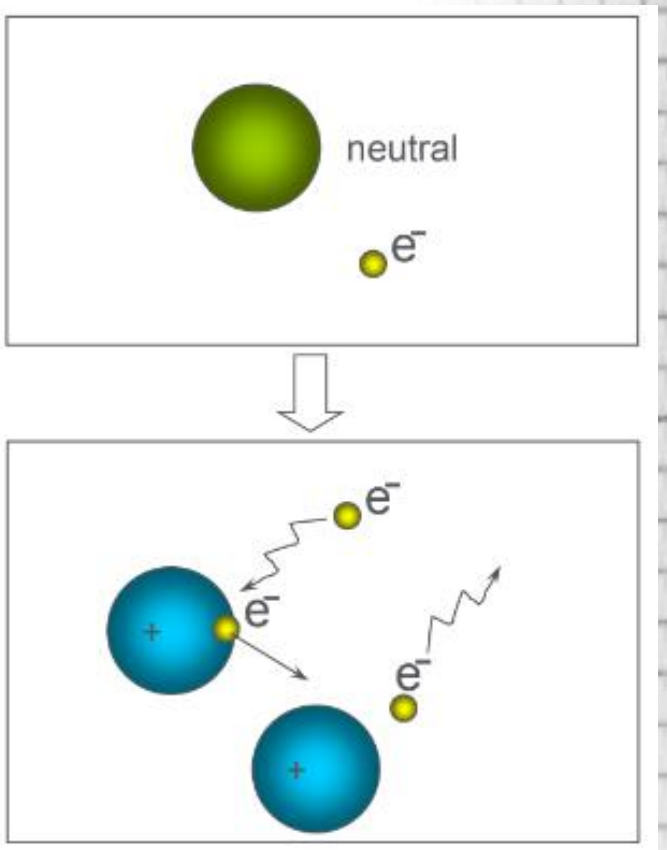
- Plasma is formed when an avalanche of ionization occurs.
- This results in a “ sea” of positive and negative charged particles
- Plasma is partially ionized gas, on the average electrically neutral.
- The diagram indicates CCP (Capacitive Coupled Plasma) chamber.



Ref. : AMAT, 2022

Basic Plasma Concept: Ionization

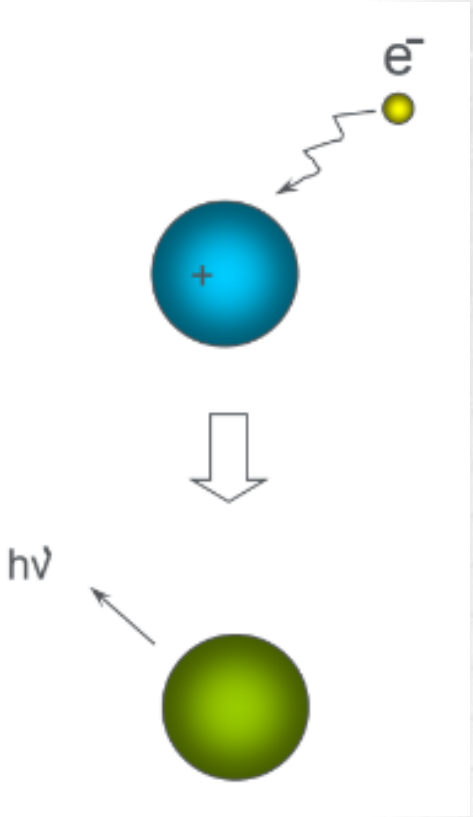
- Initially, very few electrons are present in a neutral gas.
- The electrons are accelerated by energy input and ionizing the neutrals.
- Newly produced electrons accelerate and ionize more neutrals and ionized avalanche happened.
- If the applied voltage is high enough, the number of electrons and ions increases until the plasma is formed.



Ref. : AMAT, 2022

Basic Plasma Concept: Recombination

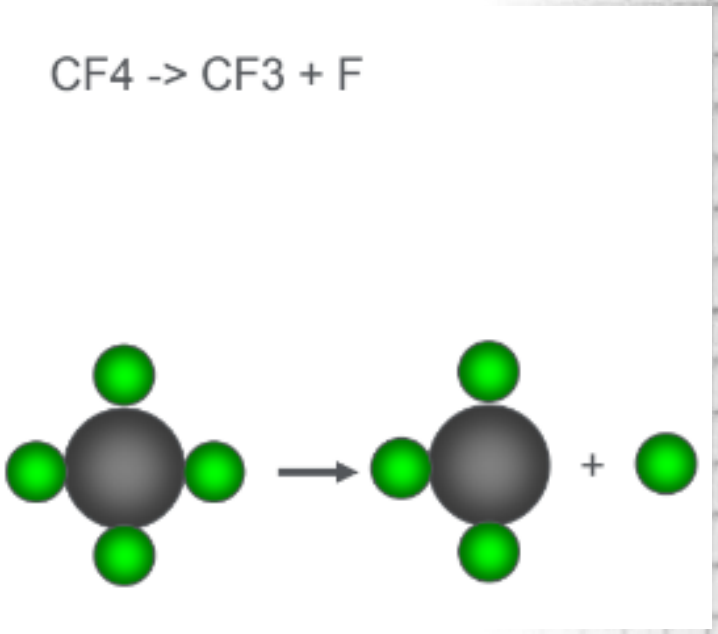
- Recombination occurs when an electron and ion recombine in the plasma.
- Light is emitted.



Ref. : AMAT, 2022

Basic Plasma Concept: Dissociation

- Dissociation occurs when an electron collides with a molecule with enough energy to break its bonding energy into apart.
- Dissociation requires much less energy than ionization.
- The dissociation rate is much higher than the ionization rate.



Ref. : AMAT, 2022

Semiconductor manufacturing process

01 Wafer manufacturing

02 Oxidation/ALD

03 Photolithography /EUV

04 Etch

05 Deposition (PVD/Epi) & Ion implantation

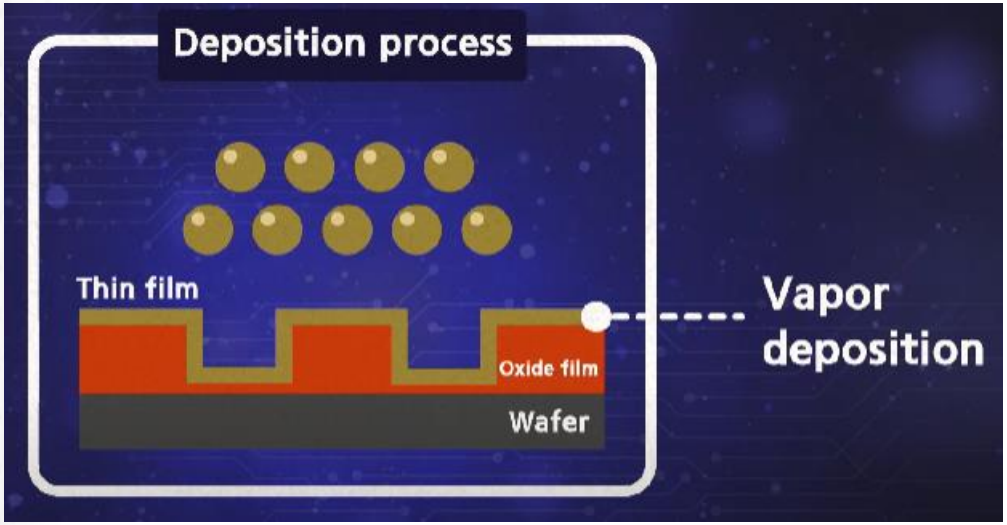
06 Interconnect/CMP

07 Testing

08 Packaging

Deposition

- The photolithography and etching process are repeated several times on the wafer, layer by layer.
- Deposition : coating the thin film at a desired molecular or atomic level onto a wafer.

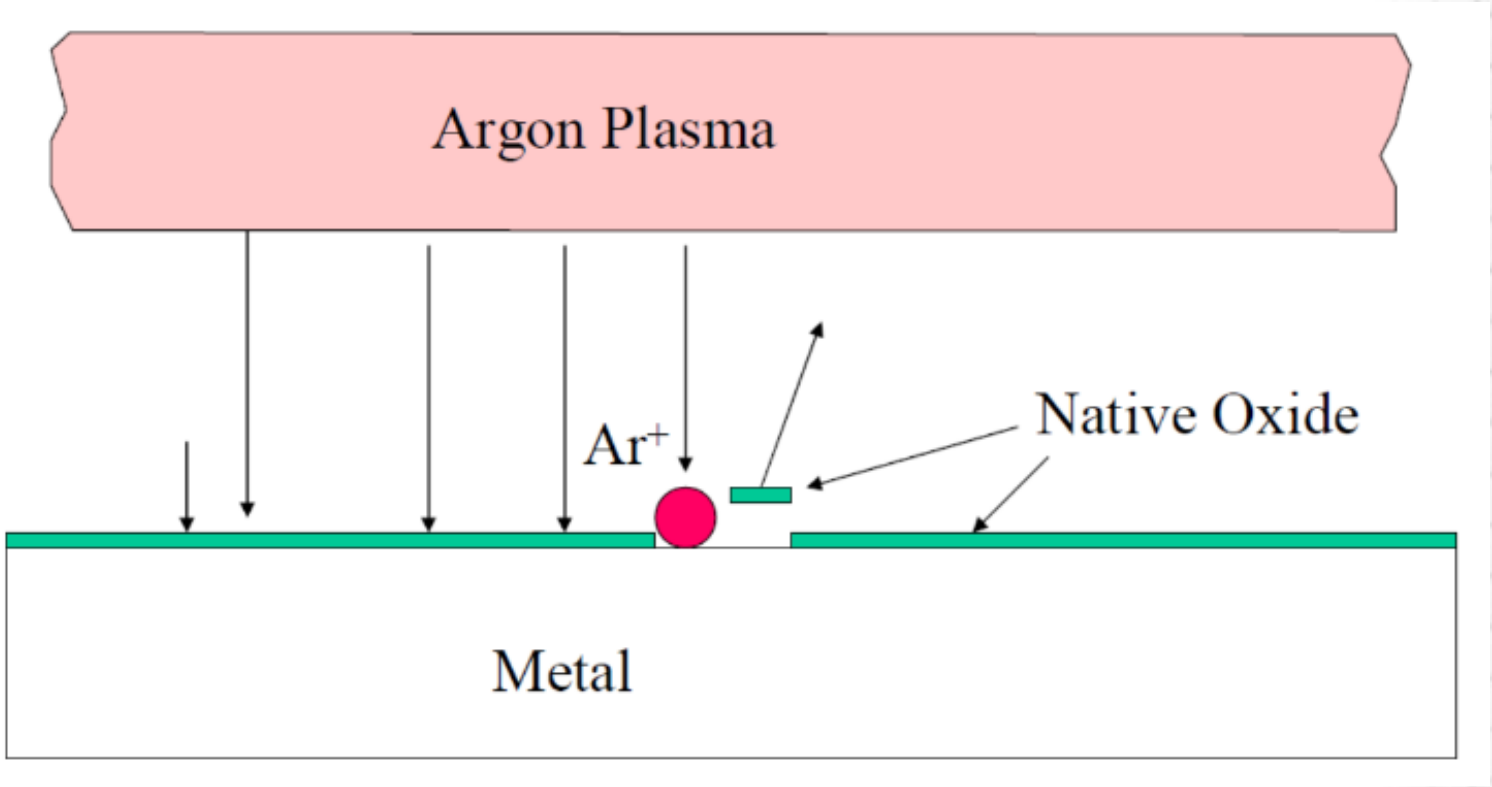


Ref. :
https://www.youtube.com/watch?v=Bu52CE55BN0&ab_channel=SamsungSemiconductorNewsroom

Pre-clean Technology

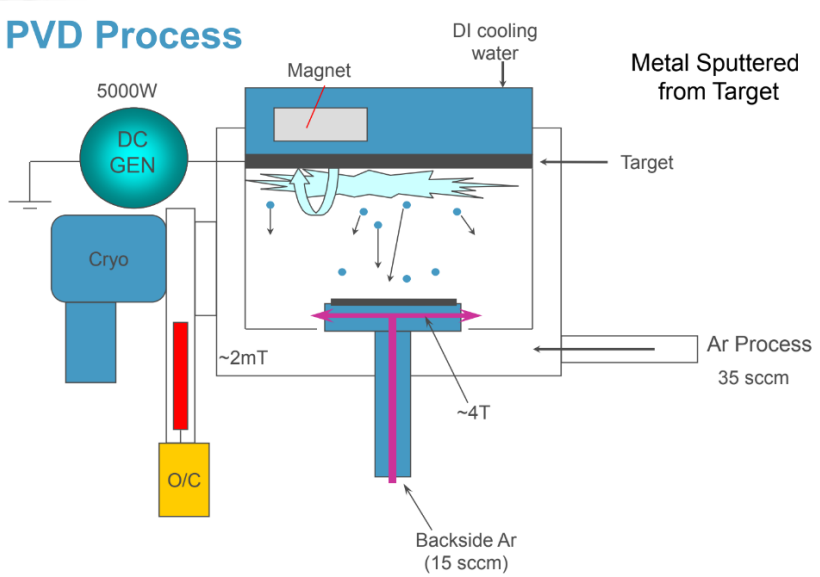
- Physical Clean
  - Ar Sputter
  - Native oxide & Metal oxide
- Chemical Clean
  - Selective etch
  - Isotropic etch
  - Radical clean
- Physical + Chemical Clean
  - Ar Sputter + Chemical Etch

Pre-clean Process



Ref. : AMAT, 2022

Physical Vapor Deposition (PVD)



Ref. : http://www.appliedmaterials.com/products/endura-extensa-ttn

- PVD process build up the metal wire and contact for signal transfer.
- PVD deposition processes are used in creating ultra-thin cap layers and metal gate films in high-k/metal gates for advanced transistors, and in forming ultra-thin barrier materials and seed layers for interconnects.

Plasma for PVD

- Plasma is a gas that contains
  - Neutral atoms
  - Positive ions
  - Negative electrons (same number as ions)
- Created by giving energy to a gas
  - Heat, DC current, RF current, etc.
- Ar is the most common gas for sputtering

Step Coverage : Most Important Item for PVD

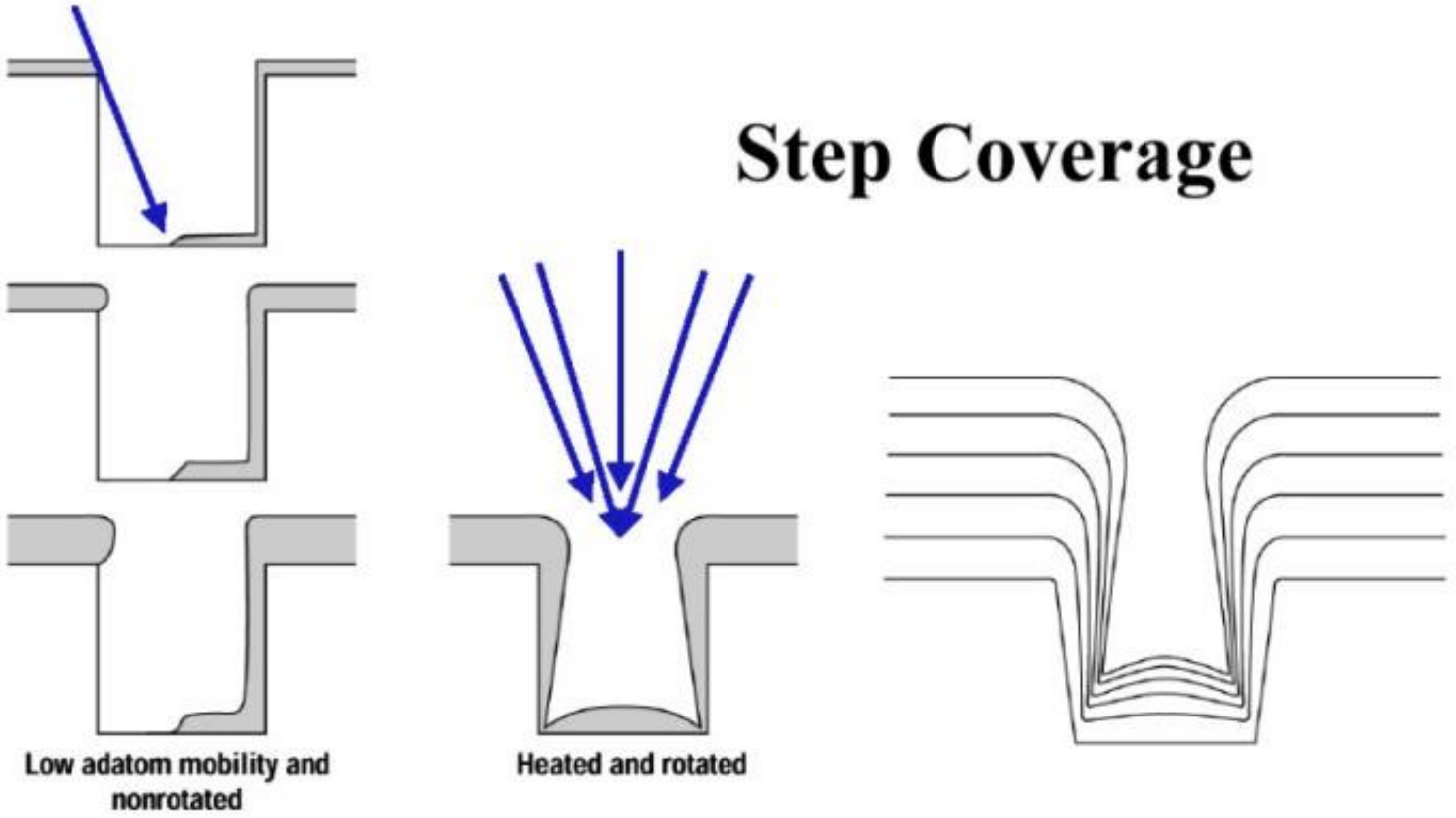
Before Deposition

After Deposition

Ref. : AMAT, 2022

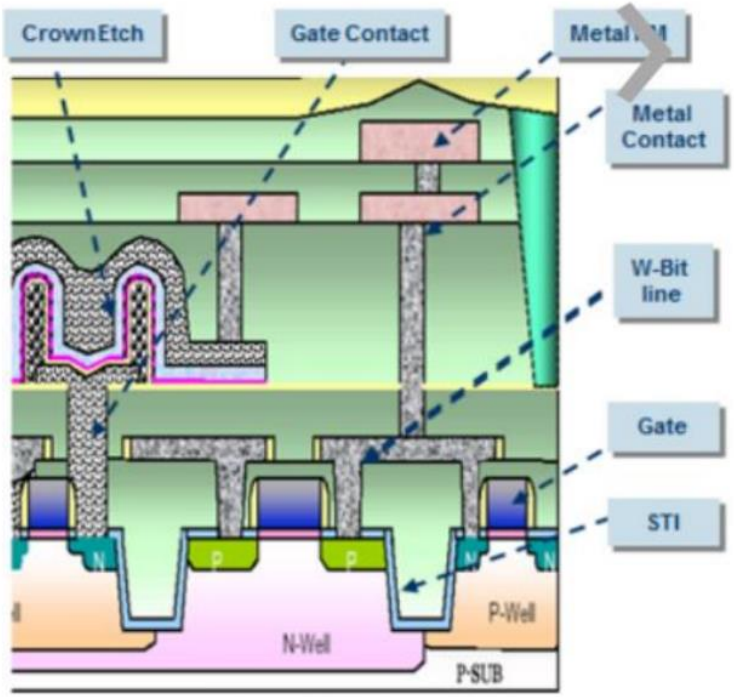
- It is a measure of how well the film covers topography.

Step Coverage concerns in contacts



Ref. : https://inst.eecs.berkeley.edu/~ee143/fa16/lectures/Lecture06-Thin%20Film%20Deposition.pdf

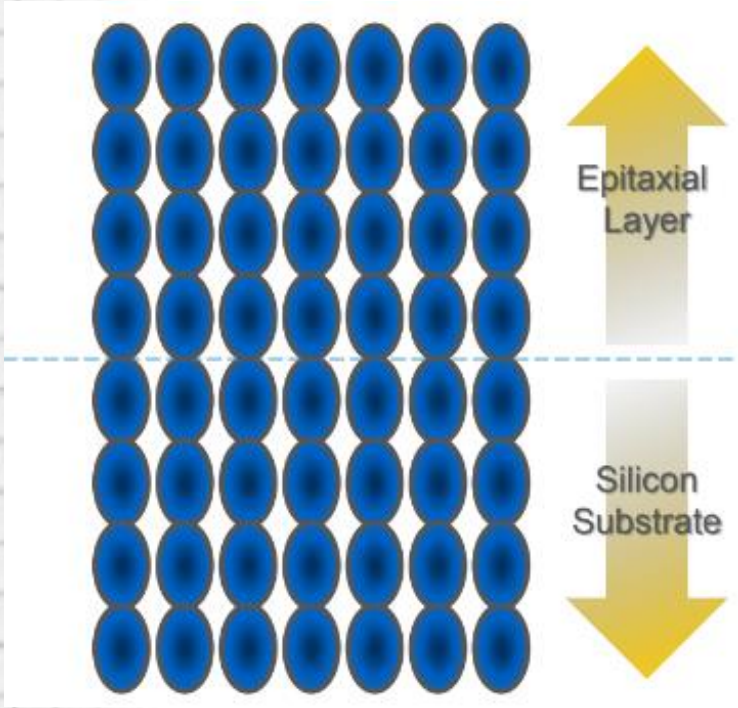
Chemical Vapor Deposition (CVD)



Ref. :
http://www.appliedmaterials.com/products/producer-apf-pecvd

- CVD is the process of depositing solid films using gases or vapors through chemical reaction on the substrate surface.

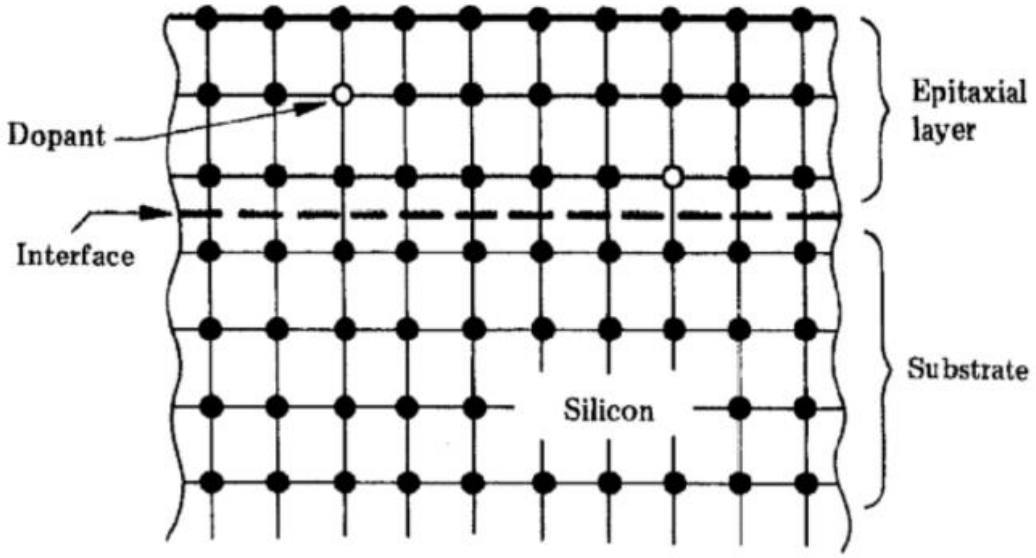
Epitaxy



- Growing a monocrystalline film which takes on a lattice structure and orientation identical to the substrate
- This enables a high-purity starting point for building a semiconductor device

Ref. : AMAT, 2022

Epitaxial Growth

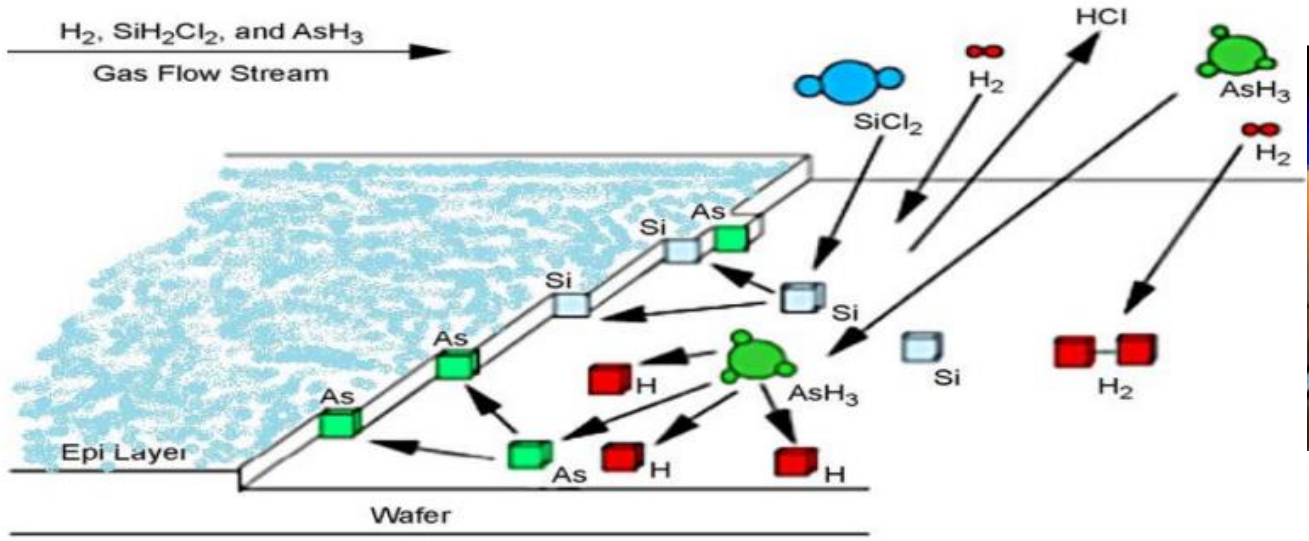


Ref. :
Prof. Nathan Cheung, U.C. Berkeley

- Requires an ultra-clean Si surface prior to epi growth
- Requires deposition of Si at very high temperature for perfect crystallinity

Epi Process

Ref. : http://www.appliedmaterials.com/products/centura-epi-



- Epitaxial deposition is chemical vapor deposition (CVD) in which single crystal silicon is deposited on bare wafer.

Chemical vapor deposition (CVD) epitaxy

Precursors

SiH_4
GeH_4
DCS
$SnCl_4$
Ge_2H_6
PH3
B2H6

Pressure, temperature, flow rate, carrier gas

Epitaxy

Si
Ge
SiGe
GeSn
Si:P
Ge:B
GeSn:B
GeSn:P
...

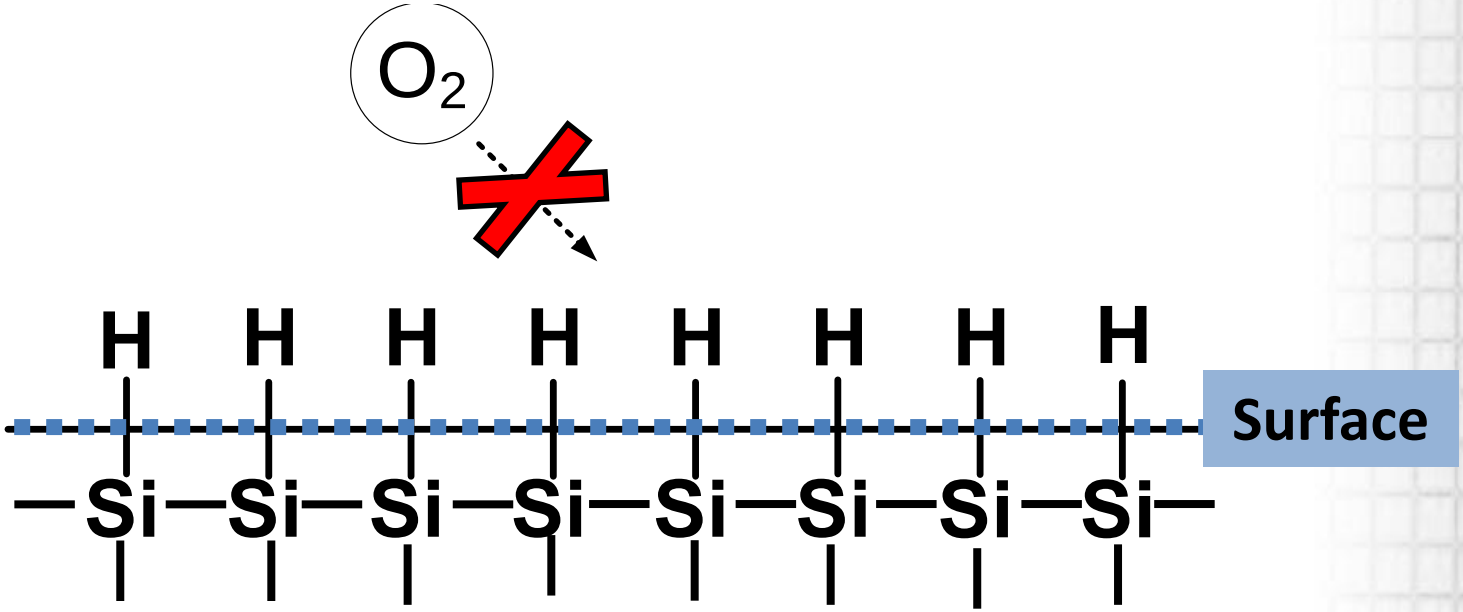
CVD-grown epi-Si/SiGe/Ge

Process flow

- Si wafer clean: HF dipping
- H_2 baking to remove the native oxide
- Epitaxial growth by RTCVD
- Material analysis of epilayers (TEM, AFM, XRD, RSM, PL…….)
- Devices fabrication

TEM: Transmission Electron Microscope
AFM: Atomic Force Microscope
RSM: Reciprocal Space Mapping
PL: Photoluminescence

Surface Pre-cleaning



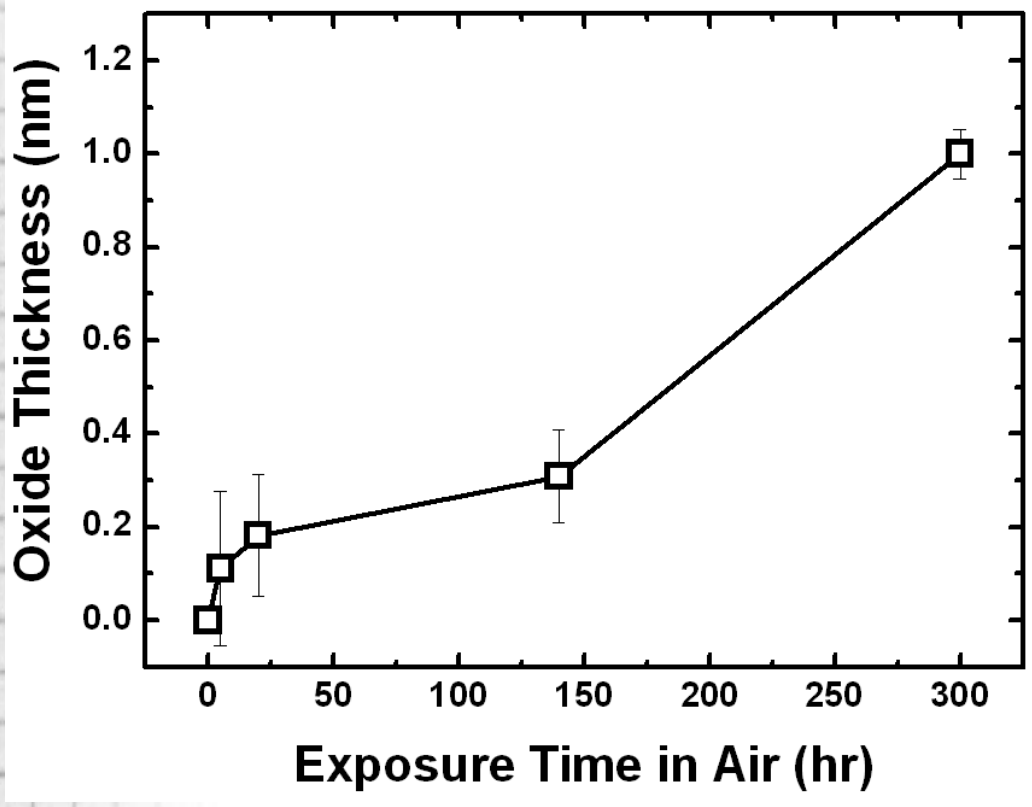
- H-passivation can avoid native oxidation.
- Several way to form H-passivation surface:

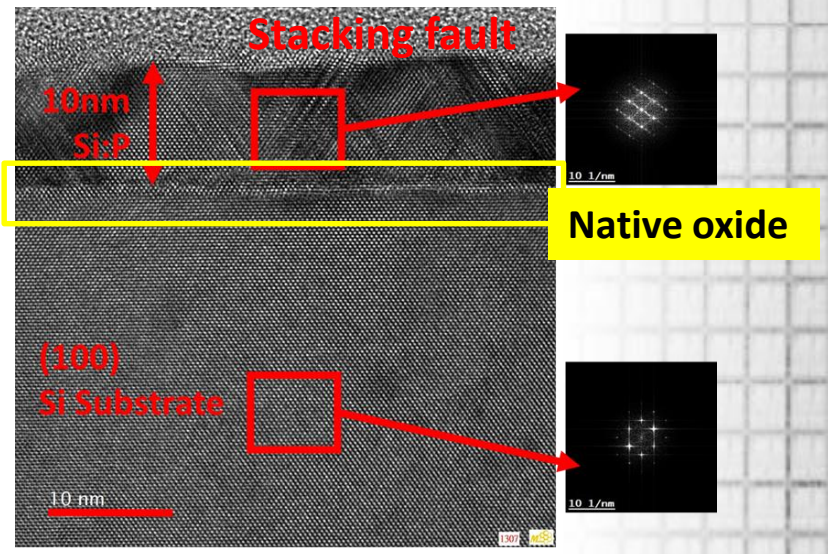
a) HF dip

b) Prebake in H_2

c) H_2 exposure

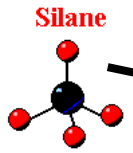
Native Oxide Formation





- Si wafer exposure time in Air ↑ ➔ Native oxide thickness ↑
- Native oxide formation ➔ EPI quality ↓

Growth Mechanism of SiH_4



(a) Silane adsorption

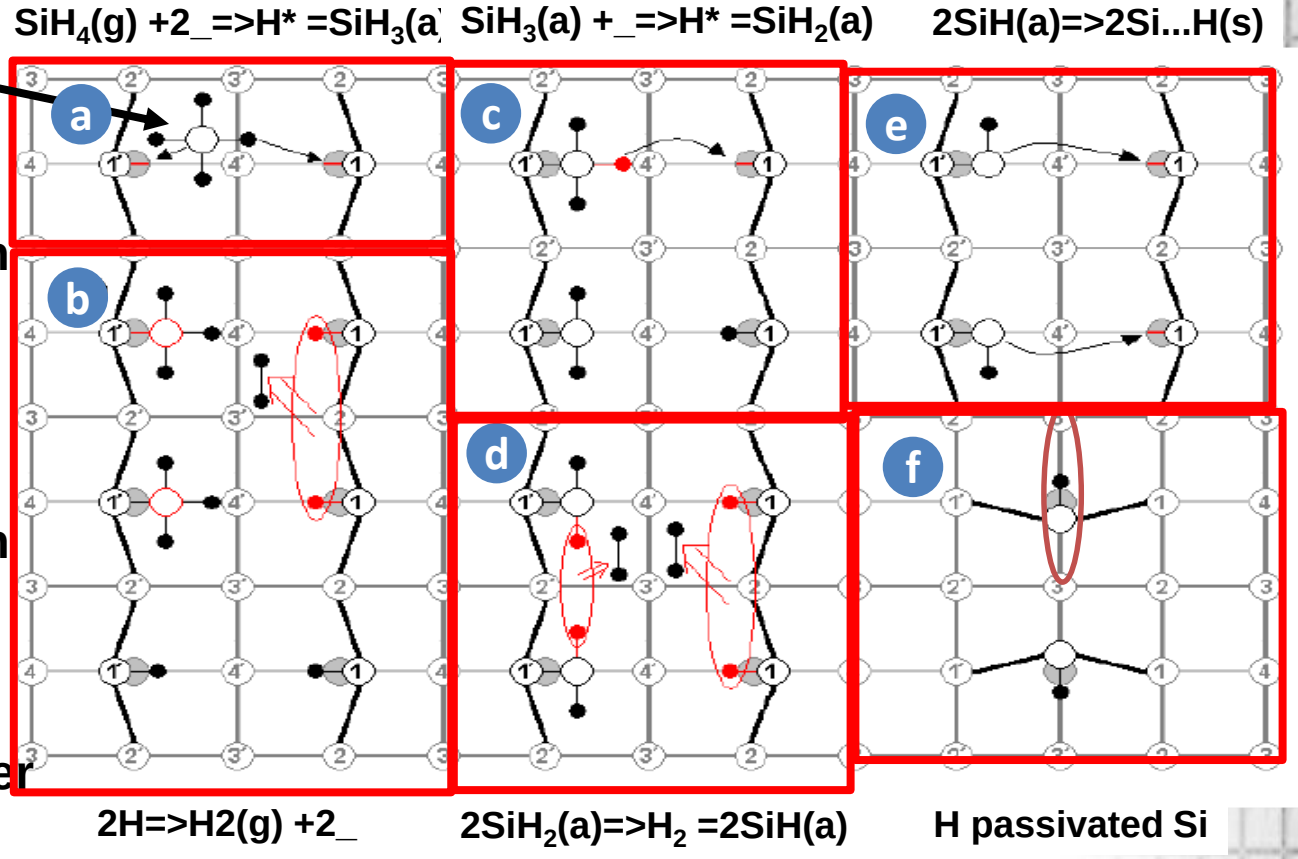
(b) Hydrogen desorption (2_created)

(c) SiH_3 ➔SiH_2 + H*

(d) Hydrogen desorption (2_created) and SiH_2 ➔SiH

(e) SiH(a) bond with other Si

(f) H passivated Si

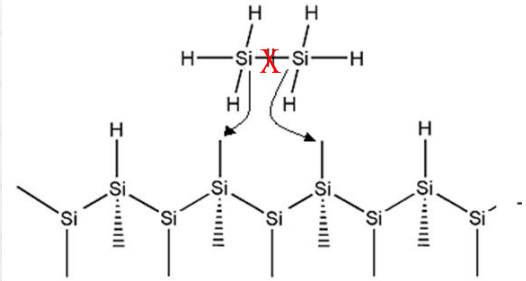


- Adsorption of precursor is a important factor for the epitaxial growth mechanism in CVD system.

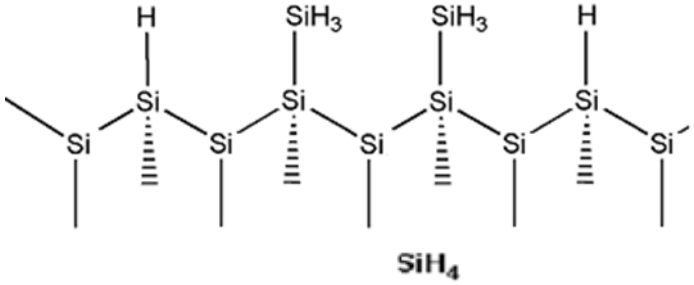
Keith H. Chung-Silicon-Based Epitaxy by Chemical Vapor Deposition Using Novel Precursor Neopentasilane (2010). Part 1

Growth Mechanism of Si_2H_6

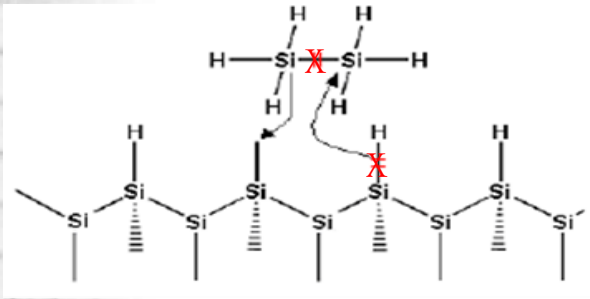
Break Si-Si bond instead of Si-H bond:

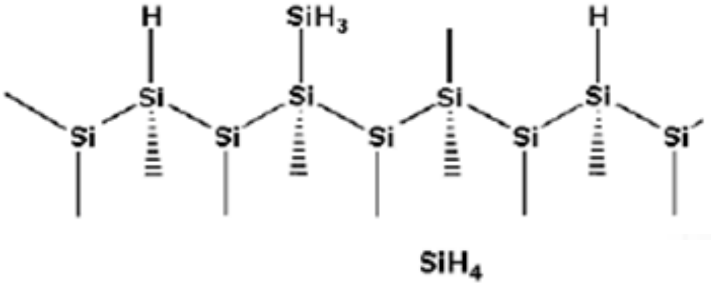


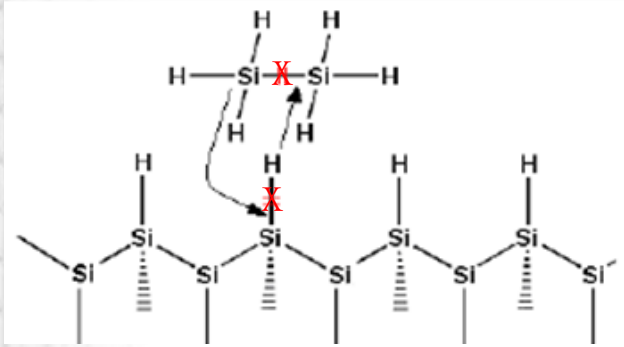
Bond energy:
Si-H 3.31 eV
Si-Si 2.31 eV

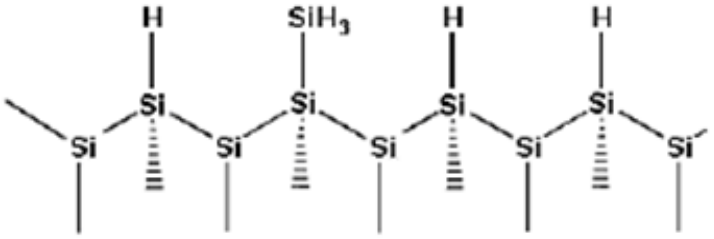


Create open sites:





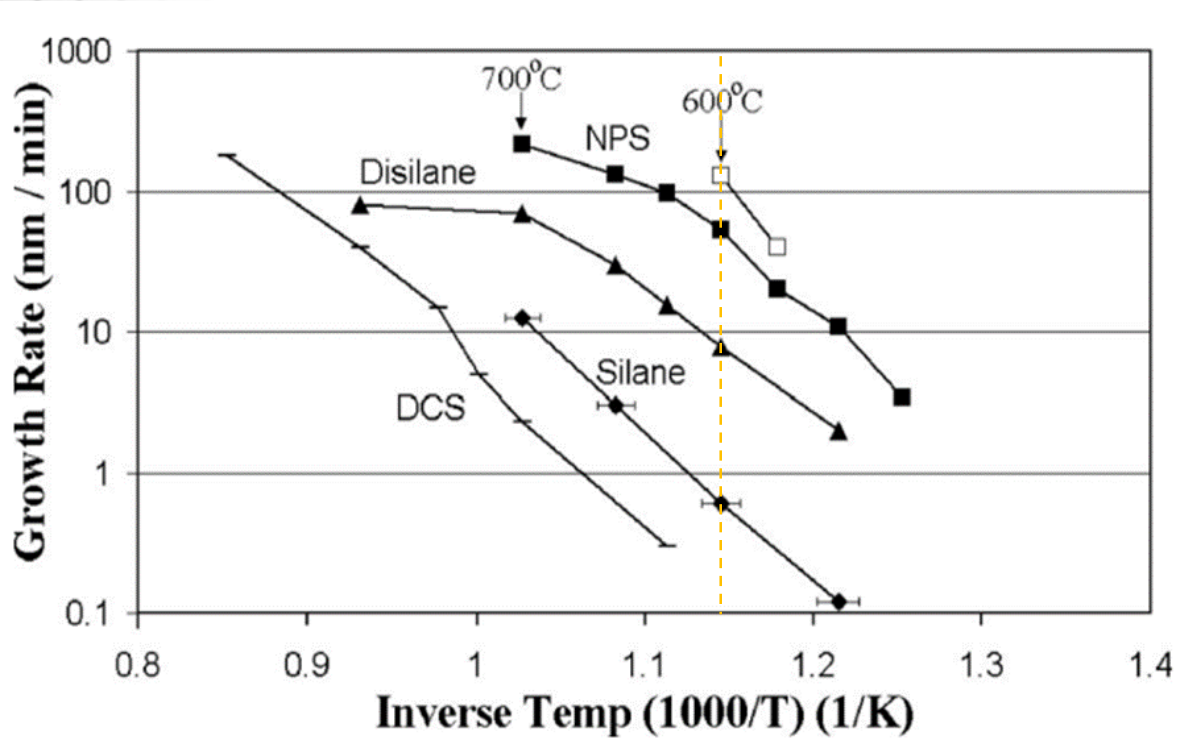


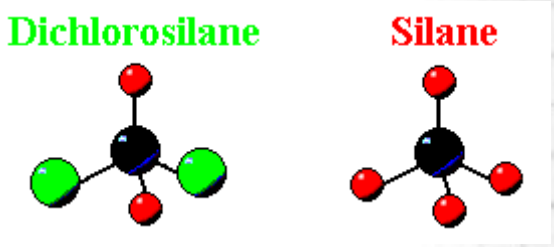


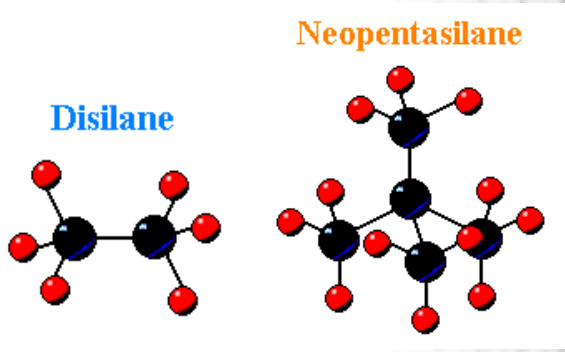
Revised from Si case: K. H. Chung et al., APL, 2008.

- Si_2H_6 can create open sites ➔ Growth rate ↑

Growth Rate of Higher Order Silane



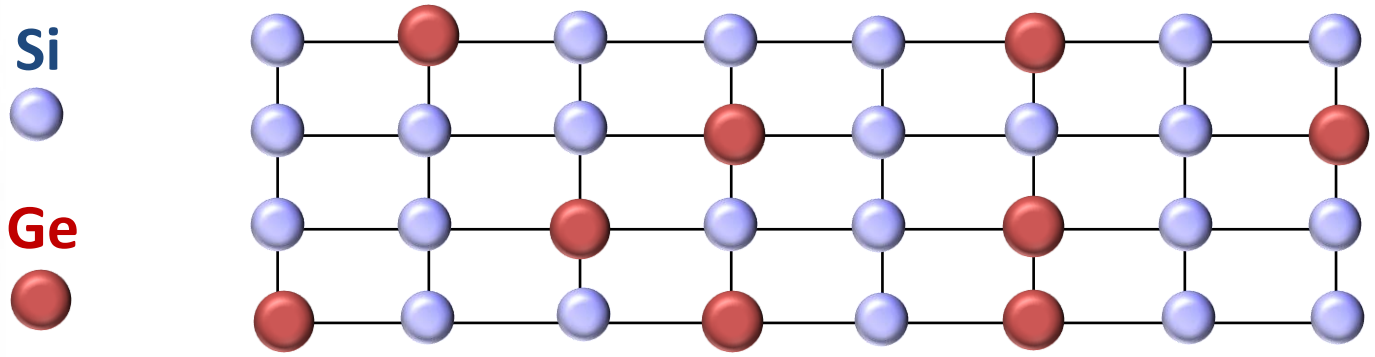




Ref: K. H. Chung et al., Appl. Phys. Lett., 92, 113506 (2008).

- Growth rate (600℃): NPS (Si_5H_{12}) > Disilane (Si_2H_6) > Silane (SiH_4)

$Si_{1-x}Ge_x$



- **Precursor:**

  Si: Silane(SiH_4), High order silane (Si_2H_6, Si_3H_8…),

  Dichlorosilane ($SI_2H_2Cl_2$).

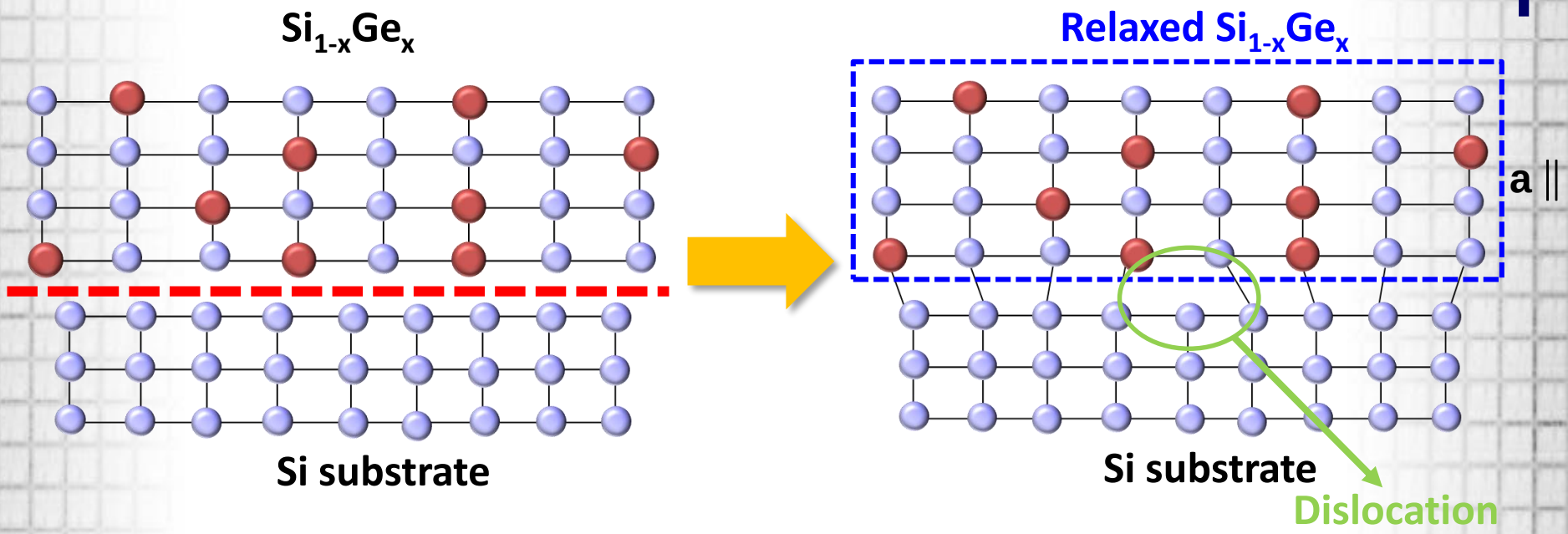
  Ge: Germane (GeH_4), Digermane (Ge_2H_6)

- **Lattice constant:**

  a_{Si} = 0.5431 nm

  a_{Ge} = 0.5658nm, Ge is larger by 4.2% than the Si lattice constant.

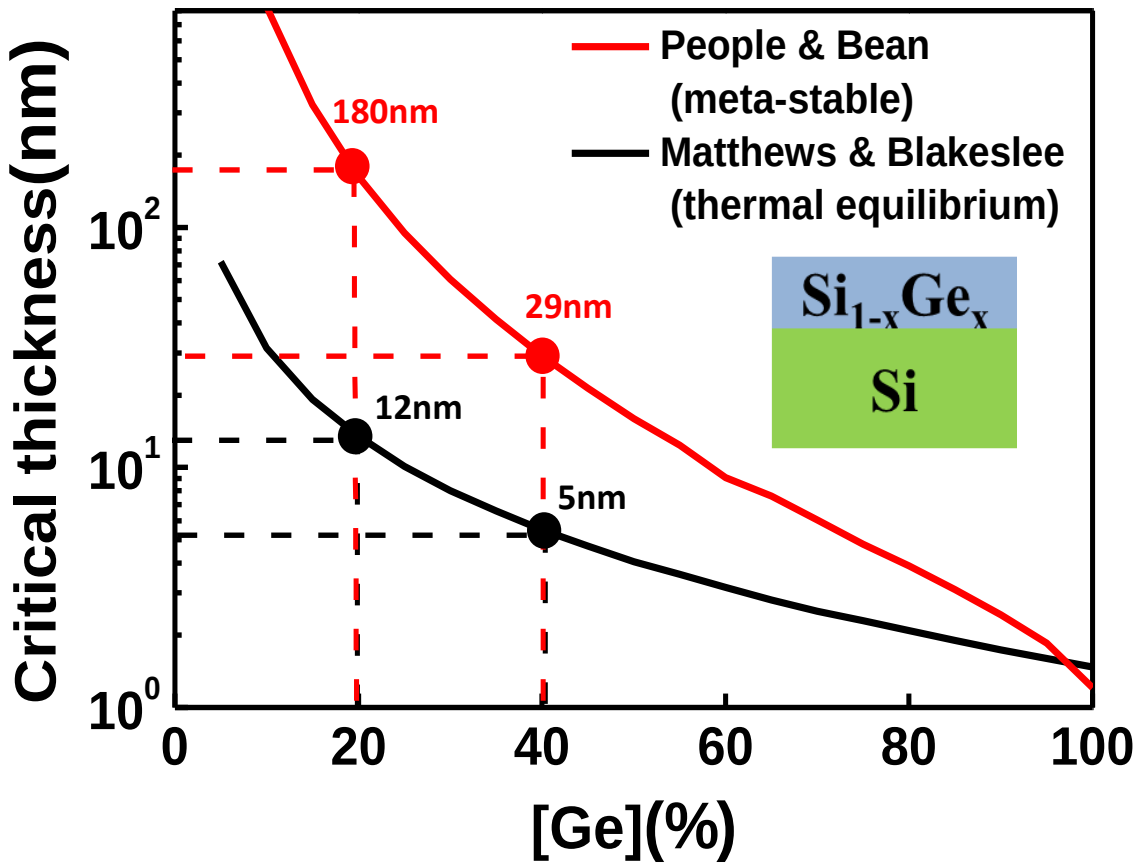
Relaxed SiGe



- Epi thickness > critical thickness ➔ Relaxed $Si_{1-x}Ge_x$
- Relaxed $Si_{1-x}Ge_x$ lattice constant:

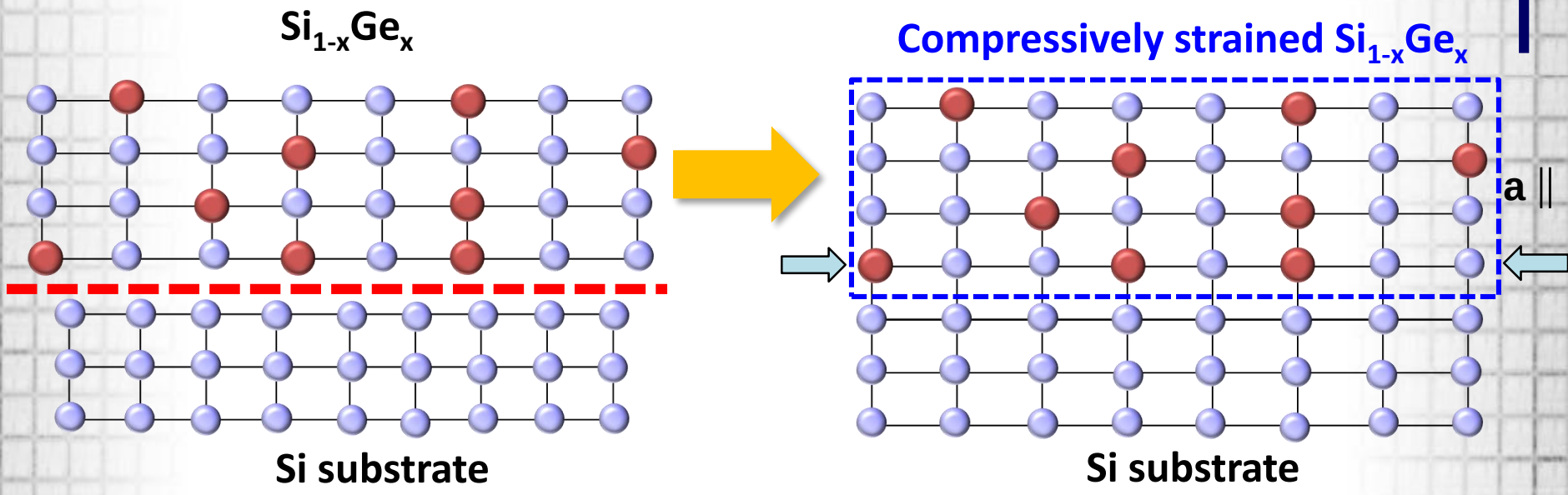
  $a_{\parallel} = a_{Si1-xGex}$
- Strained SiGe: $a_{\parallel} = a_{si}$

[Ge]% vs Critical thickness



- [Ge]% ↑ > critical thickness ↓
- Low growth temperature ➔ Meta-stable
- High growth temperature➔ Thermal equilibrium

Compressively strained SiGe

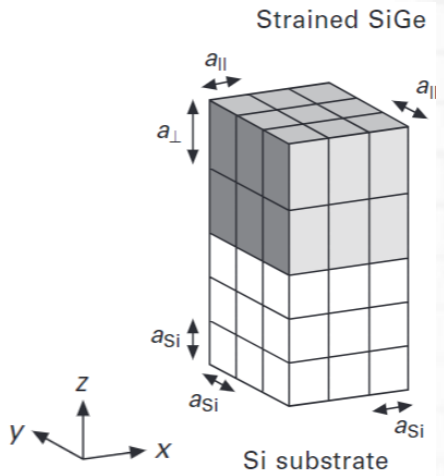


- **Compressively strained SiGe lattice constant:**

  $a \parallel = a_{Si} < a_{Si1-xGex}$

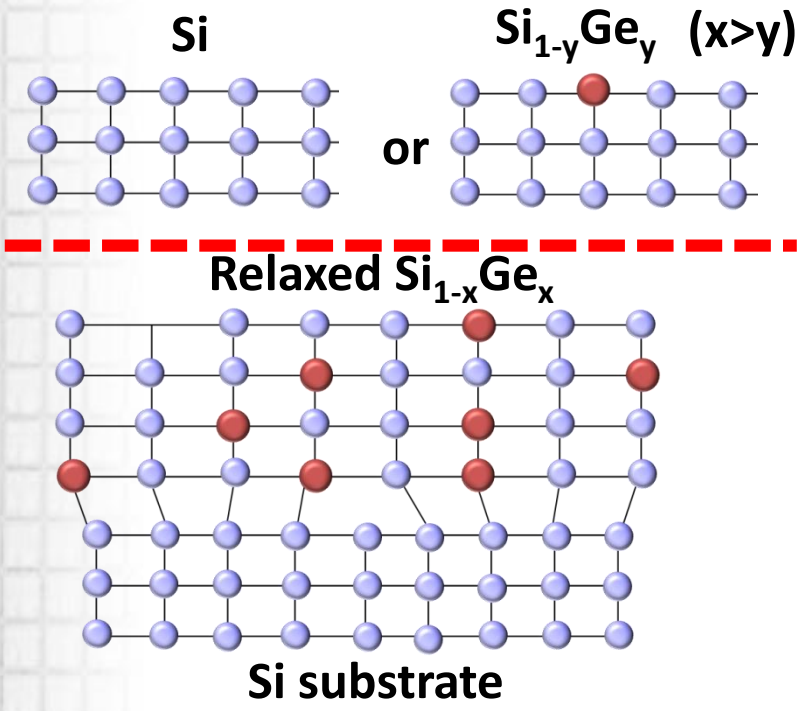
  $a \perp > a_{Si1-xGex}$

- **Poisson ratio**



Woodhead Publishing Limited, 2011

Tensily strained Si & SiGe



- **Tensily strained Si lattice constant:**

  $a_{\parallel} = a_{Si1-xGex} > a_{Si}$

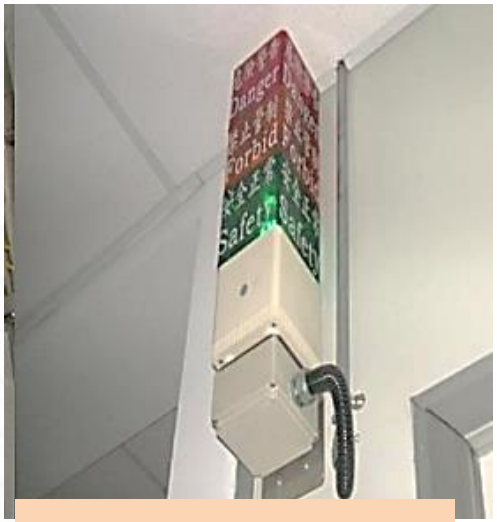
- **Tensily strained $Si_{1-y}Ge_y$ lattice constant:**

  $a_{\parallel} = a_{Si1-xGex} > a_{Si1-yGey}$ (x>y)

$SnCl_4$ Gas Cabinet and cylinder

Ge_2H_6 Gas Cabinet and cylinder

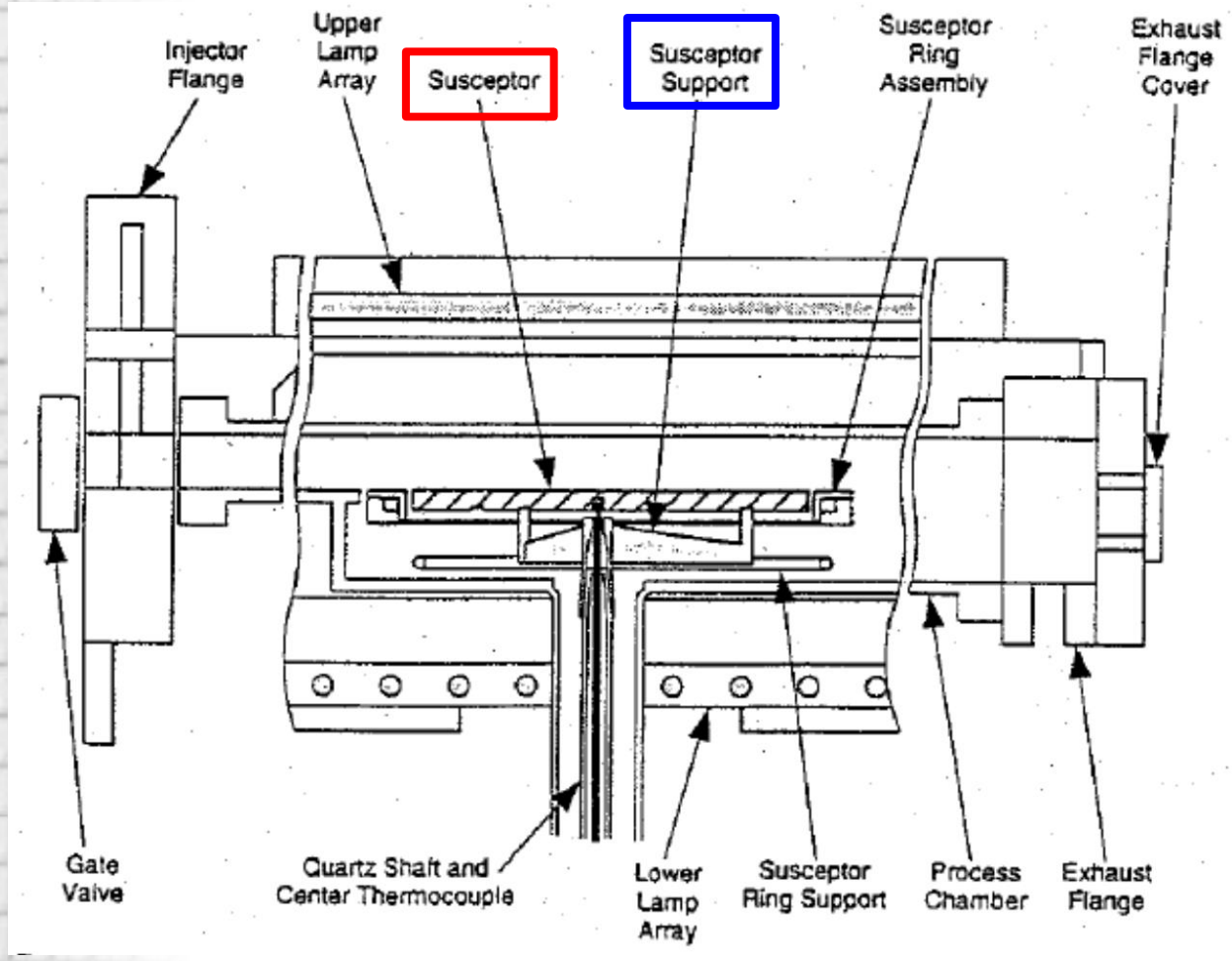
Gas Detector and Local Scrubber



Gas Detector

Local Scrubber

ASM Process Chamber

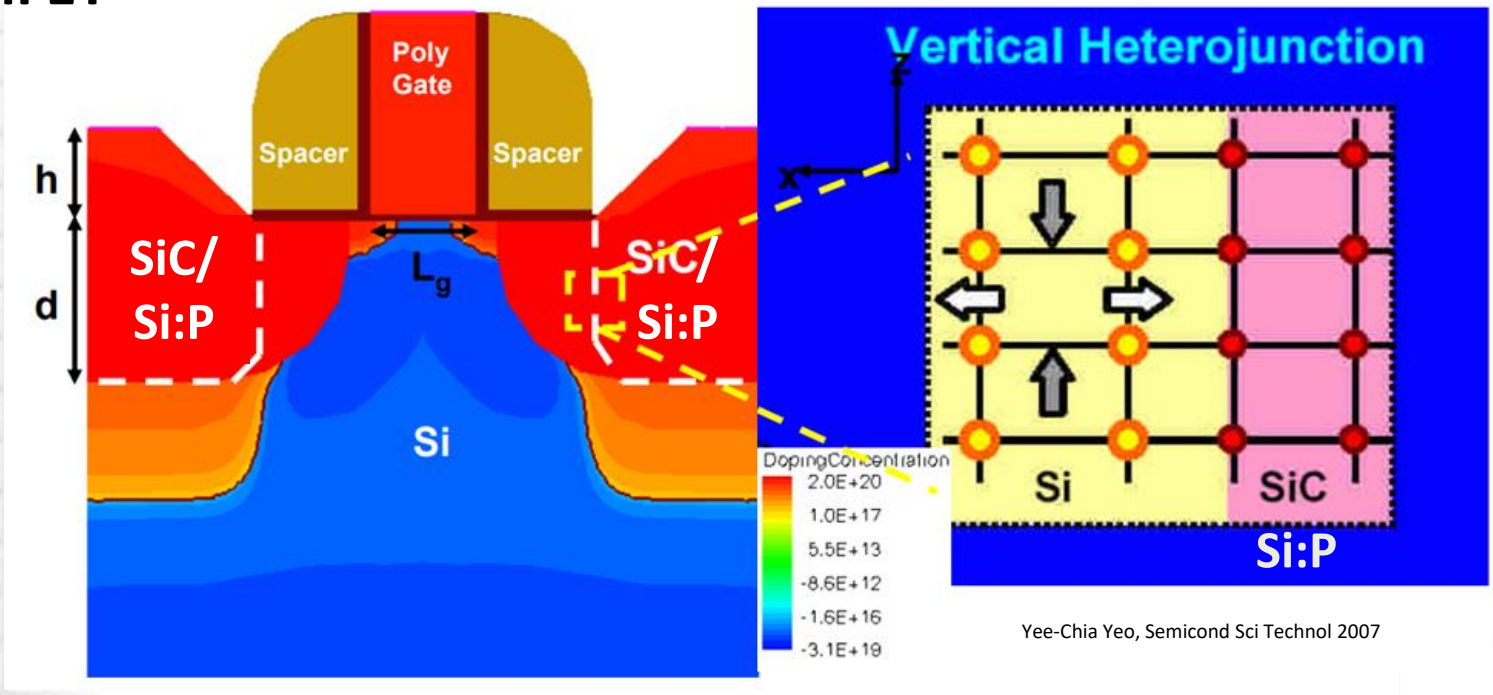


Susceptor (SiC coating)

Susceptor Support (Quartz)

Tensile Strain Technologies (S/D stressor)

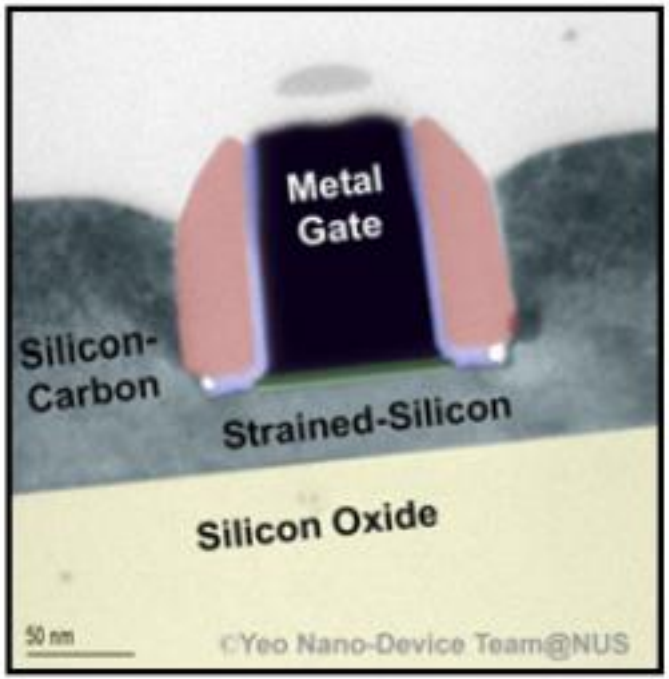
nFET



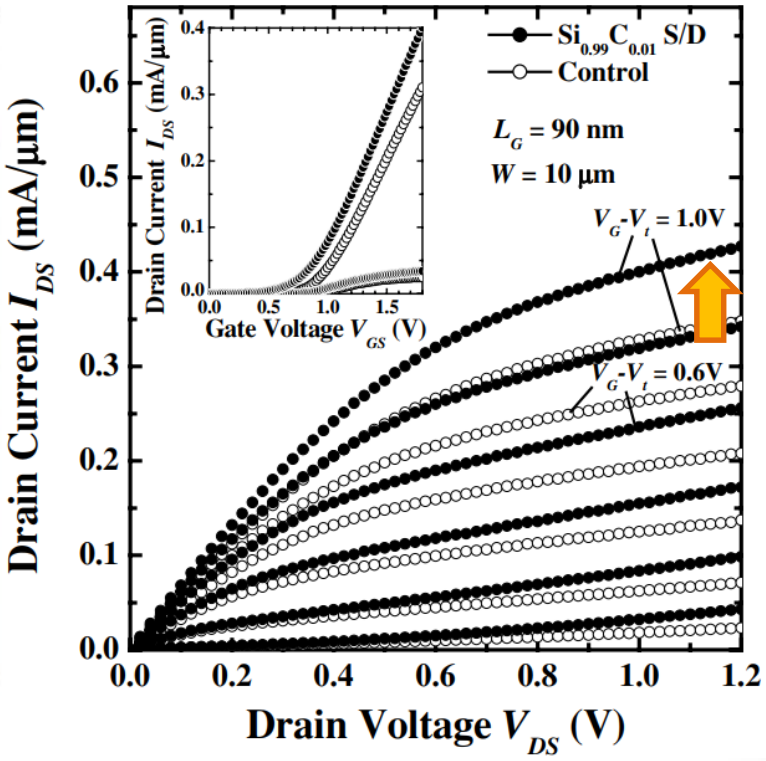
Yee-Chia Yeo, Semicond Sci Technol 2007

- **Si:P /SiC for engineering the lattice strain in the transistor channel region to improve electron mobility in nFET.**

Tensile Strain Technologies (S/D stressor)

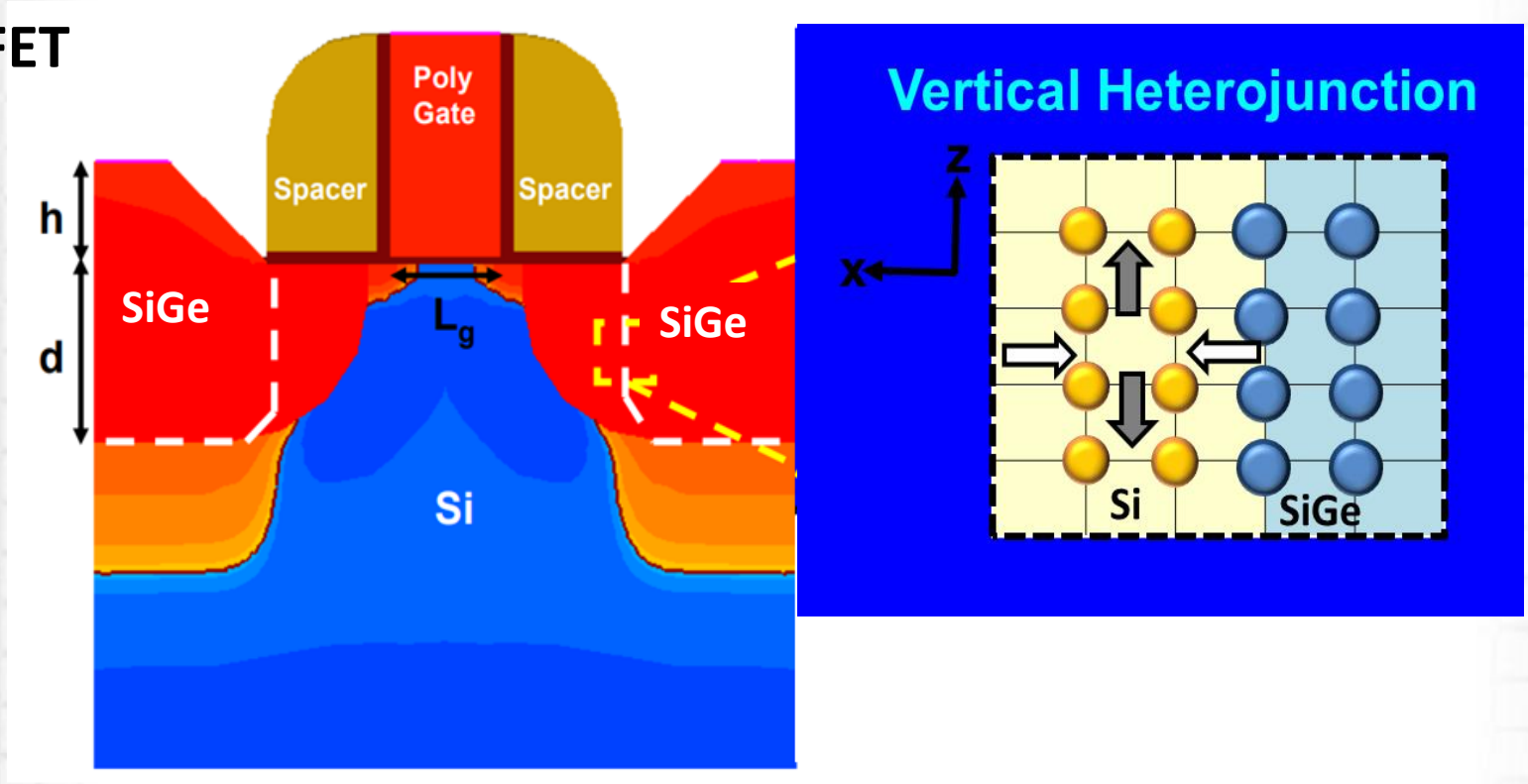


Yee-Chia Yeo, Semicond Sci Technol 2007



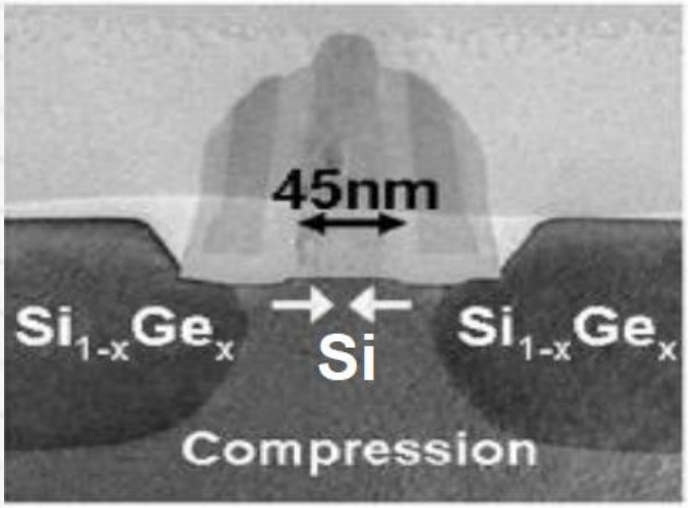
- **Tensile strained Si on SOI nFET with SiC S/D, showing a 25% I_{Dsat} enhancement over a control transistor with Si S/D.**

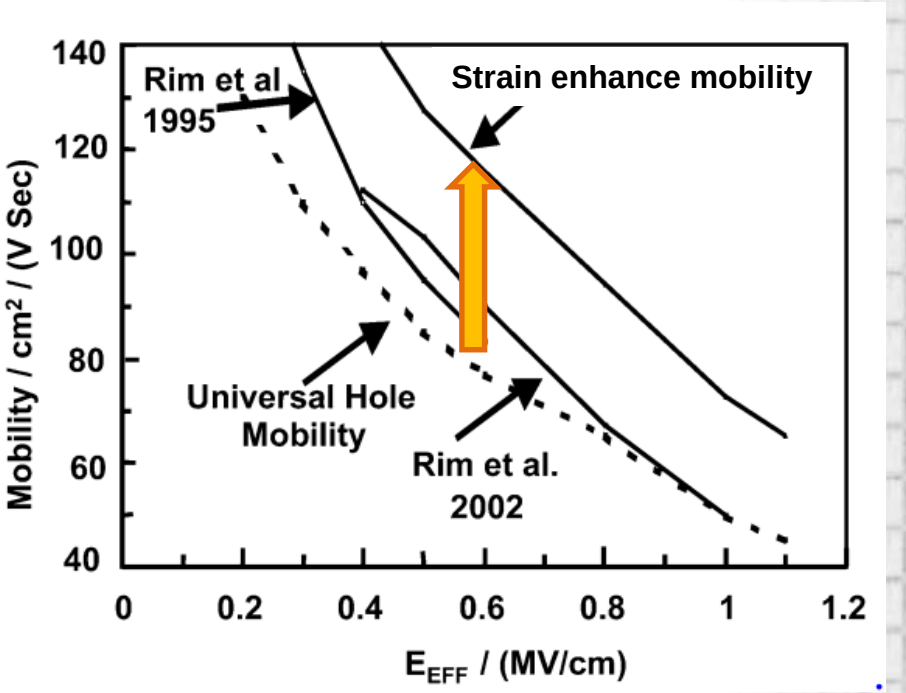
Compressive Strain Technologies (S/D stressor)

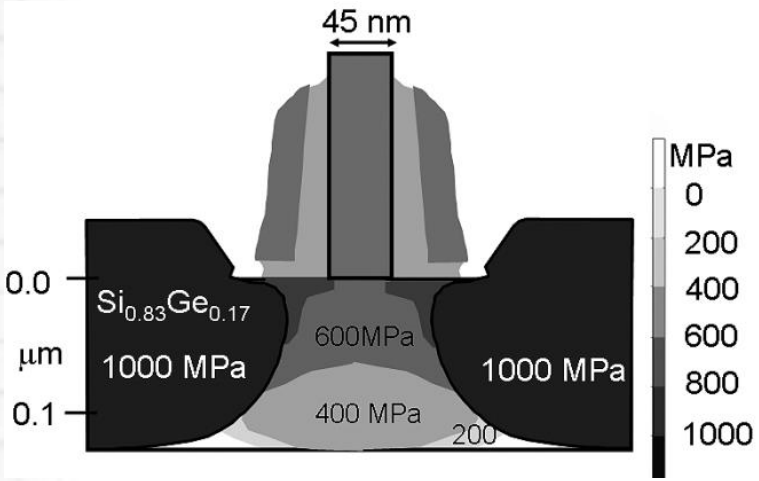


- **SiGe for engineering the lattice strain in the transistor channel region to improve hole mobility in pFET.**

Compressive Strain for pMOSFET (S/D stressor)



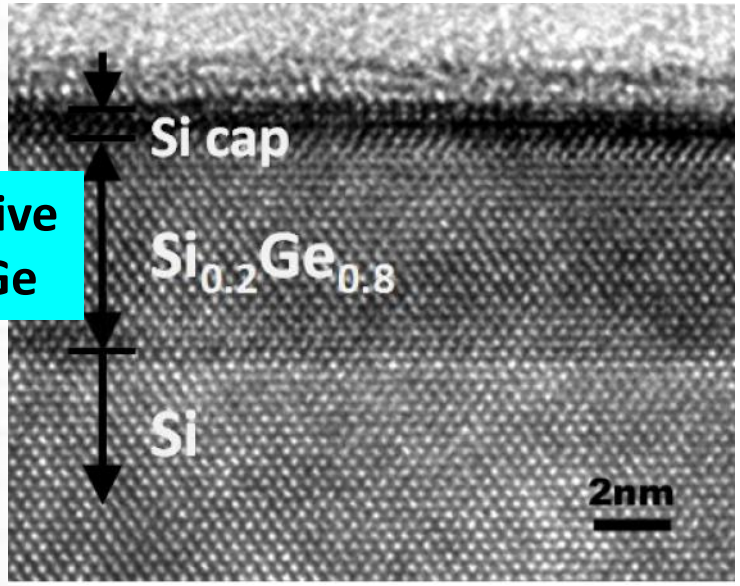


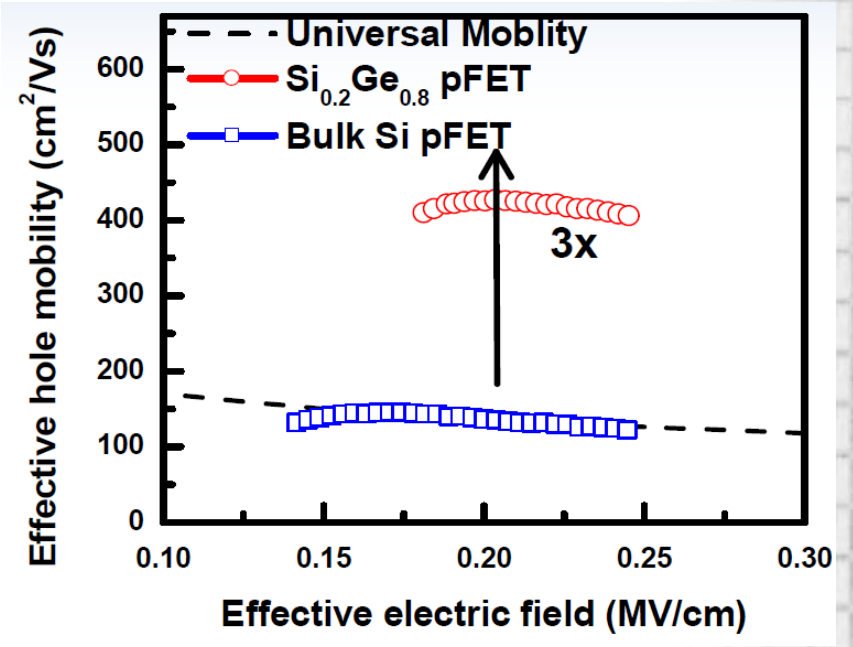


- **Uniaxial compressive strain introduced by the $Si_{1-x}Ge_x$ in the S/D of the pMOSFET increases the hole mobility for the 45-nm gate length transistor by 50%.**

Compressive Strain technologies for pFET

Compressive Strain SiGe



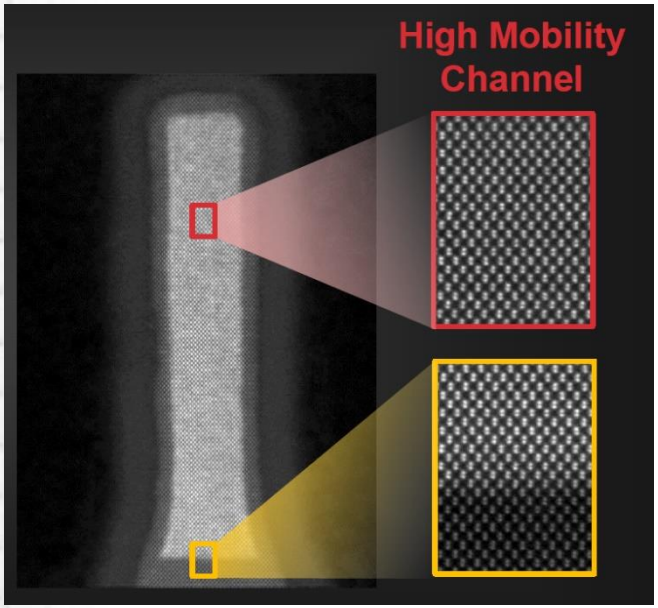


C.-Y. Peng et al. and C. W. Liu, Appl. Phys. Lett. 90, 012114, 2007

- The Si cap layer is grown on the top of SiGe layer to passivate and smoothen the surface. (Dit ↓)
- The ~3x hole mobility enhancement for the SiGe pFET is obtained compared with bulk Si pEFT.

tsmc 2021 ISSCC (5nm)

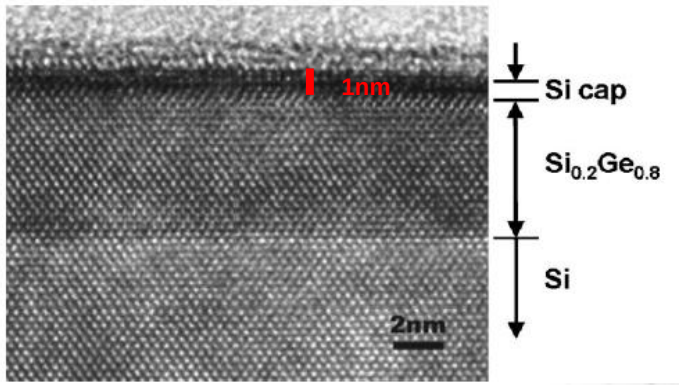
tsmc 2021 ISSCC (5nm)

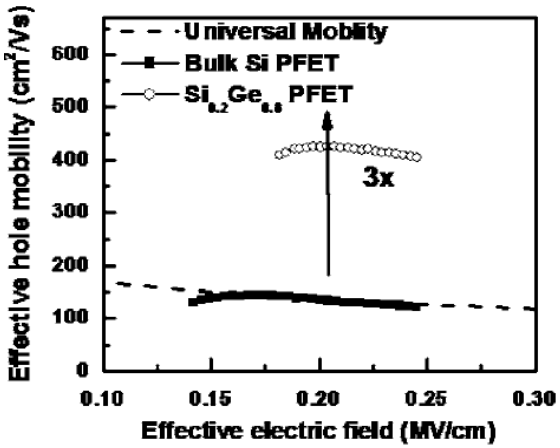


13 years

(2007-2020)

NTU 2007 APL



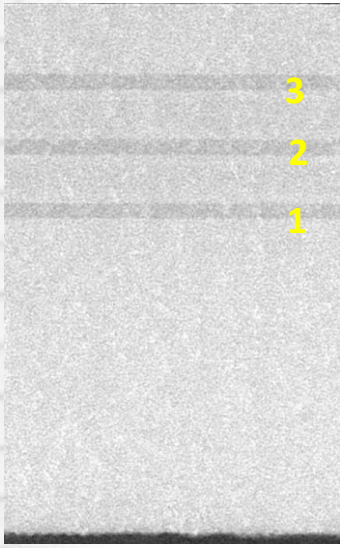


The 5nm technology node of tsmc have high mobility channel (*Mark Liu, Plenary Session 1.1, ISSCC 2021)*

(C.-Y. Peng et al. and C. W. Liu, Appl. Phys. Lett. 90, 012114, 2007)

EPI for Highly stacked nanosheet

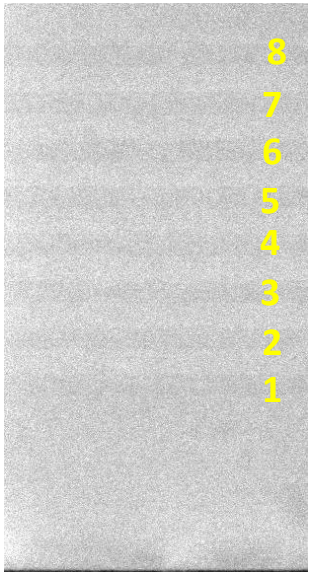
NTU 2021
3 stacked GeSi



NTU 3 stacked TreeFET

Chien-Te Tu et al. and C. W. Liu, to be submitted to Electron Device Letters.

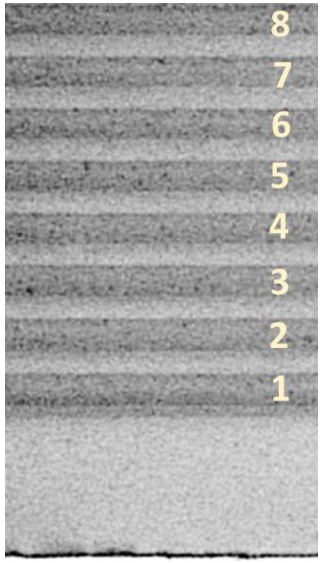
NTU 2021 VLSI
8 stacked GeSi



NTU 8 stacked nanosheets

Yi-Chun Liu et al. and C. W. Liu, Symposium on VLSI Technology (VLSI-Technology), 2021.

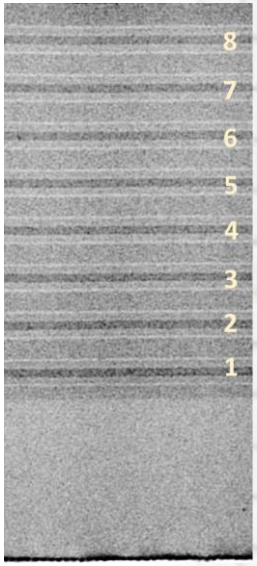
NTU 2021 IEDM
8 stacked GeSn



NTU 8 stacked thick nanosheets

Chung-En Tsai et al. and C. W. Liu, accepted by International Electron Devices Meeting (IEDM), 2021.

NTU 2021 IEDM
8 stacked GeSn

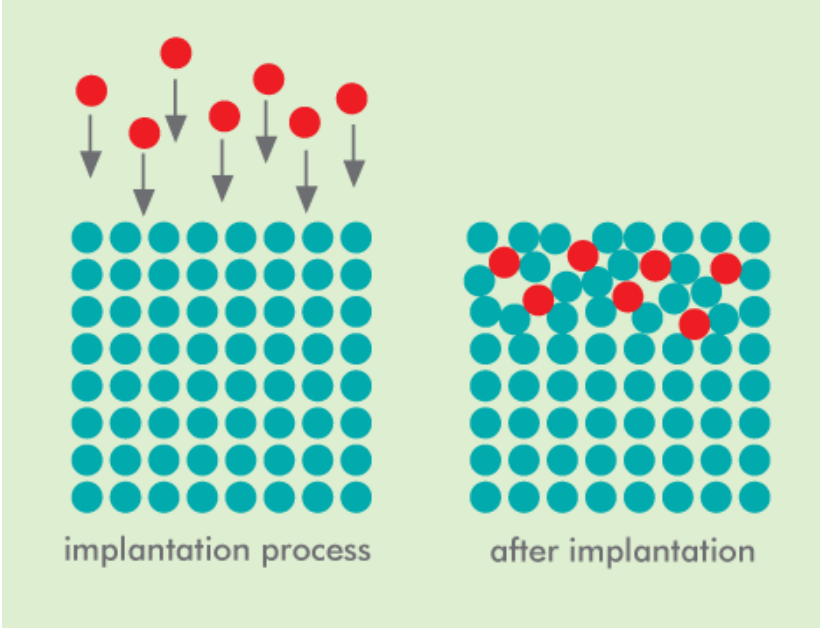


NTU 8 stacked ultrathin bodies

Chung-En Tsai et al. and C. W. Liu, accepted by International Electron Devices Meeting (IEDM), 2021.

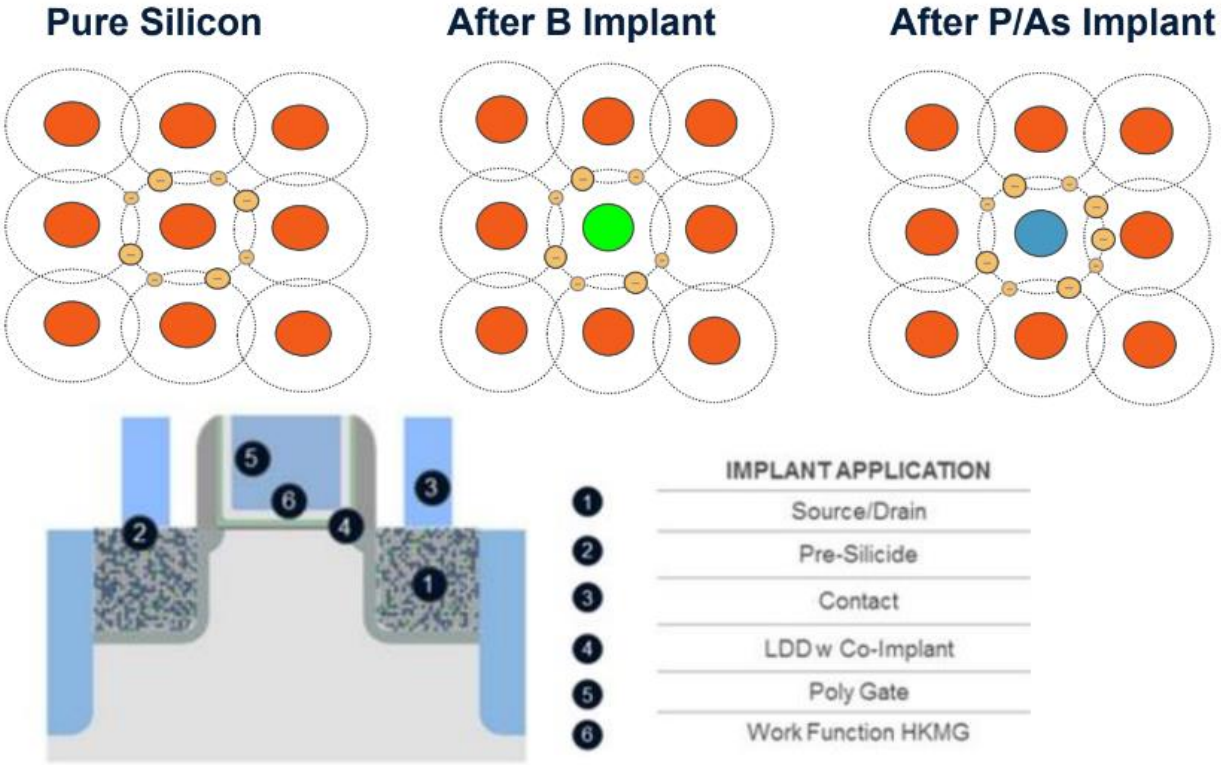
Ion Implantation

- Add impurities so that it conducts current and has conductive properties



Ref. :
https://www.google.com/url?sa=i&url=https%3A%2F%2Fmatenggroup.wordpress.com%2Fion-implantation

Ion Implanter Process



Ref. :
http://www.appliedmaterials.com/files/pdf_documents/Applied%20Varian%20VIISta%20Trident%20Technical%20Briefing_060512_0.pdf

Semiconductor manufacturing process

01 Wafer manufacturing

02 Oxidation/ALD

03 Photolithography /EUV

04 Etch

05 Deposition (PVD/Epi) & Ion implantation

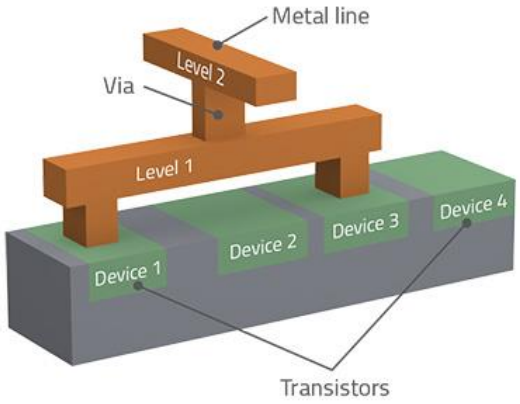
06 Interconnect/CMP

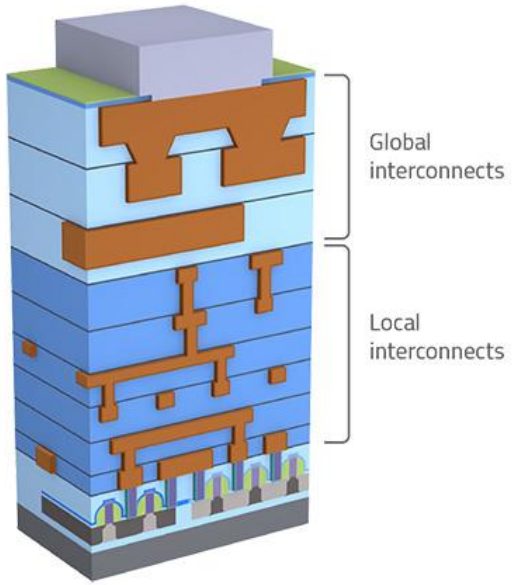
07 Testing

08 Packaging

Interconnect

- Create a path for electricity to pass through by depositing a thin metal film using materials such as aluminum, copper, titanium, or tungsten

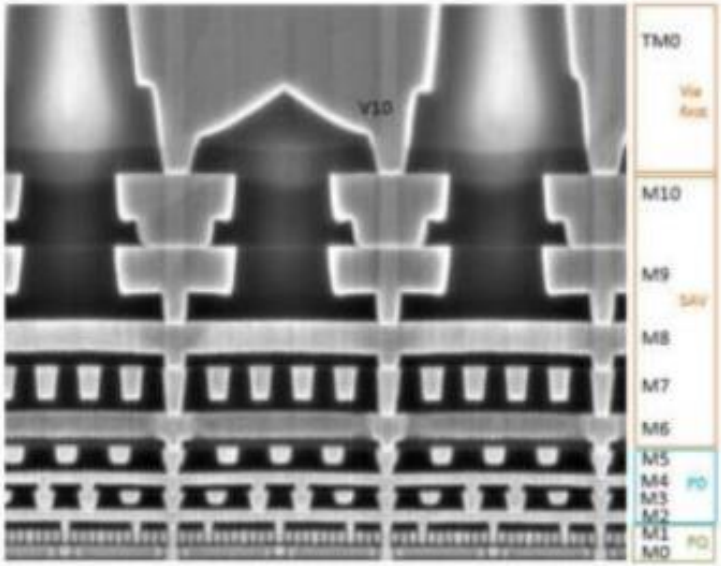




Ref. : https://www.google.com/url?sa=i&url=https%3A%2F%2Fsemiengineering.com%2Fall-about-interconnects

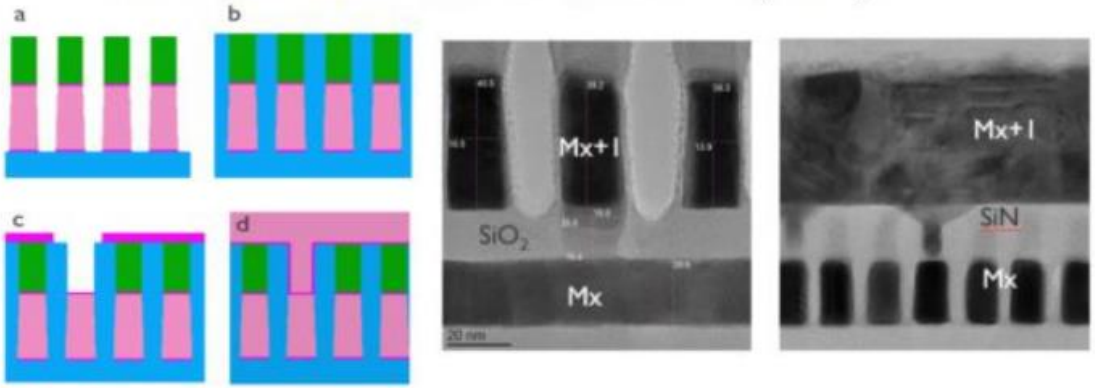
Metal Interconnects

Co interconnects (intel 10nm)



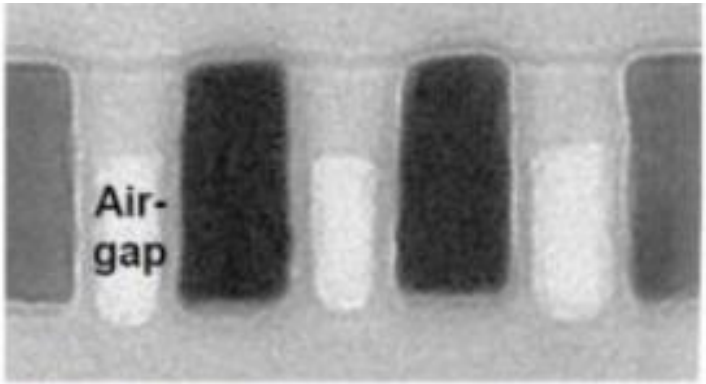
Ref. : A. Yeoh et al. (Intel), IITC 2018

Ru semi-damascene interconnects (Imec)



Ref. : G. Murdoch et al. (Imec), VLSI 2022

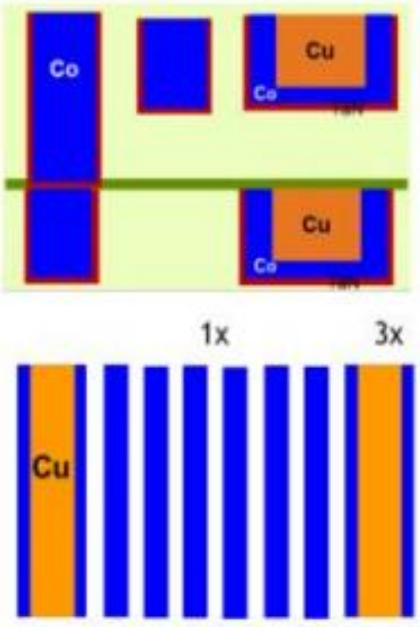
Subtractive metal + Airgap (TSMC)



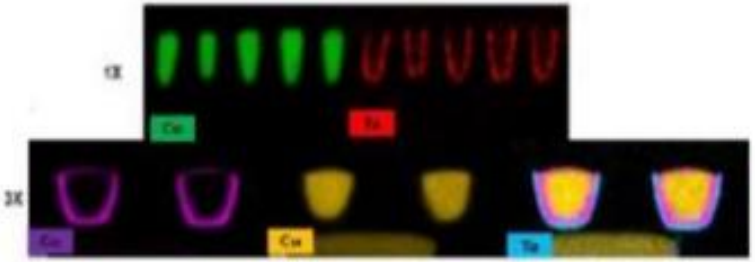
Ref. : Y. Mii et al. (TSMC), VLSI 2022

Composite Interconnects

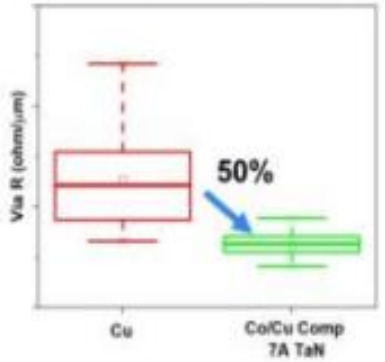
Co/Cu composite interconnects



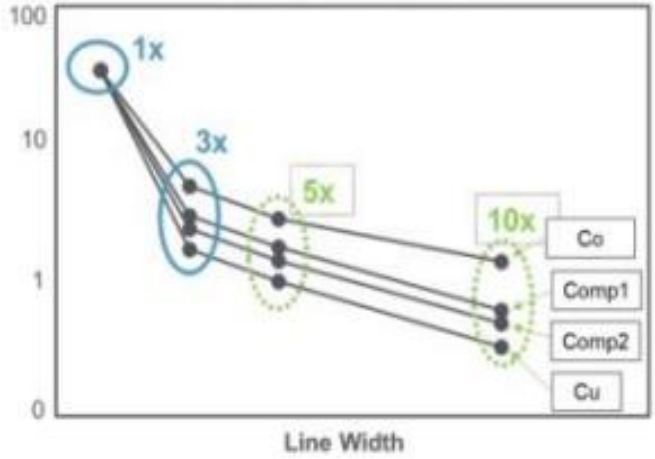
EDX mapping on composite interconnects



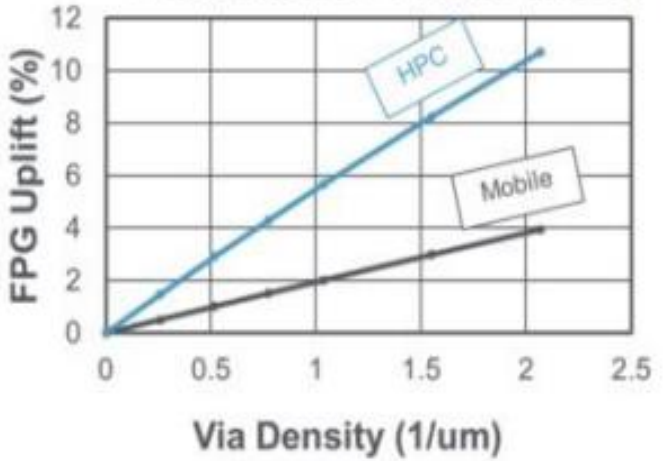
Via resistance



Line resistance



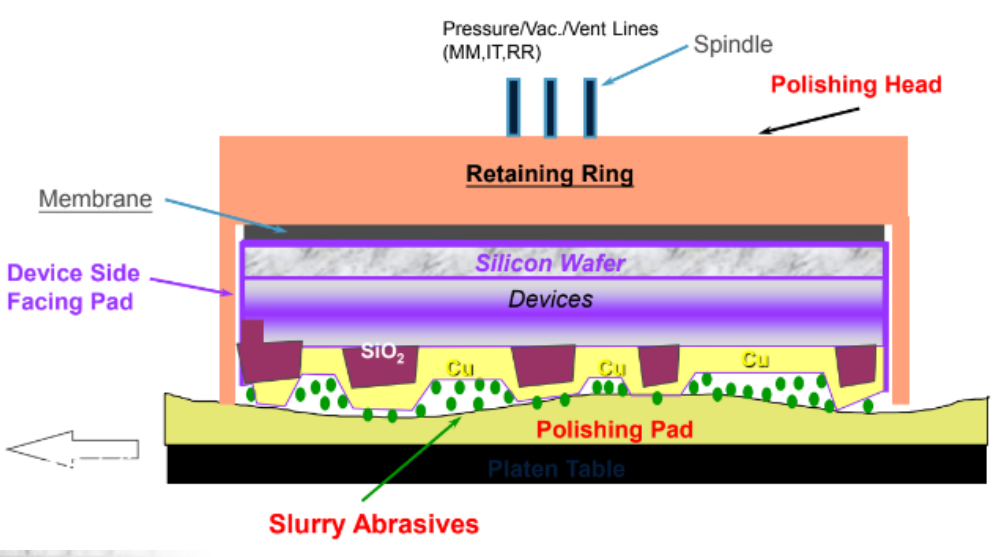
Performance enhancement

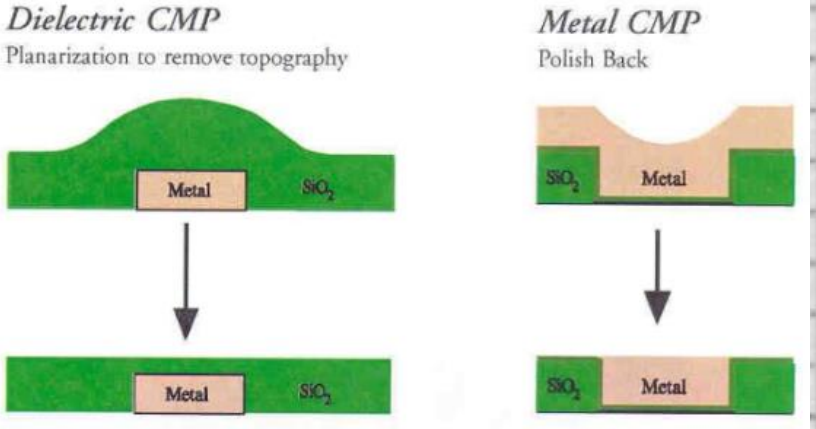


Ref. : T. Nogami et al. (IBM), IITC 2017

Ref. : P. Bhosale et al. (IBM), VLSI 2020

CMP

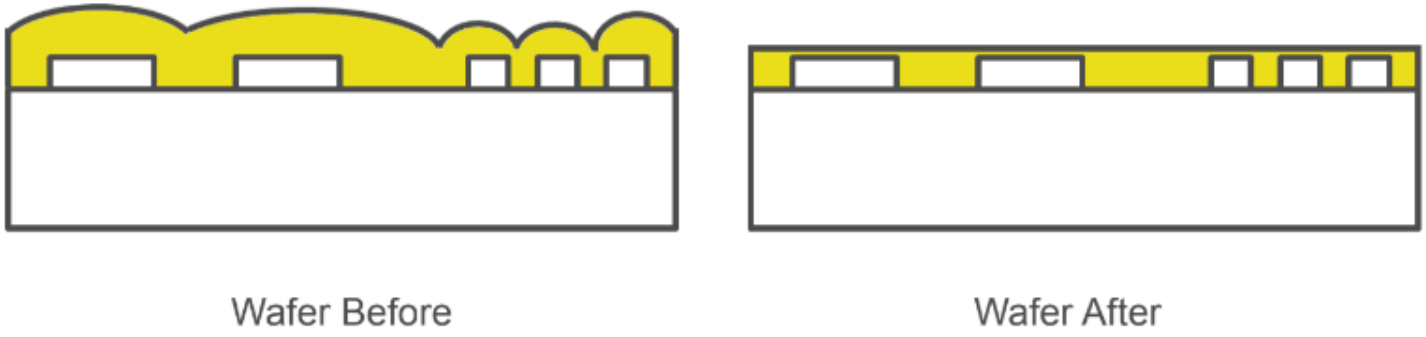




Ref. : AMAT, 2022

- CMP = Chemical Mechanical Planarization/Polishing
- Planarization : Removal of material through combined action of chemical and mechanical forces
- Polishing : Smoothing of surfaces

Two Primary Reasons for CMP

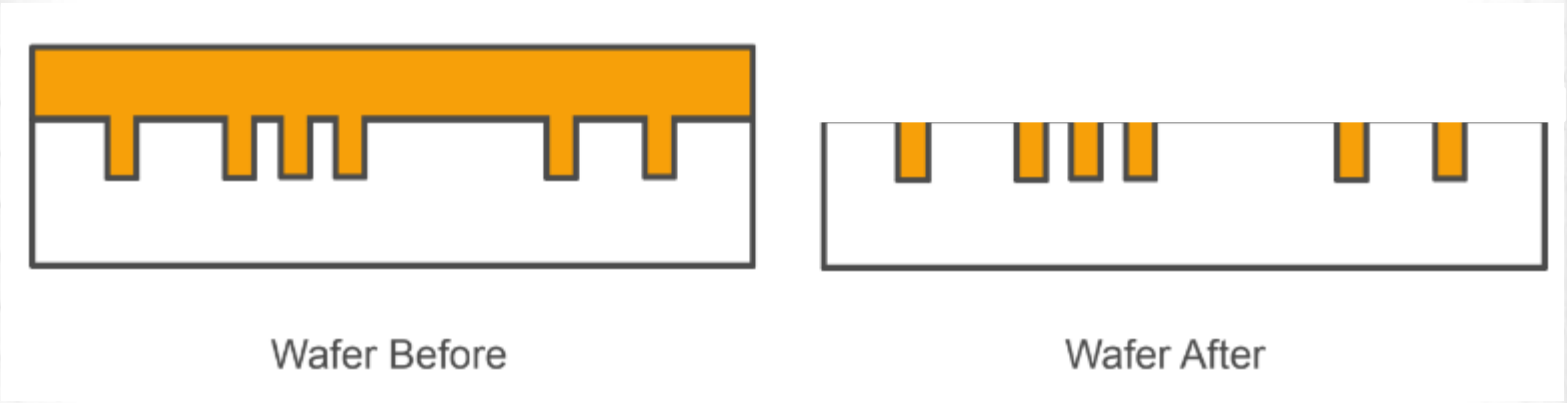


1. Polish Out High Spots :

Ref. : AMAT, 2022

As layers are added to the surface of a wafer, the surface becomes uneven. In the lithography stage, we print a pattern on the wafer on a microscopic scale. When printing an image like this, the lenses have a very shallow depth of focus. If the surface is not flat enough, the image is distorted. Using CMP, we can polish out the high spots and make the wafer flat again.

Two Primary Reasons for CMP



Ref. : AMAT, 2022

2. Remove Material to Expose the Layer Below :

The second reason to remove specific amounts of material is to expose the layer below, as done in copper and tungsten polish. A layer of metal is put down on the wafer to fill lines and vias (feedthroughs). It is not possible to fill only the lines and vias. Instead, the entire surface of the wafer is covered. The excess is polished to expose the layer underneath, but leaves the lines and vias filled.

Semiconductor manufacturing process

01 Wafer manufacturing

02 Oxidation/ALD

03 Photolithography /EUV

04 Etch

05 Deposition (PVD/Epi) & Ion implantation

06 Interconnect/CMP

07 Testing

08 Packaging

Testing

- Electrical Die Sorting (EDS) is the process of testing electrical characteristics to make sure each individual chip has reached the desired quality level
- Yield :
  - Total yield : $Y_T = Y_W \times Y_D \times Y_C$
  - Wafer yield : $Y_W = \frac{Wafers_{good}}{Wafers_{good} + Wafersbad}$
  - Die yield : $Y_D = \frac{Dies_{good}}{Dies_{good} + Diesbad}$
  - Packaging yield : $Y_C = \frac{Chipsgood}{Chipsgood + Chipsbad}$

Semiconductor manufacturing process

01 Wafer manufacturing

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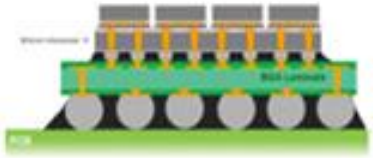
06 Interconnect/CMP

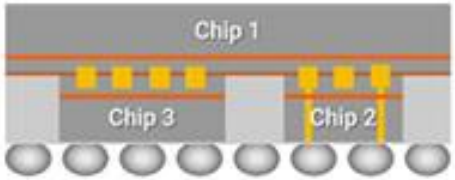
07 Testing

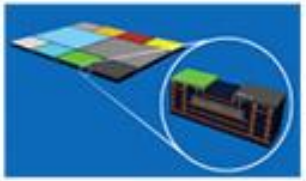
08 Packaging/3DIC

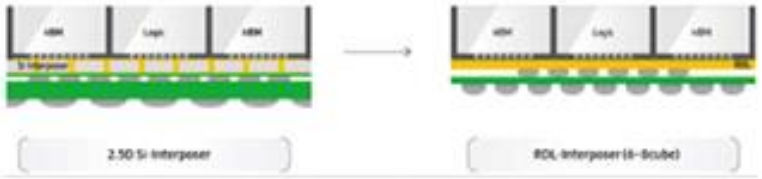
台積電、英特爾、三星積極投入3D封裝技術

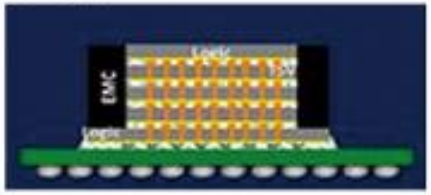
業者	2.5D封裝技術		3D封裝技術
台積電	CoWoS	InFO	SoIC
英特爾	EMIB		Foveros
三星	I-Cube		3D SiP





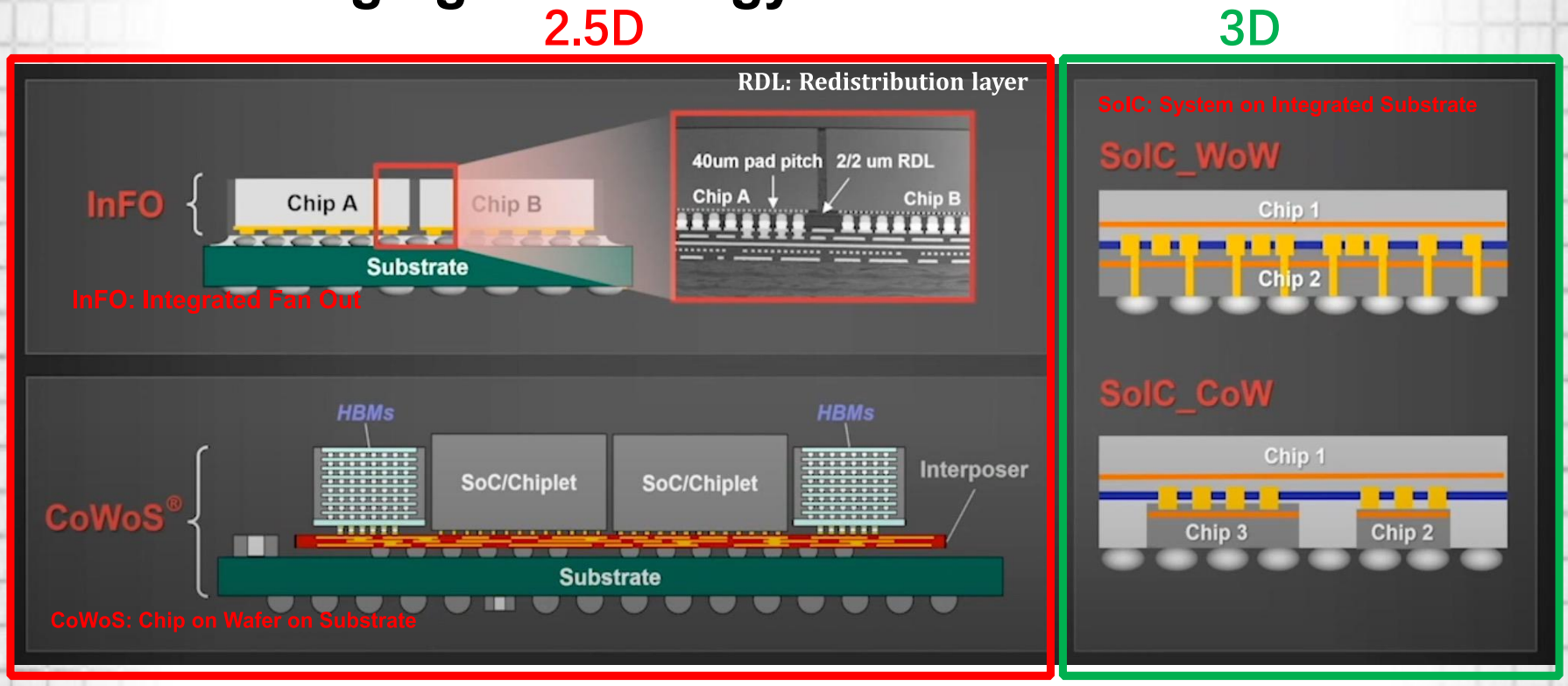






資料來源：DIGITIMES Research整理，2020/6

TSMC's Packaging Technology

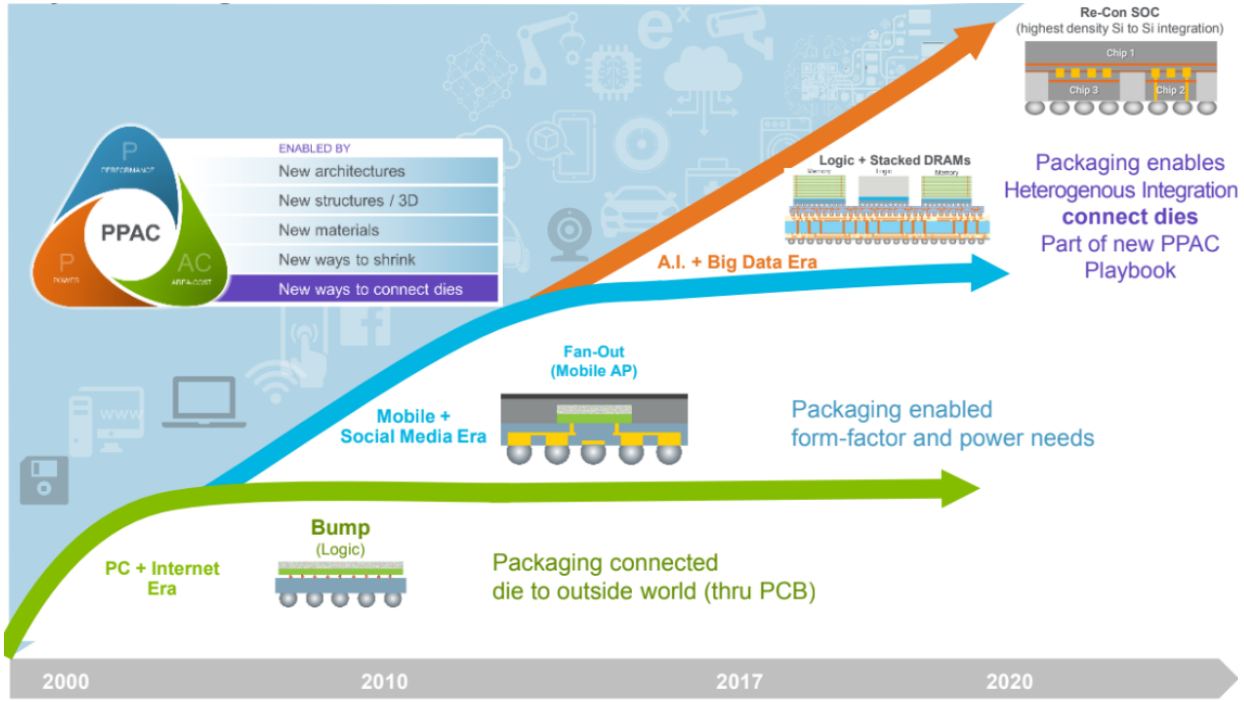


Ref: Mark Liu, Plenary Session 1.1, ISSCC 2021.

- 2.5D (InFO and CoWoS): connection through RDL or interposer
  - Cheap and flexible to have large product portfolio
- 3D (SoIC): directly connection through SoIC bonding (< 10μm pitch)
  - Expensive to further improve system performance

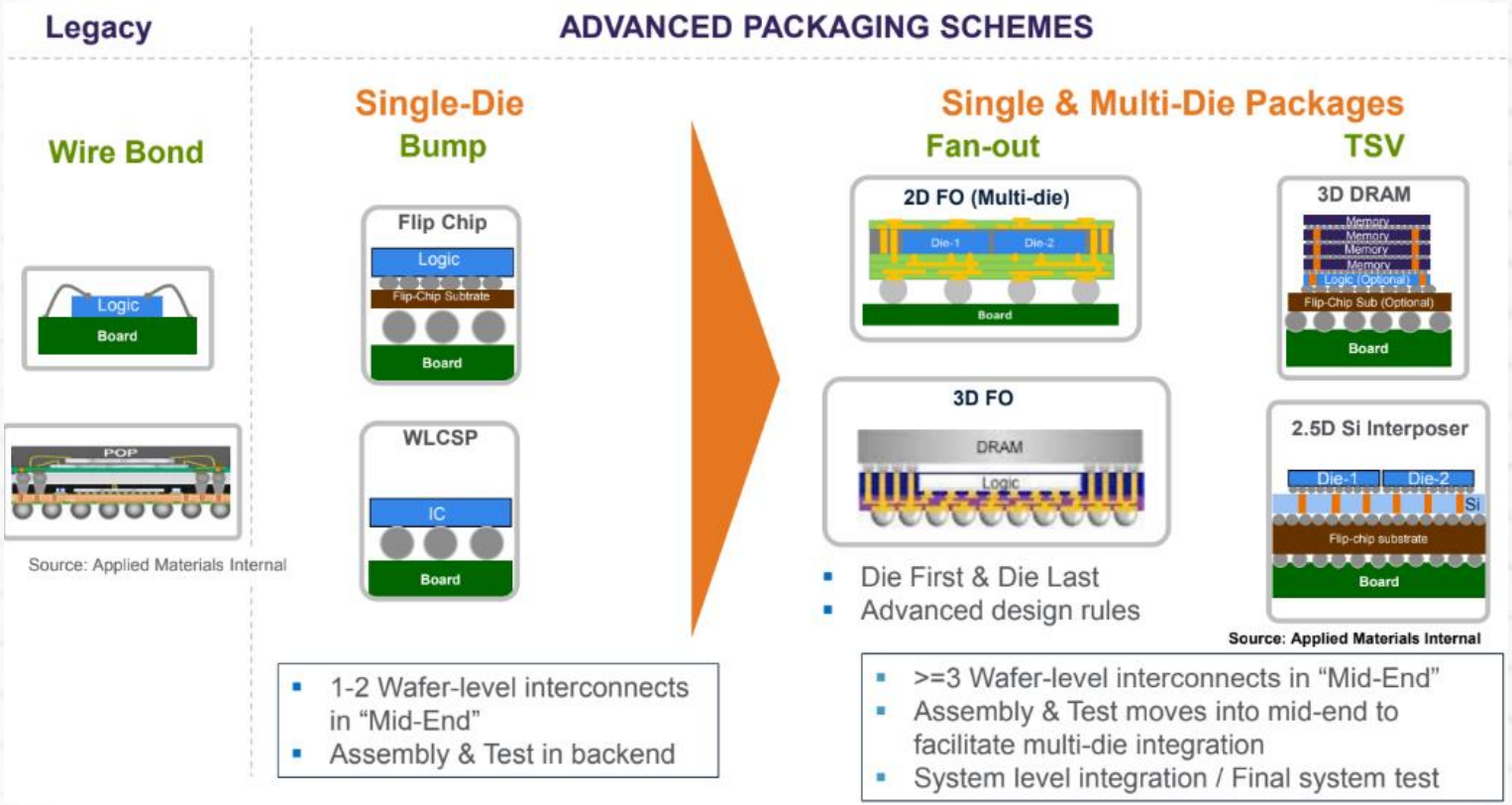
Packaging

- 2D and 3D packaging technologies are enabling new device form factors and additional boosts in performance and efficiency.



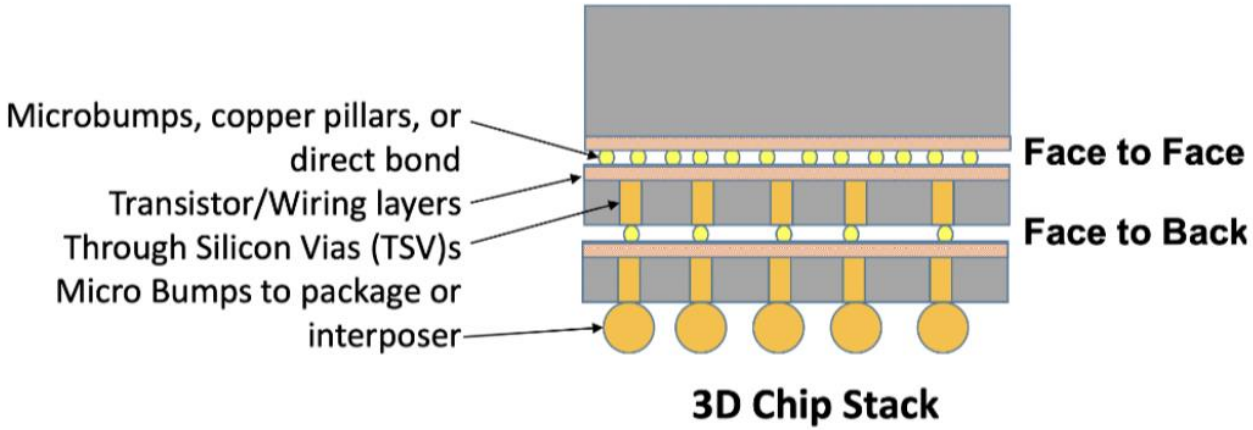
Ref. : AMAT, 2022

Packaging



Ref. : AMAT, 2022

3DIC

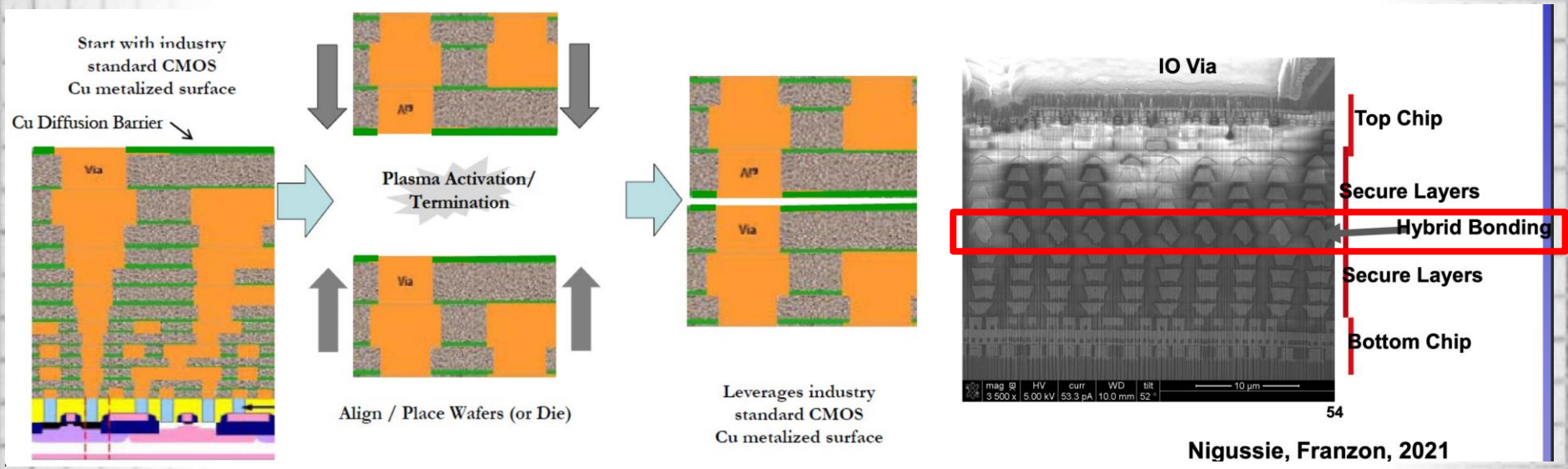


Typical Dimensions: Thinned Chip : 25 - 50 μm
Unthinned chip : 300 μm
Microbump pitch : 25 μm +
Direct Bond pitch : 1 μm +
Through Silicon Via (TSV) Diameter : 5 – 10 μm
TSV pitch : 25 μm +

Ref. : Paul Franzon, 3D-IC, 2021

- Vertically stacking chips into a single package

Hybrid Bonding

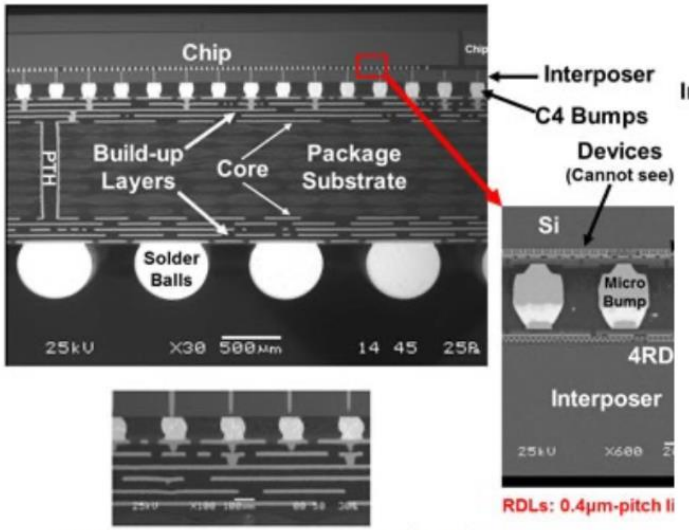


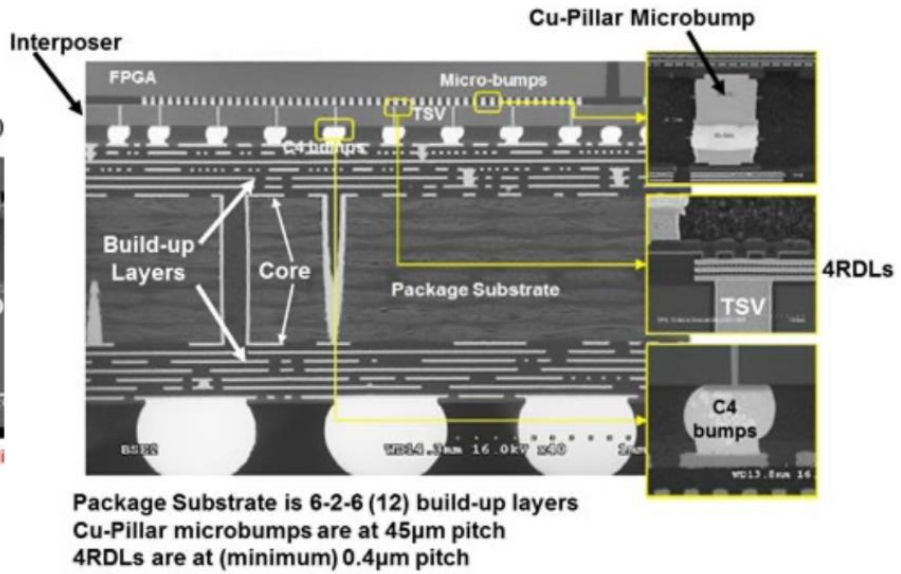
Ref. : Paul Franzon, 3D-IC, 2021

Ref. : Nigussie, Franzon, 2021

- Plasma active bonding

Interposer



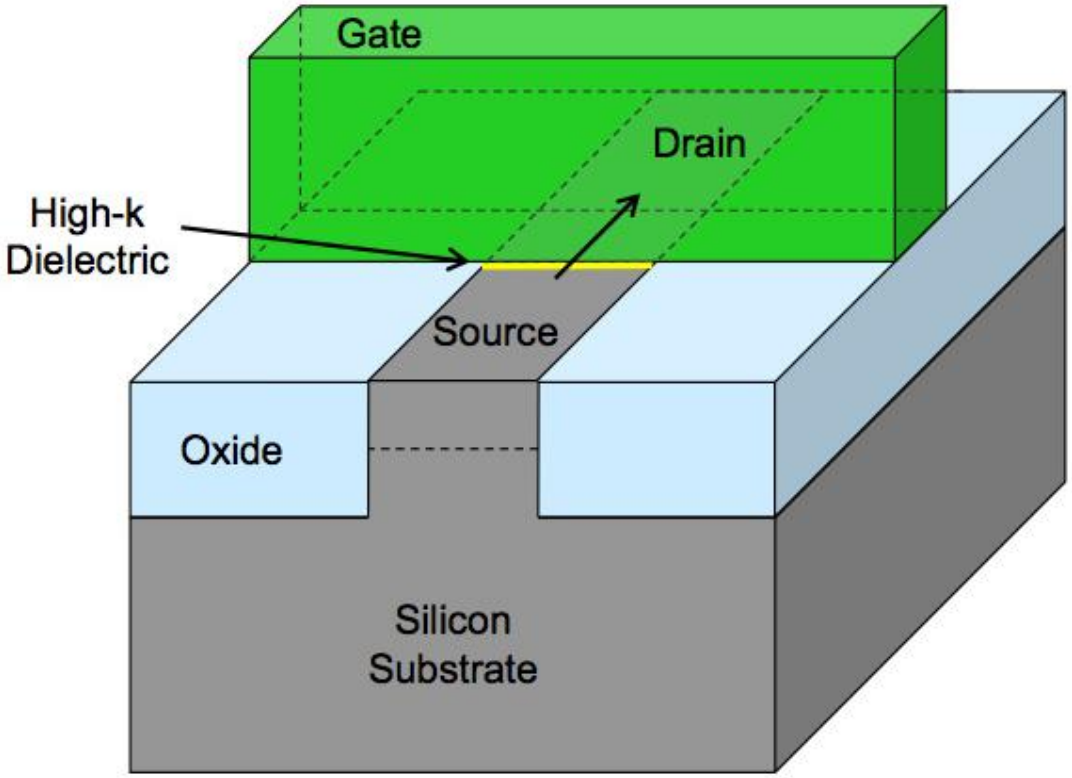


Ref. : Paul Franzon, 3D-IC, 2021

- High density silicon interposers are expensive

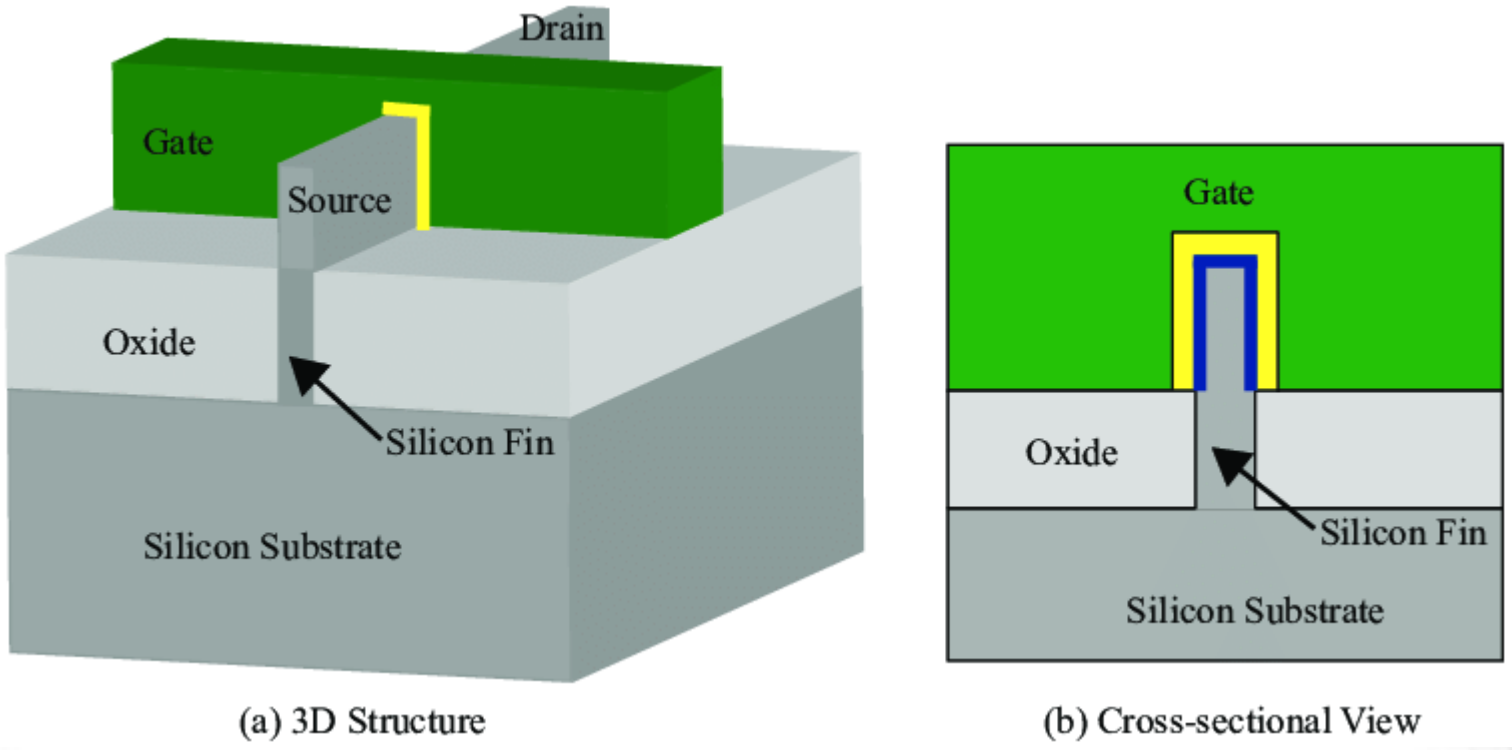
Ref. : https://semiwiki.com/semiconductor-services/ic knowledge/316095-semicon-west-2022-and-the-imec-roadmap/

Planar



Ref. : https://www.google.com/url?sa=i&url=https%3A%2F%2Fwww.anandtech.com

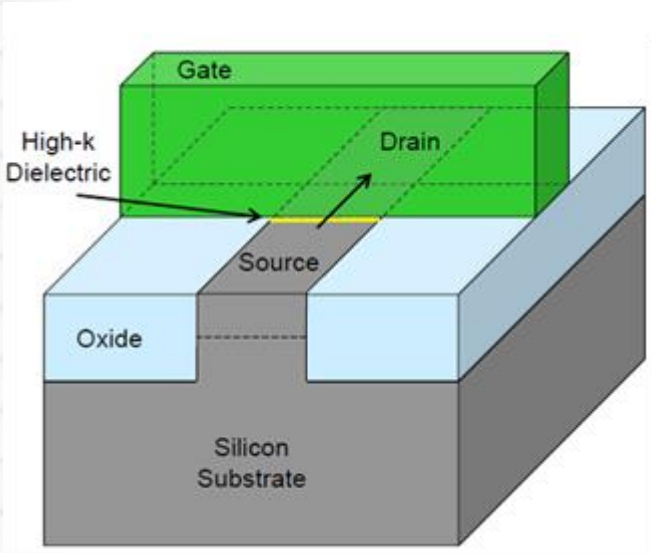
FinFET



Ref. : https://www.google.com/url?sa=i&url=https%3A%2F%2Fwww.researchgate.net

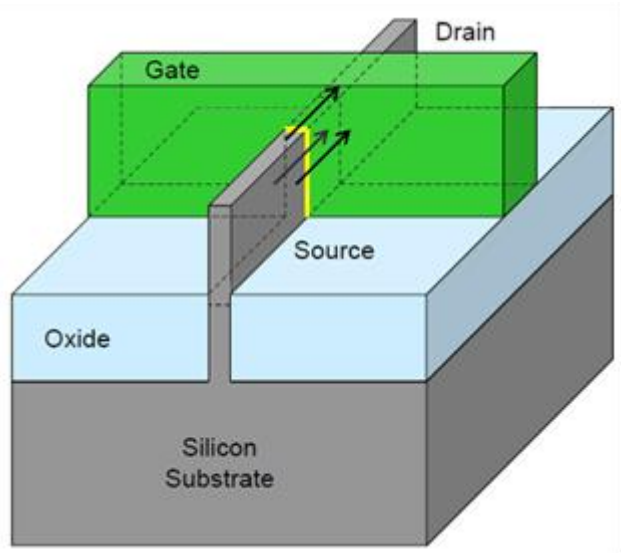
Planar v.s. FinFET

Planar



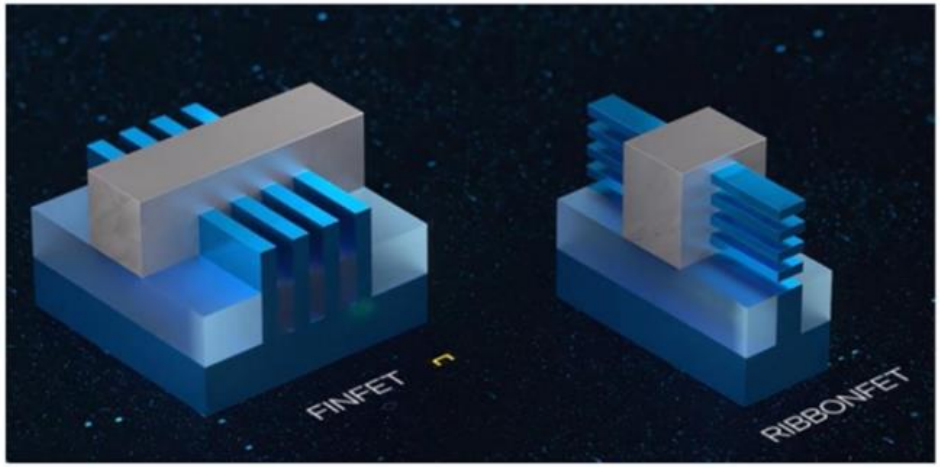
- Conducting channel only on the surface

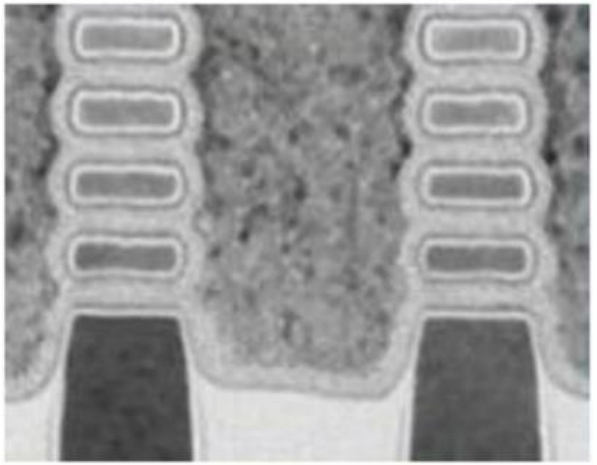
FinFET



- Conducting channel on 3 sides of the fin

Nanosheet (GAA)





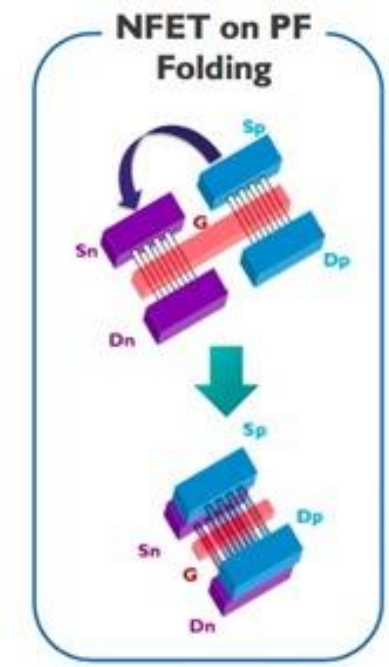
Ref. : Intel, 2022 VLSI Short Course

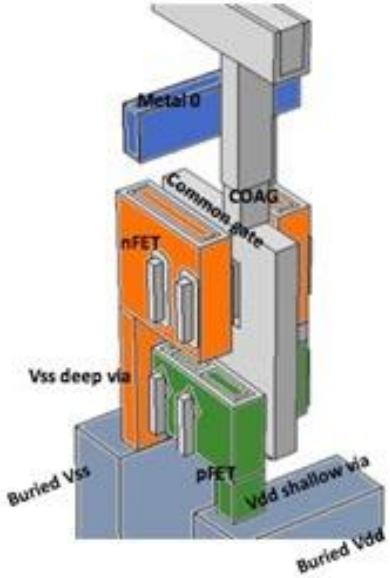
Nanosheet benefits over FinFET

- More effective and flexible transistor width per footprint
- Better short channel control over FinFET

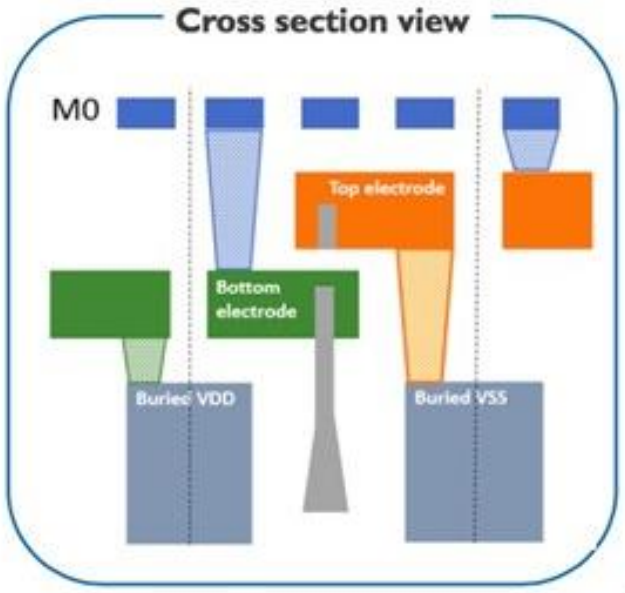
CFET

Ref. : N. Horiguchi, VLSI 2021



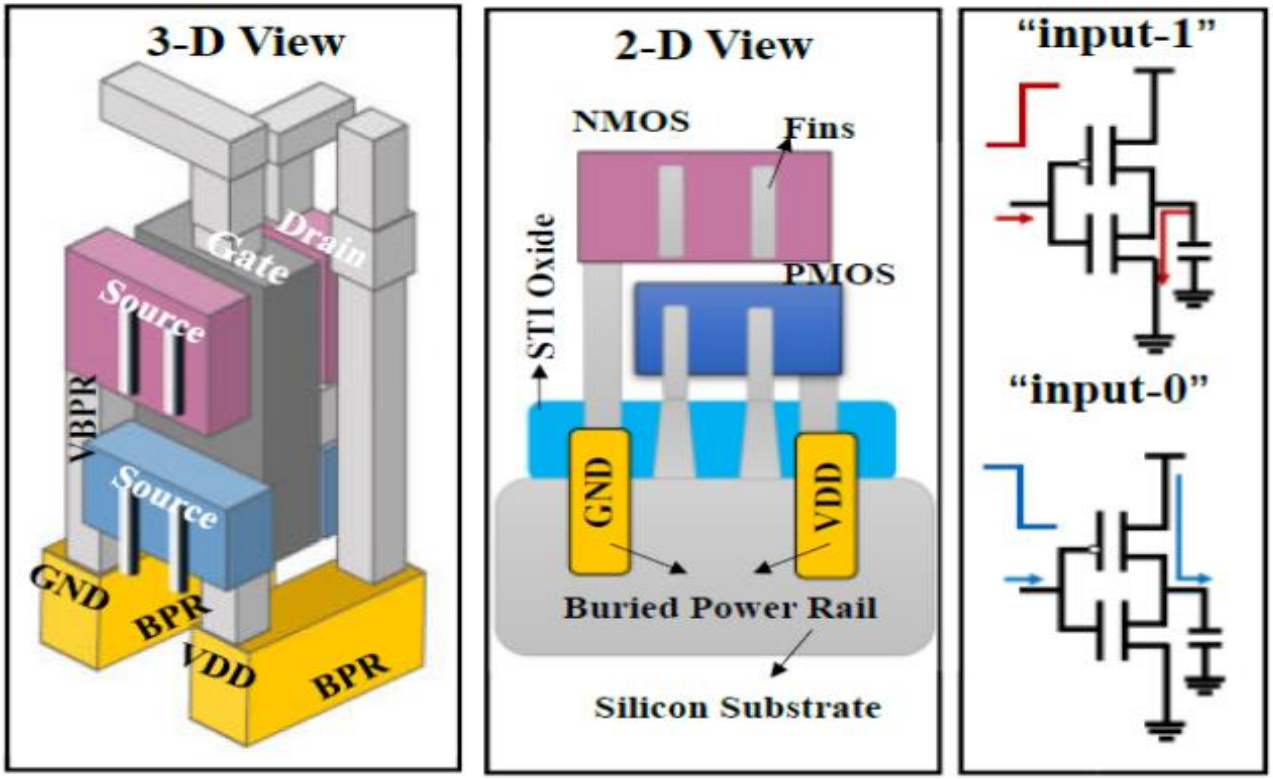


Ref. : J. Ryckaert et al, IEDM 2019



- Vertically stack nFET on pFET or vice versa
- Increase transistor density per footprint

CFET Inverter

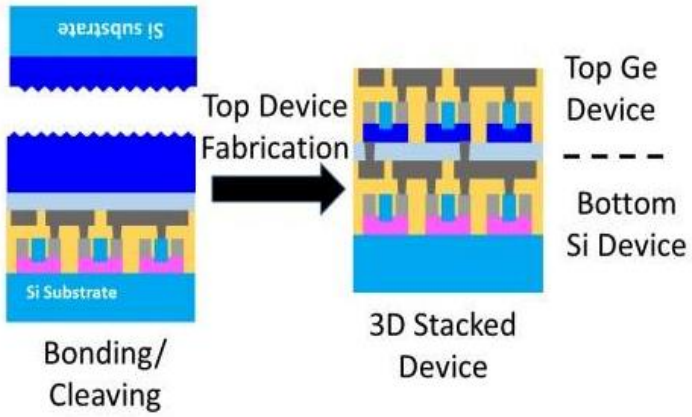


Ref. :

S. Zhao et al., "Investigation of Self-heating and Thermal Network for Complementary FET," 2021 Silicon Nanoelectronics Workshop (SNW), Kyoto, Japan, 2021, pp. 1-2.

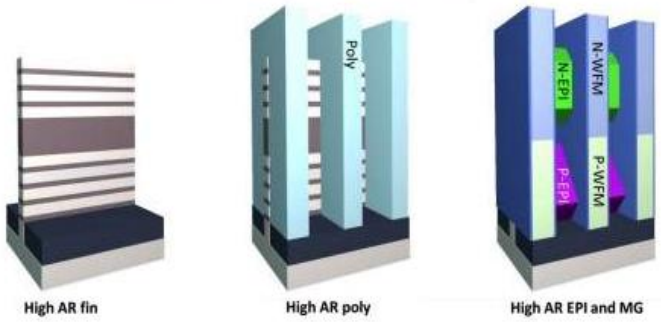
CFET

Sequential 3D



- Separate top and bottom layer processing
- Flexible to co-integrate heterogeneous channel materials
- Thermal budget limit
- Top devices not self-aligned to bottom devices
- Higher cost

Self-Aligned (Monolithic) 3D



- Self-aligned fin and poly patterning for top and bottom devices
- Similar flow as conventional 2-D CMOS → lower cost
- Higher aspect ratio process complication

Ref. : Chung-Hsun Lin, Advanced Semiconductor Device and Technology Spring 2023