VLSI SINCE 1983
2023 International VLSI Symposium on Technology, Systems and Applications
ITRI Industrial Technology Research Institute
IEEE
April 17-20, 2023 Hsinchu, Taiwan

Nanosheet Extensions and Beyond

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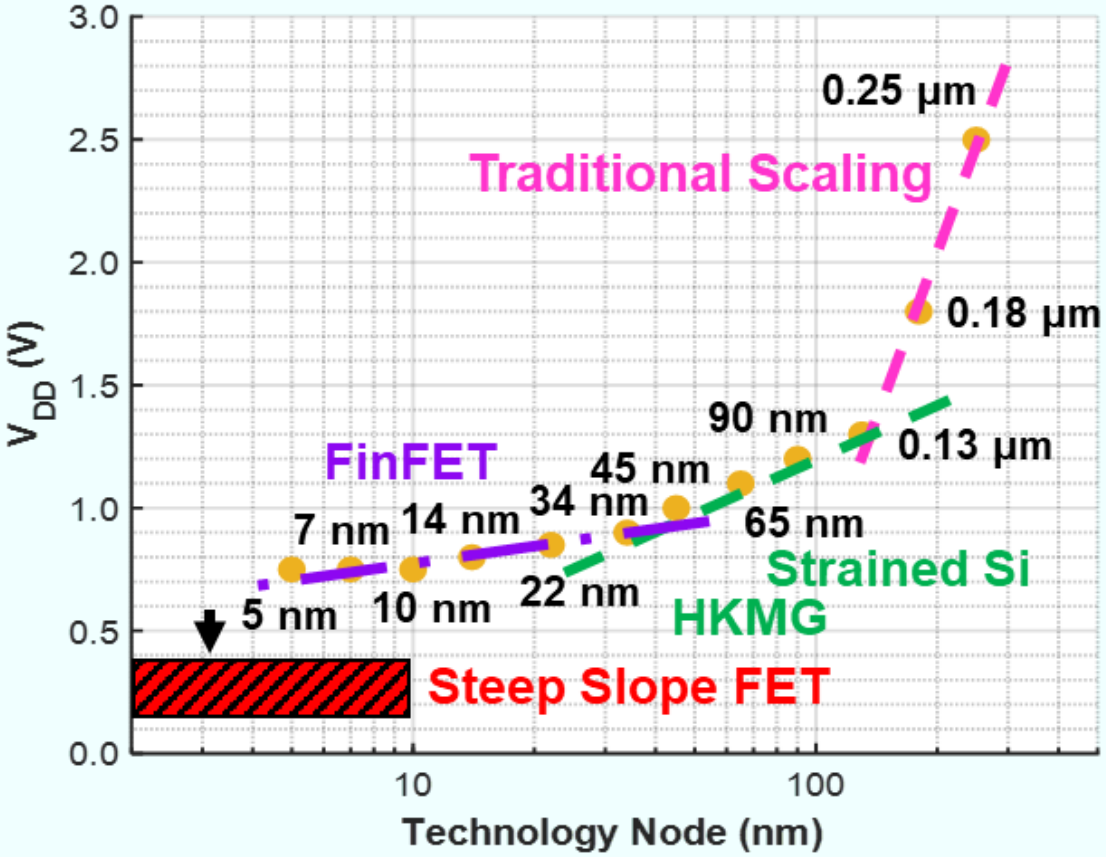
http://nanosioe.ee.ntu.edu.tw

https://wa-people.com/post.aspx?seq=4623

Outline

- Introduction
- Extensions
  - High Mobility Channels
  - Highly Stacked Channels
  - High-κ Gate Dielectric
  - Ultrathin Body
- Beyond
  - TreeFET
  - CFET

V_{DD} Scaling Trend vs Technology Node



Ref:

10 nm: IRDS 2017 EDITION MORE MOORE

7 nm:

[1] IRDS 2018 UPDATE MORE MOORE

[2] Hung-Li Chiang et al., Design Technology Co-Optimization for Cold CMOS Benefits in Advanced Technologies, 2021 IEDM

[3] J. Chang *et al*., ISSCC, 2017(TSMC)

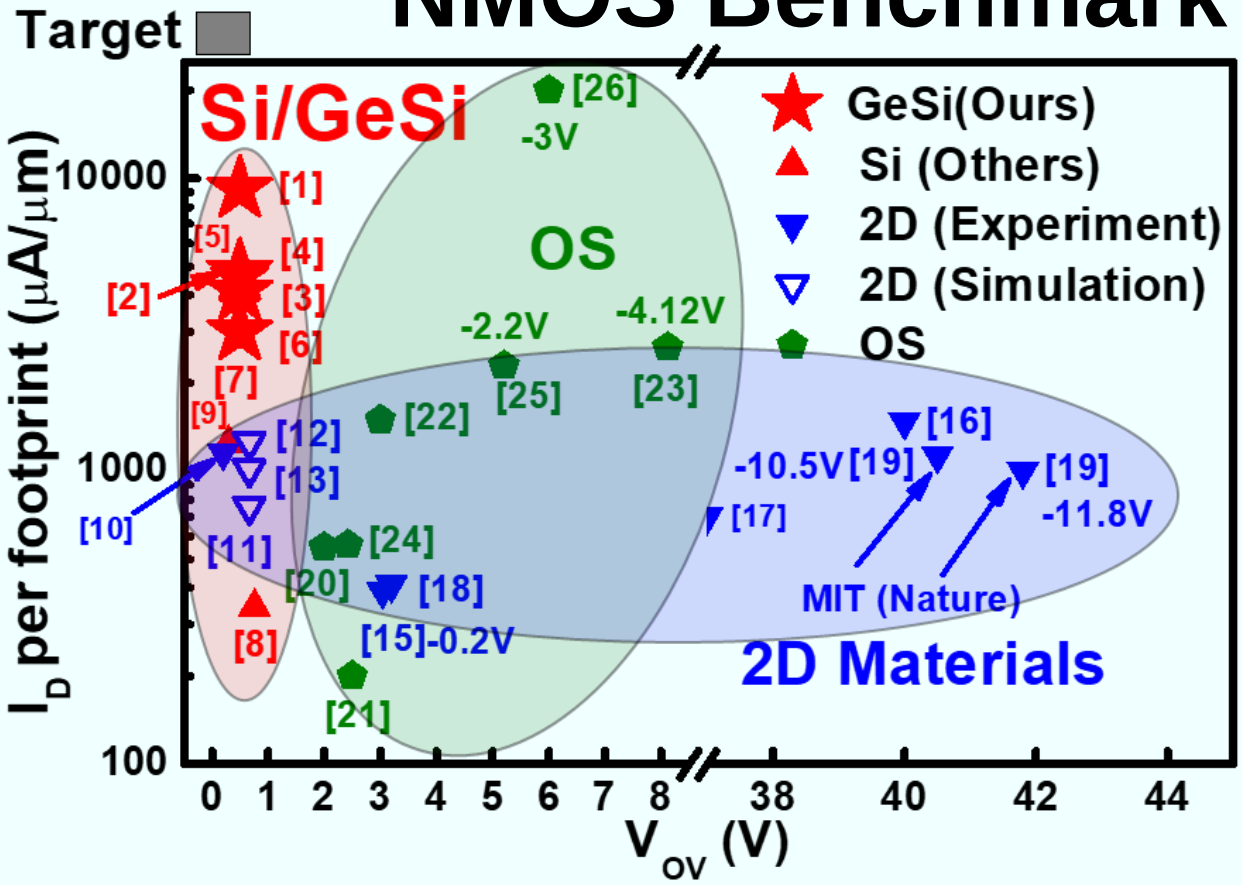
5 nm:

[1] IRDS 2021 UPDATE MORE MOORE

[2] J. Chang *et al*., ISSCC, 2020(TSMC)

- iMOS
- TFET
- NCFET

NMOS Benchmark

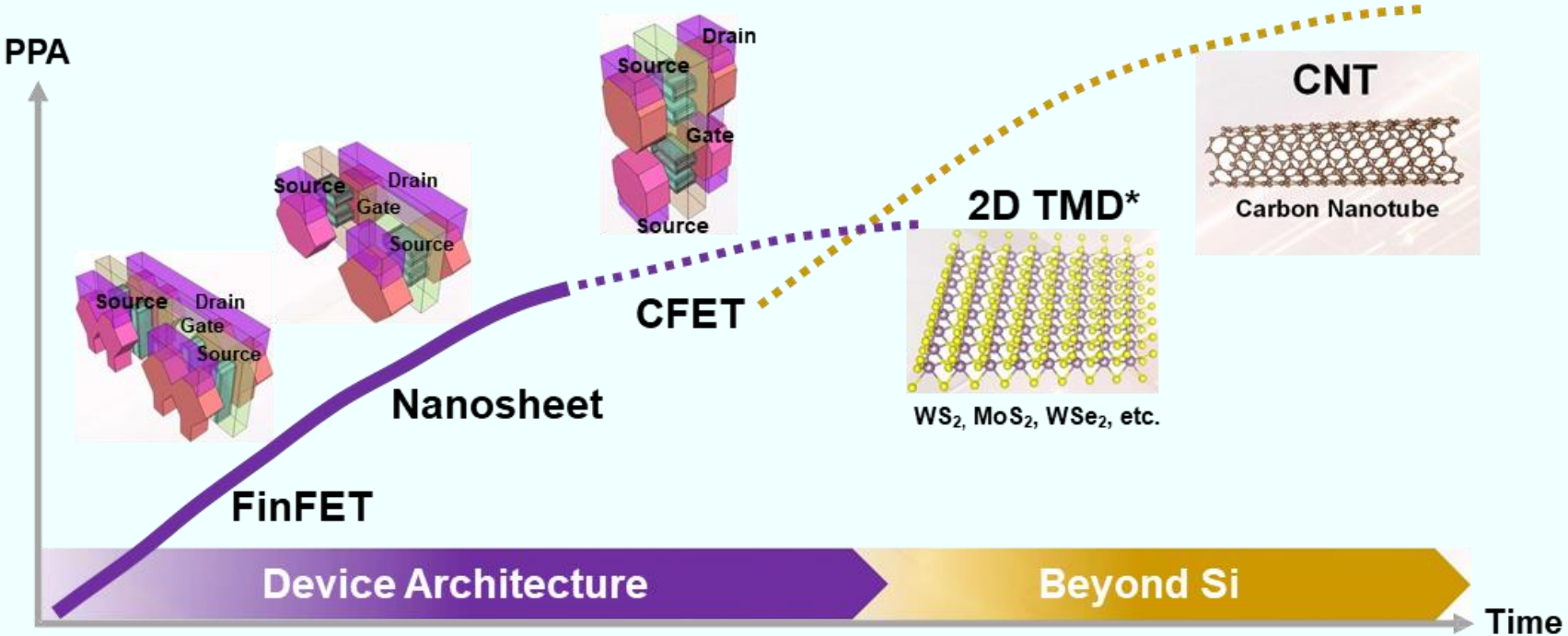


- Negative V_t and large V_{OV} are not acceptable for IC design.

Device roadmap

- FinFETs has been adopted for 6/7 generation from 16/22 node
- Nanosheet extensions are desired to extend its lifetime.
- Atomic channel can be 2D or ultrathin body (<3 nm).

Device Architecture Outlook



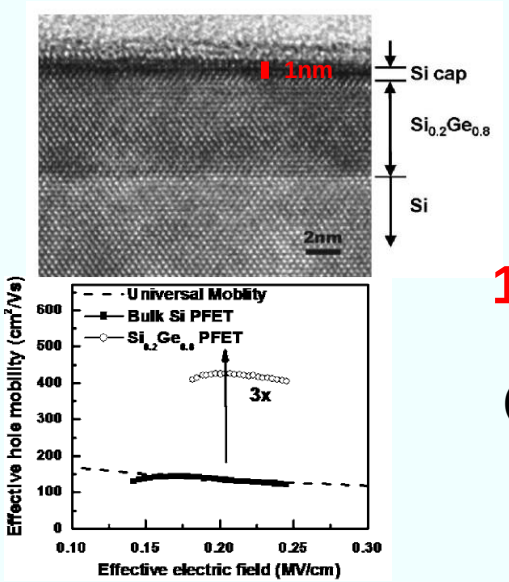
* TMD: transition metal dichalcogenides

Yuh-Jier Mii, VLSI, 2022, Plenary Session 2-2. (tsmc)

- CFET after nanosheets, 2D after CFETs
- Si PPA may be underestimated?

The first adoption of HMC in 5 nm node

2007 APL

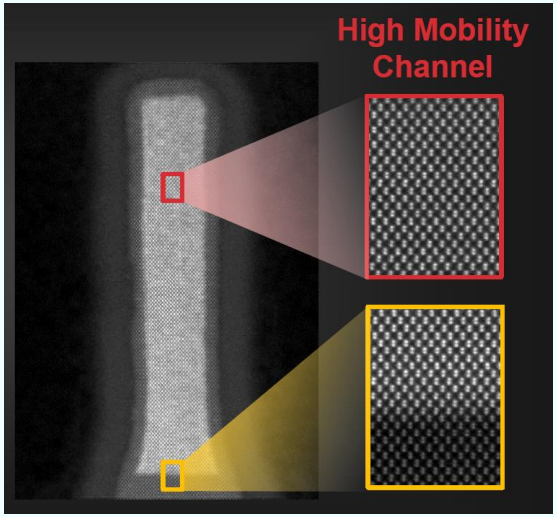


C.-Y. Peng, F. Yuan, C.-Y. Yu, P.-S. Kuo, M. H. Lee, S. Maikap, C.-H. Hsu, and C. W. Liu, Appl. Phys. Lett. 90, 012114 (2007) .(Cited No./Self Cited No.= 30/ 7)

13 years

(2007-2020)

2021 TSMC ISSCC

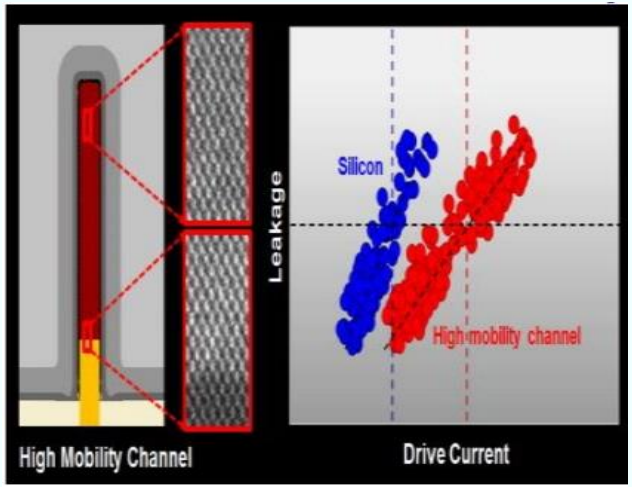


Mark Liu, Plenary Session 1.1, ISSCC 2021.

- **$Si_{0.2}Ge_{0.8}$ channel with 1nm Si cap, having higher mobility (3X) than Si.**
- **It takes 13 years to commercialize HMC.**

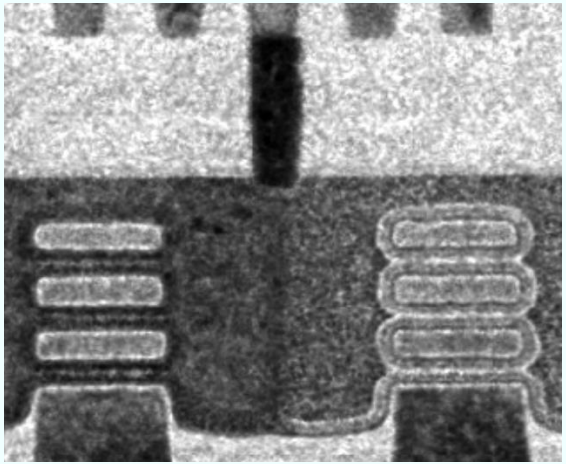
HMC and Stacked GAAFETs

(TSMC)



Geoffrey Yeap *et al*., *IEDM*, 2019, 36.7.

(TSMC)



Mark Liu, *ISSCC*, 2021, Plenary Session 1.1.

Yuh-Jier Mii, *VLSI*, 2022, Plenary Session 2-2.

- High mobility SiGe channel (HMC) is used in the 5nm node.
- Stacked GAAFET as replacement of FinFETs.

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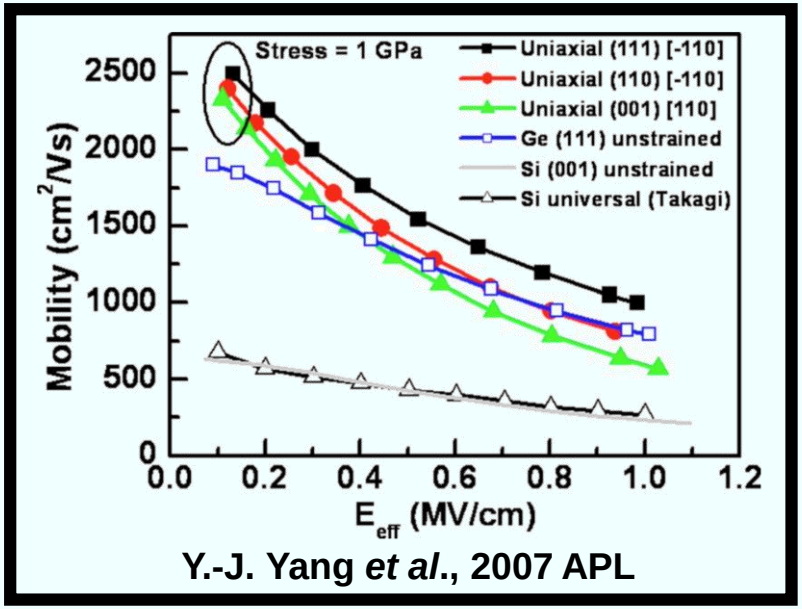
  - **Highly Stacked Channels**
  - **High-κ Gate Dielectric**
  - **Ultrathin Body**
- Beyond
  - TreeFET
  - CFET

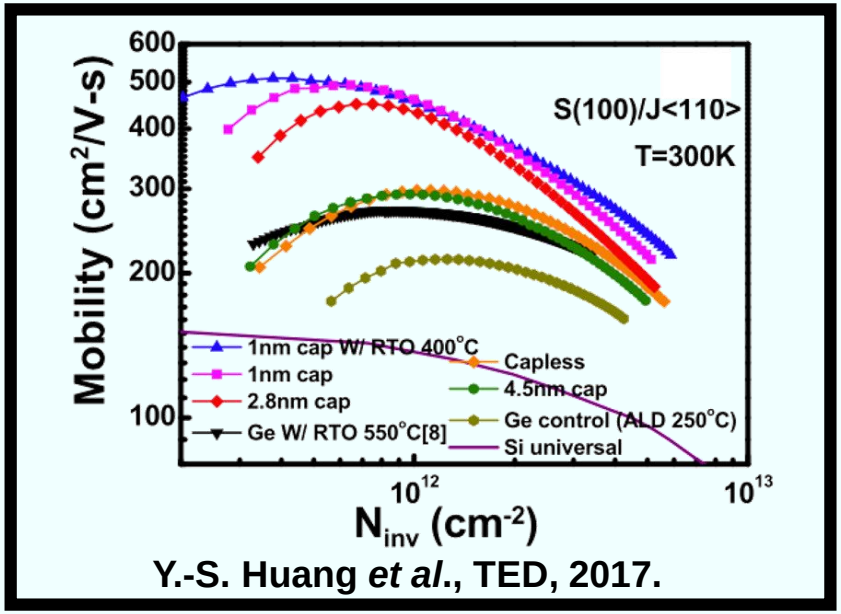
High Mobility Channel

Ge electron mobility



Y.-J. Yang *et al.*, 2007 APL

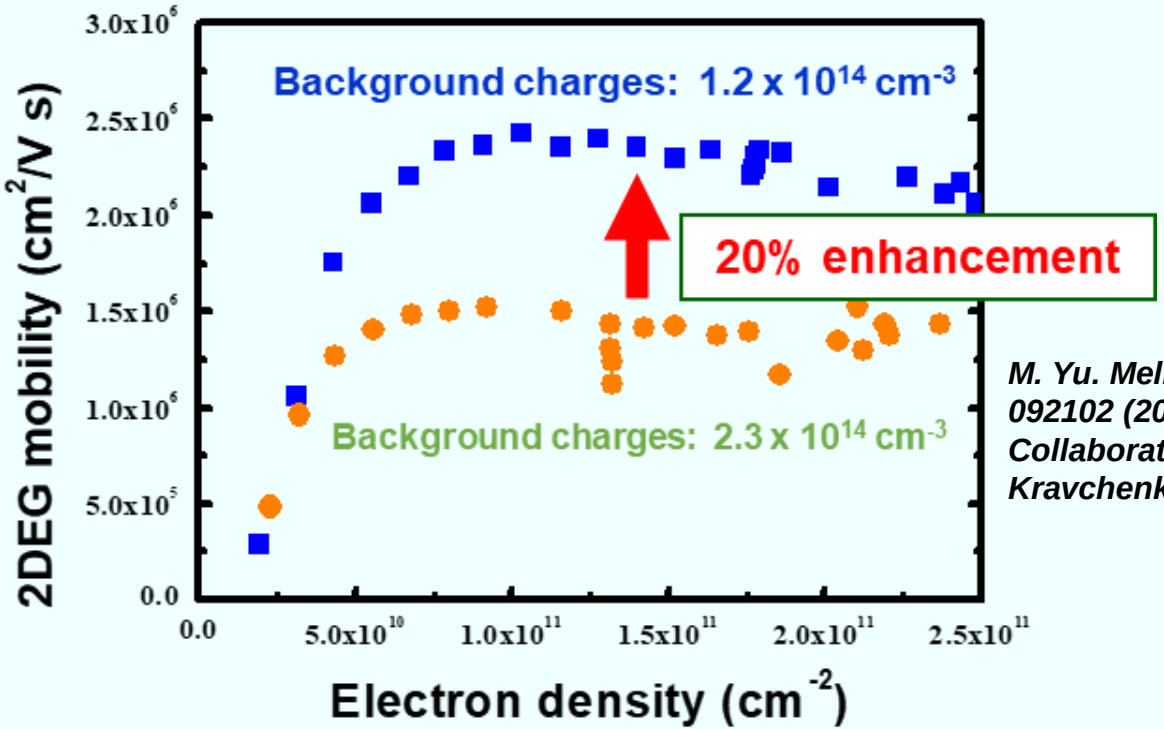
GeSn hole mobility



Y.-S. Huang *et al.*, TED, 2017.

- Ge has higher electron mobility than Si.
- GeSn/Ge has higher hole mobility than Si.

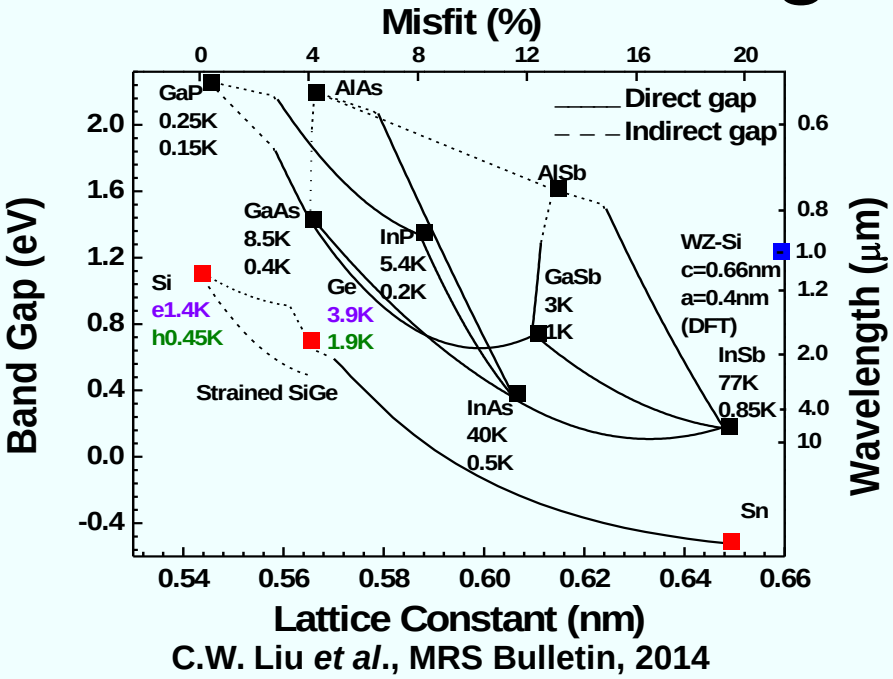
Record High 2DEG Mobility (2.4 M cm²/V s)



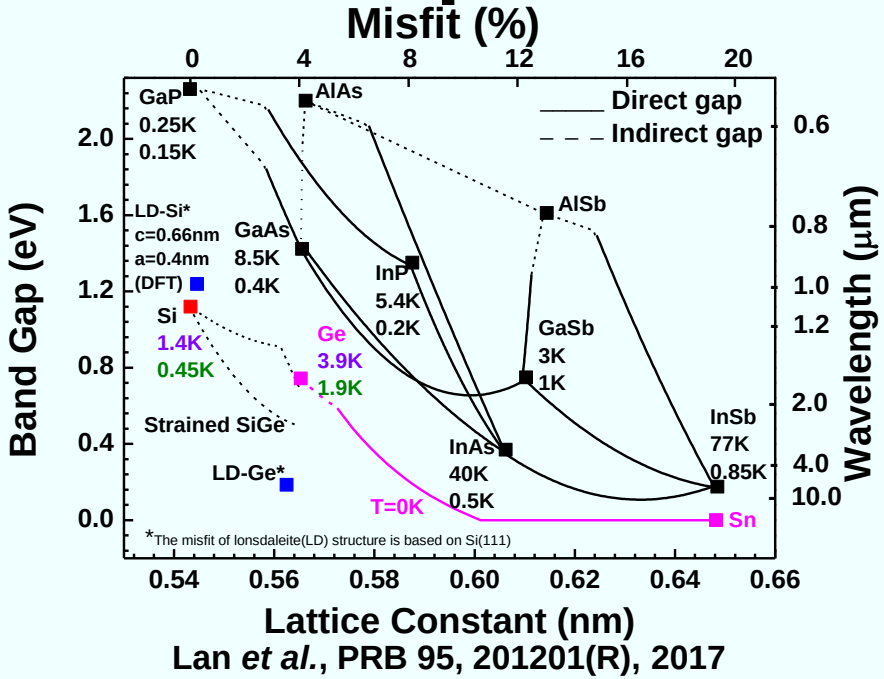
M. Yu. Melnikov et al., APL, 106, 092102 (2015).
Collaborate with Prof. S. V. Kravchenko, Northeastern Univ.

- **2.4×10^6 cm²/V s by the reduction of background charges from 2.3 x 10^{14} cm^{-3} to 1.2 x 10^{14} cm^{-3}.**

Something About Group IV



C.W. Liu *et al*., MRS Bulletin, 2014

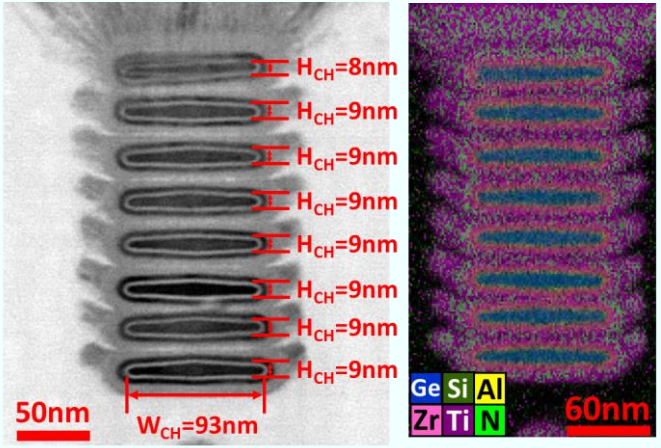


Lan *et al.*, PRB 95, 201201(R), 2017

- [Sn] > 0.41 ➔ $Ge_{1-y}Sn_y$ becomes topological semimetal/ zero bandgap semiconductor (E_g=0)
- [Sn] =0.1 ➔ E_g = 0.54eV ➔ Large I_{OFF}

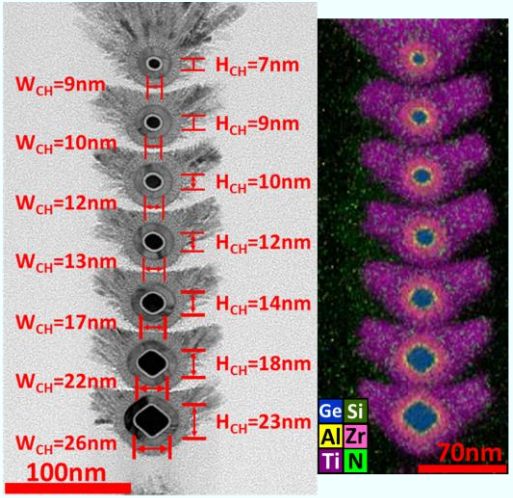
Highly Stacked GAAFETs

8 $Ge_{0.75}Si_{0.25}$ Nanosheets (NTU)



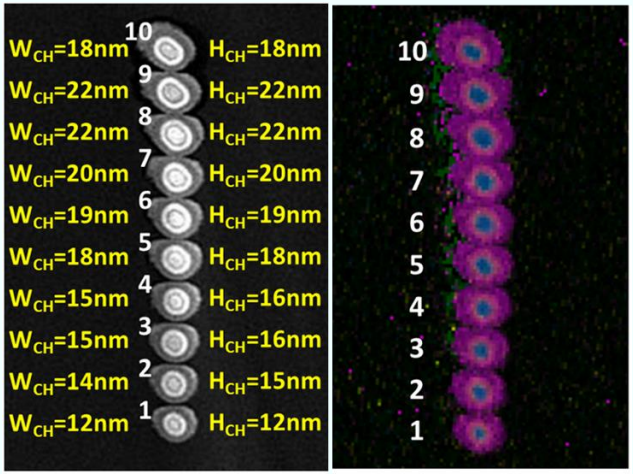
Yi-Chun Liu *et al.*, *VLSI*, 2021, T15-2.

8 $Ge_{0.95}Si_{0.05}$ Nanowires (NTU)



Yi-Chun Liu *et al.*, *VLSI*, 2021, T15-2.

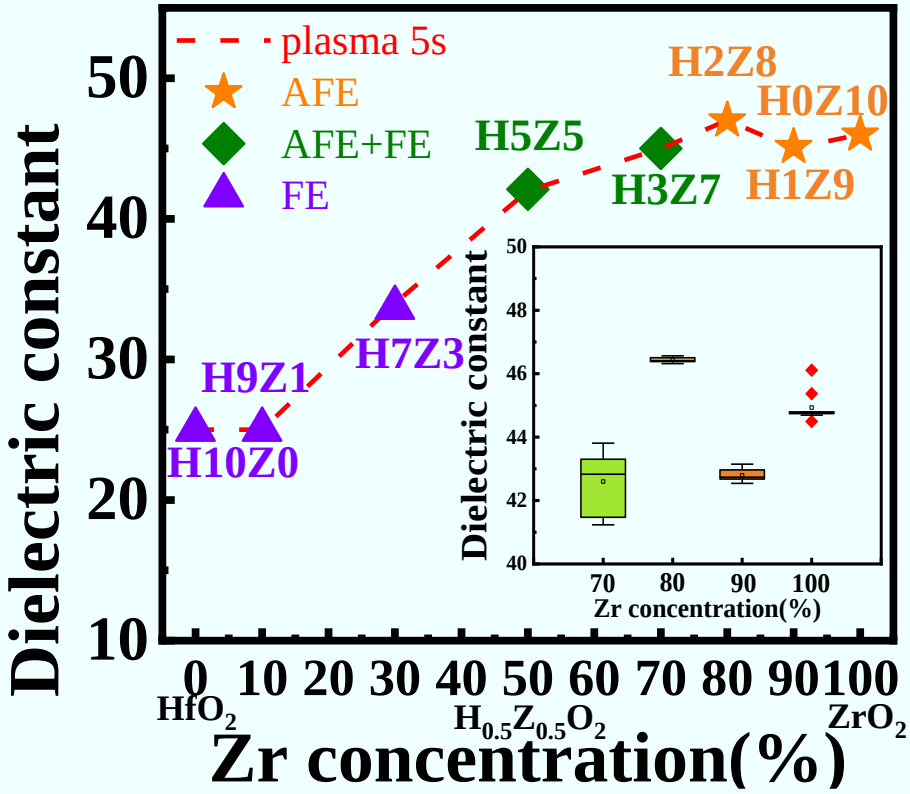
10 $Ge_{0.95}Si_{0.05}$ Nanowires (NTU)



Yi-Chun Liu *et al.*, *SISC*, 2022.

- **The higher number of stacked channels can further enhance the drive current for a given footprint.**

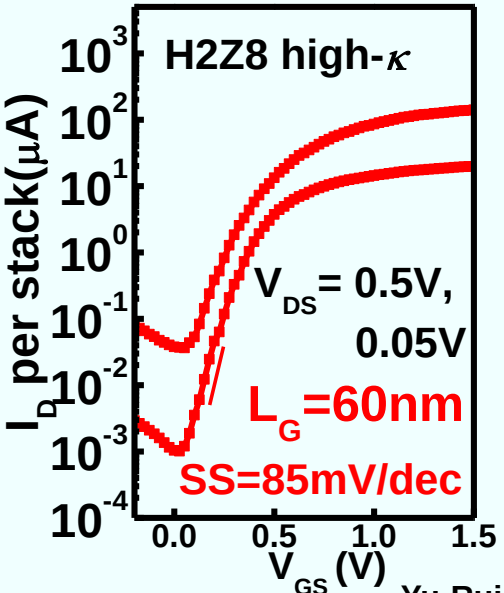
Dielectric Constant of H_xZ_yO MFM/MIM Capacitors

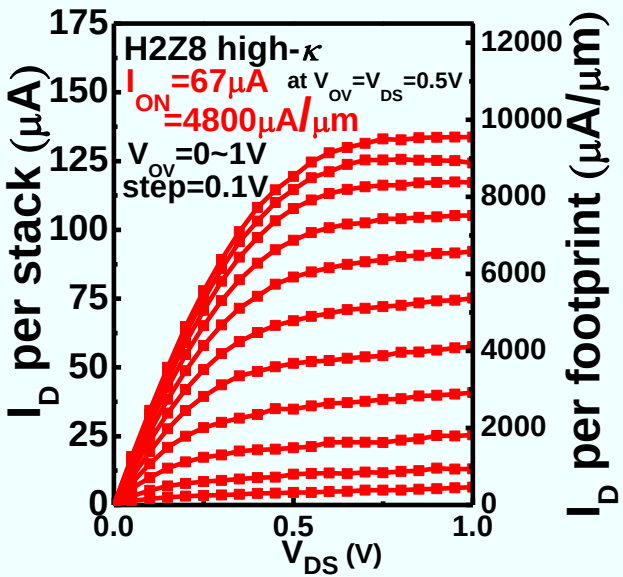


Yu-Rui Chen *et al.*, *EDL*, vol.43, no. 10, 2022.

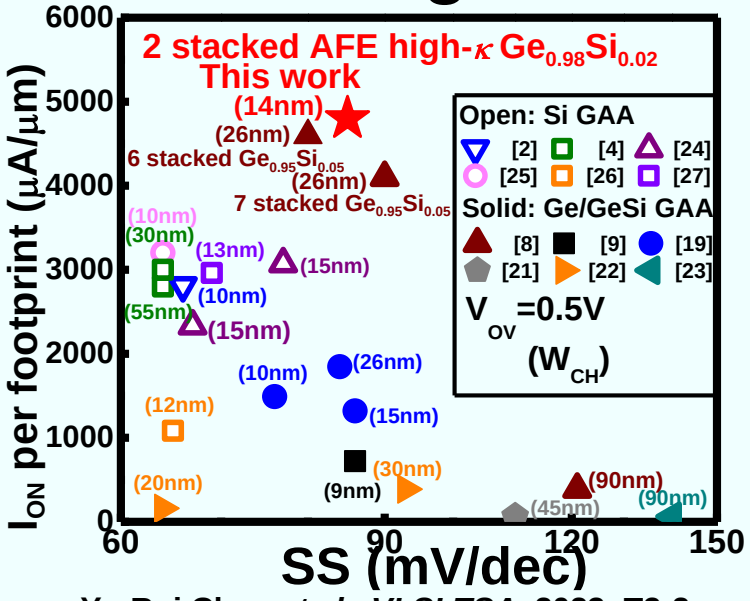
- **The peak dielectric constant of 47 is achieved at [Zr]=80%.**

2 Stacked $Ge_{0.98}Si_{0.02}$ NWs with H2Z8 High-κ





Yu-Rui Chen *et al.*, *EDL*, vol.43, no. 10, 2022.



Yu-Rui Chen *et al.*, *VLSI-TSA*, 2023, T3-2.

- High I_{ON}=67μA per stack and high I_{ON} per footprint=4800 μA/μm at V_{OV}=V_{DS}=0.5V are achieved.
- High I_{ON} per footprint of 4800μA/μm is achieved among Si and Ge/GeSi nFETs with reasonable SS.

8 Stacked $Ge_{0.95}Si_{0.05}$ NWs/NSs with H2Z8 High-κ

Yi-Chun Liu *et al*.,
accepted by *VLSI*, 2023

- **The extremely high-κ $Hf_{0.2}Zr_{0.8}O_2$ gate stacks are integrated into both the 8 stacked $Ge_{0.95}Si_{0.05}$ nanowires and nanosheets.**

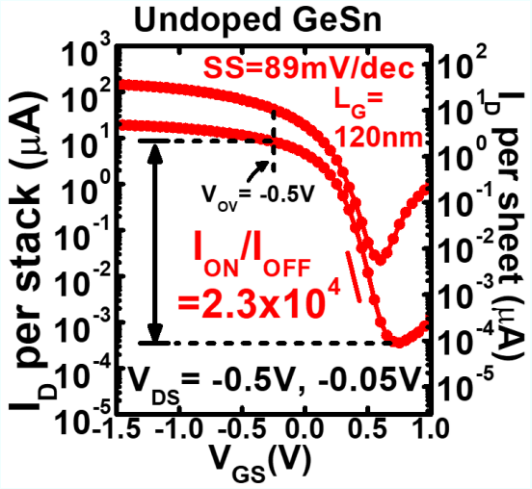
8 Stacked $Ge_{0.95}Si_{0.05}$ NWs/NSs with H2Z8 High-κ

Yi-Chun Liu *et al*.,
accepted by *VLSI*, 2023

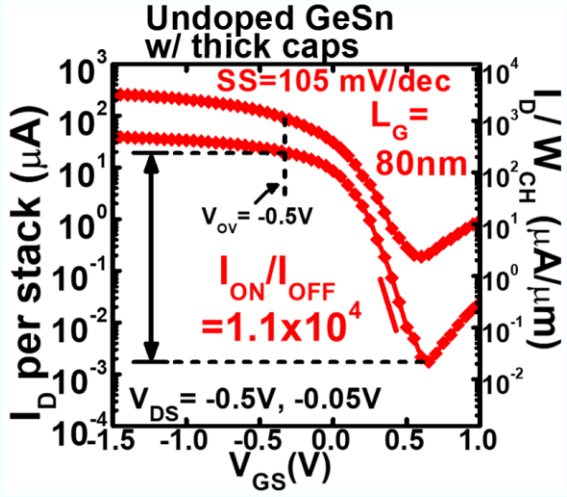
- **The 8 stacked $Ge_{0.95}Si_{0.05}$ nanowires and nanosheets reach the record I_{ON} per footprint of 9200μA/μm and the record I_{ON} per stack of 360μA at $V_{OV}=V_{DS}=0.5V$, respectively, among reported Si/GeSi/Ge 3D nFETs.**

Issues: Large I_{OFF} of GeSn Channels

Stacked GeSn nanosheets

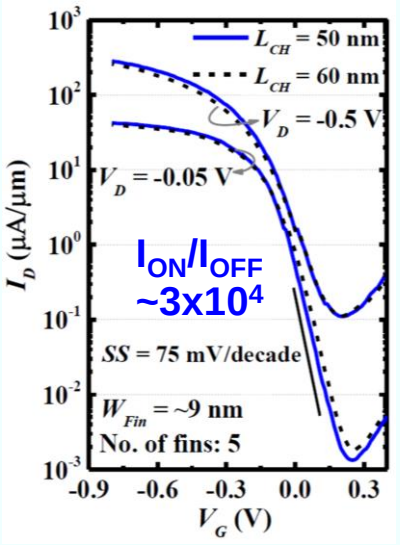


Yu-Shiang Huang *et al.*, *VLSI*, 2020, TC2.3. (NTU)



Yu-Shiang Huang *et al.*, *IEDM*, 2020, pp. 23. (NTU)

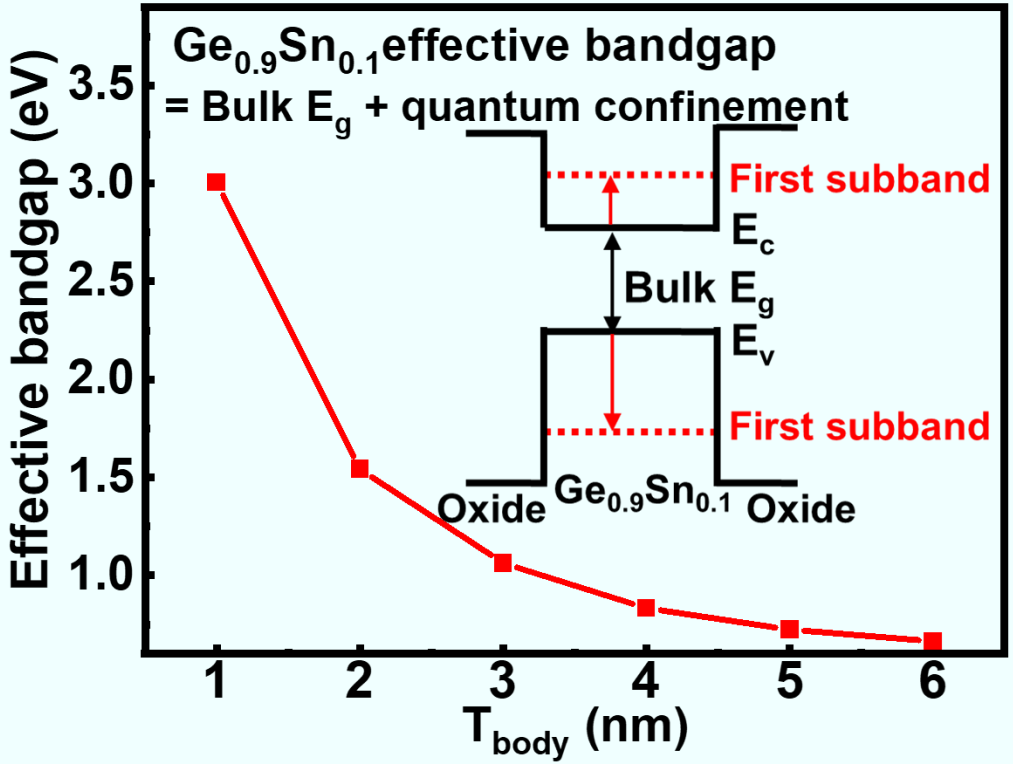
GeSn pFinFETs



Dian Lei *et al.*, *VLSI*, 2018, pp. T197. (NUS)

- Large I_{OFF} and small I_{ON}/I_{OFF} (<1E5) due to the small bandgap (0.54eV) of GeSn channels.

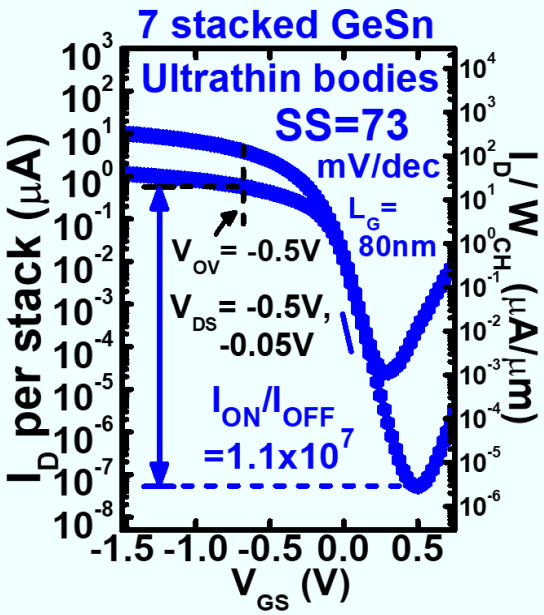
Quantum Confinement of Ultrathin Bodies

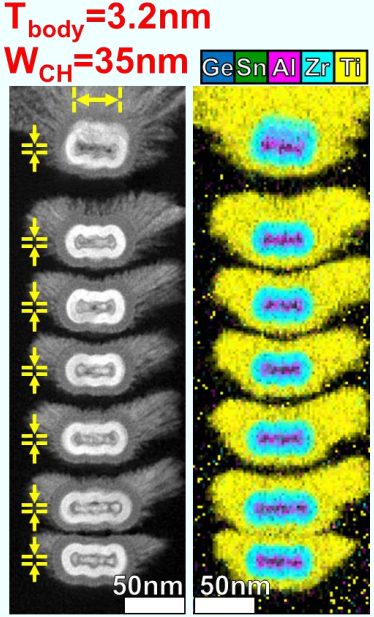


- Ultrathin bodies can increase the E_g by quantum confinement effect.

$Ge_{0.9}Sn_{0.1}$ Ultrathin Bodies (2021 IEDM)

(Roger A. Haken Best Student Paper Award, the first winner from Taiwan)



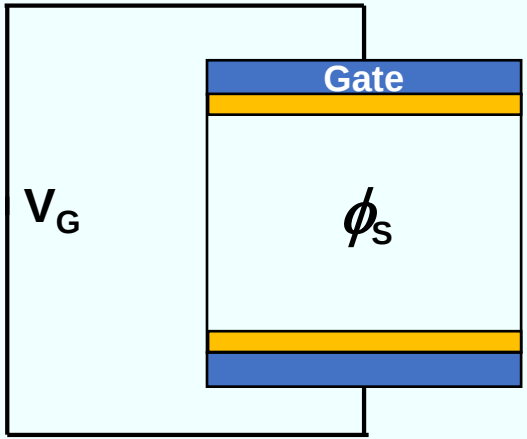


C.-E. Tsai *et al.*, IEDM, 2021, pp. 569.

- Low SS=73mV/dec and high I_{ON}/I_{OFF}=1.1x10^7 at V_{DS}= -0.05V.
- Highly uniform 7 stacked $Ge_{0.9}Sn_{0.1}$ ultrathin bodies with superior vertical uniformity.

Ultrathin Bodies for Low SS

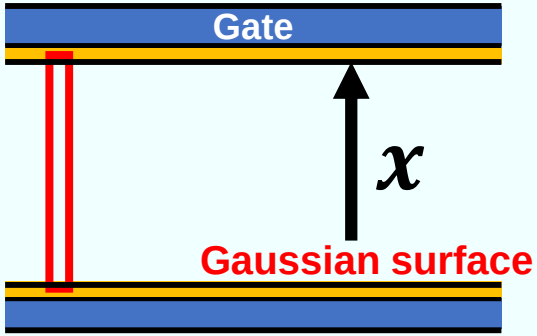
Ideally, channel doping = 0



- $\nabla\emptyset^2$=0 and boundary condition is V_G.
- No doping → $\phi_S = V_G$.
- SS = 60mV $\frac{V_G}{\emptyset_S}$

In reality, doping exist

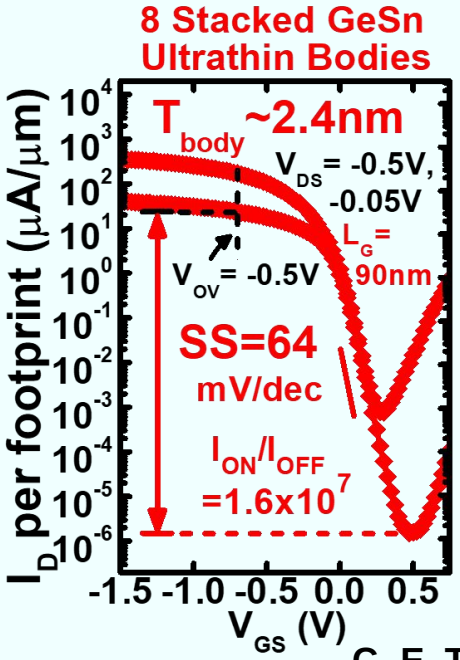
$$\nabla\emptyset^2 = \nabla E = \frac{\rho}{\epsilon}$$

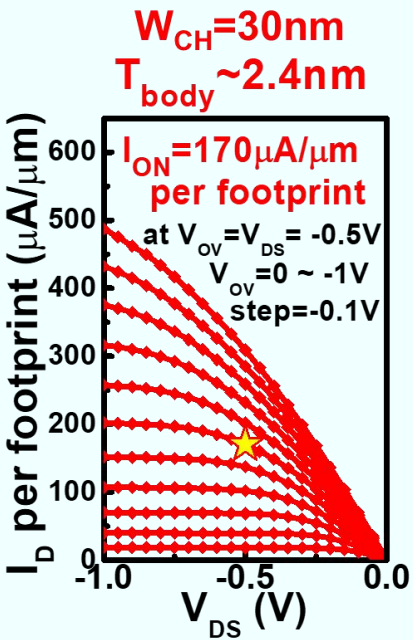


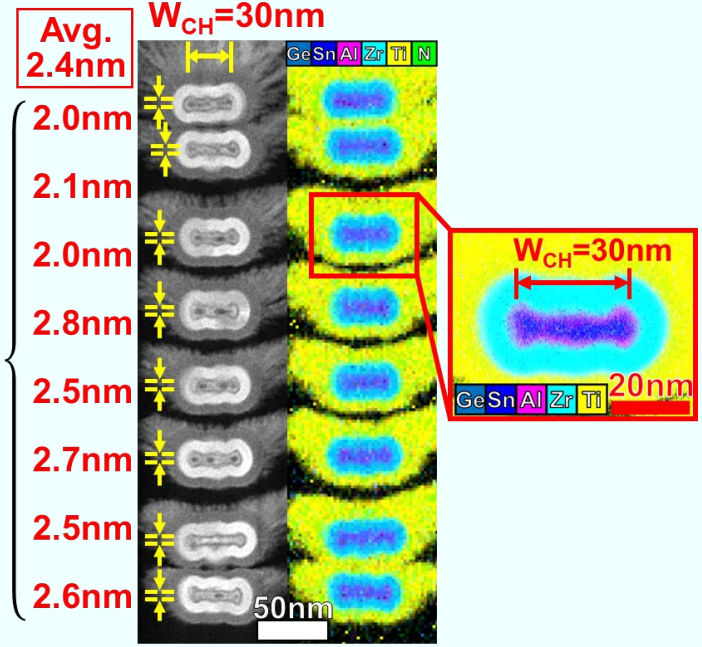
$$\oint \epsilon E dA = Q = A\int N_B dx = AN_B T_{body}$$

- $T_{body}\downarrow \rightarrow E\downarrow \rightarrow V_{OX}\downarrow$
- SS = 60mV($\frac{\emptyset_S + V_{OX}}{\emptyset_S}$)
- SS → 60mV/decade

$Ge_{0.9}Sn_{0.1}$ Ultrathin Bodies (2022 VLSI)



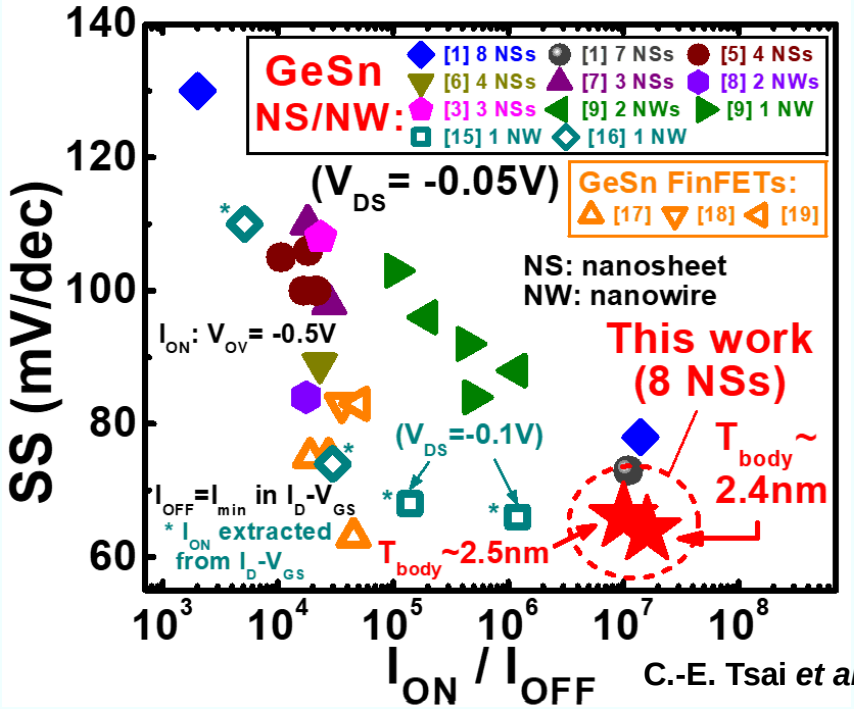




C.-E. Tsai *et al.*, VLSI, 2022, pp. 401.

- T_{body}~2.4nm with record low SS=64mV/dec and high $I_{ON}/I_{OFF}=1.6x10^7$ at V_{DS}= -0.05V among GeSn pGAAFETs.
- I_{ON}=170μA/μm per footprint normalized by W_{CH}=30nm.

SS and I_{ON}/I_{OFF} Benchmark of GeSn pGAAFETs



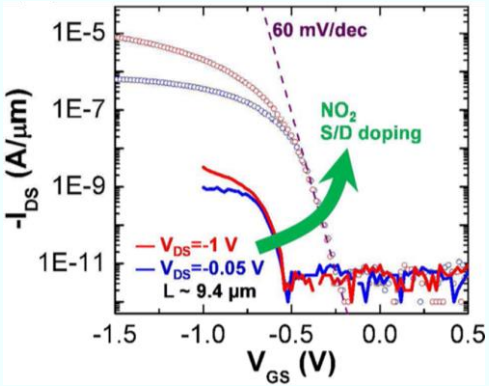
C.-E. Tsai *et al.*, VLSI, 2022, pp. 401.

[1] C.-E. Tsai et al., IEDM, 2021, pp. 569.
[3] Y.-S. Huang et al., EDL, 39, 9, 2018.
[5] Y.-S. Huang et al., IEDM, 2020, pp. 23.
[6] Y.-S. Huang et al., VLSI, 2020, TC2.3.
[7] Y.-S. Huang et al., IEDM, 2019, pp. 689.
[8] Y.-S. Huang et al., VLSI, 2019, pp. T180.
[9] Y.-S. Huang et al., IEDM, 2017, pp. 832.
[15] Y. Kang et al., Nano Lett., 21, 2021.
[16] Y. Kang et al., VLSI-TSA, 2019, T8-3.
[17] D. Lei et al., VLSI, 2018, pp. T197.
[18] D. Lei et al., VLSI, 2017, pp. T198.
[19] D. Lei et al., TED, 65, 9, 2018.

- 8 stacked GeSn ultrathin bodies (T_{body}~2.4nm) achieve nearly ideal SS of 64mV/dec and record I_{ON}/I_{OFF} of $1.6x10^7$ at V_{DS}= -0.05V among GeSn pGAAFETs.

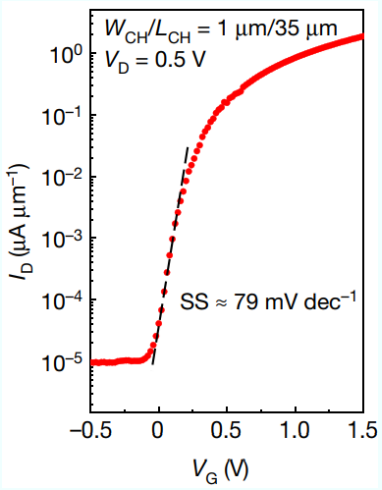
SS Benchmark

UC Berkeley
2D (WSe_2)
SS=60mV/dec



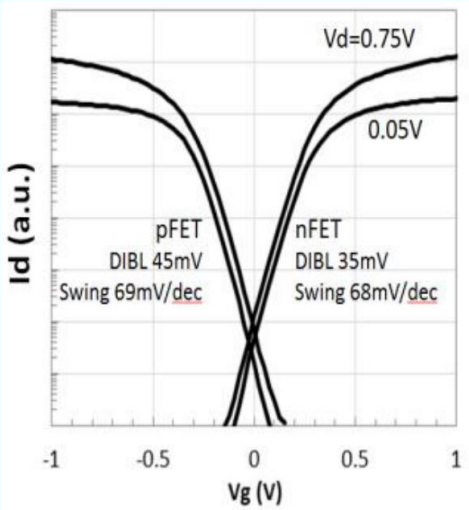
Fang, H. *et al.*, Nano Letters, 2012, 12(7), 3788–3792.

2D (MoS_2)
SS=79mV/dec



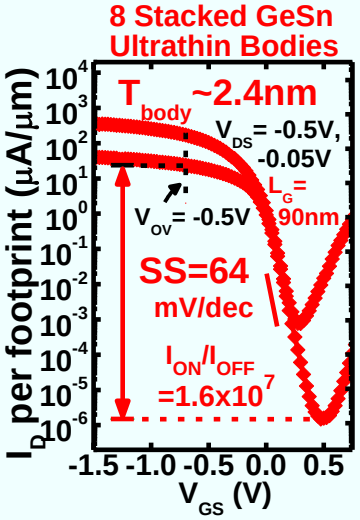
Huang, JK., Wan, Y., Shi, J. *et al.* *Nature* 605, 262–267 (2022).

TSMC 5nm
nFET SS=68mV/dec
pFET SS=69mV/dec



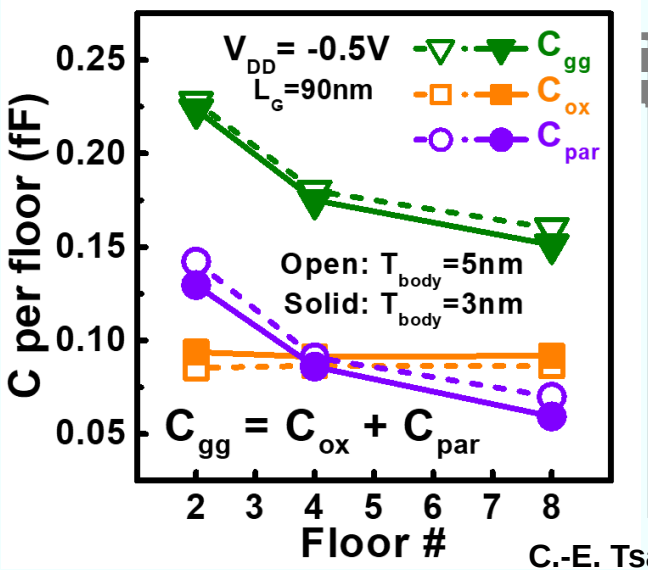
Geoffrey Yeap *et al.*, IEDM, 2019, 36.7.

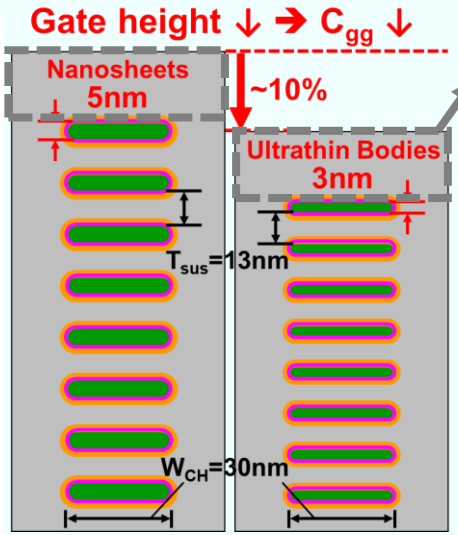
NTU Prof. C. W. Liu
Ultrathin body
pFET SS=64mV/dec



Chung-En Tsai *et al.*, VLSI, 2022.

Reduction of Total Gate Capacitance (C_{gg})





shared C_{par}

Floor # = the number of stacked channels

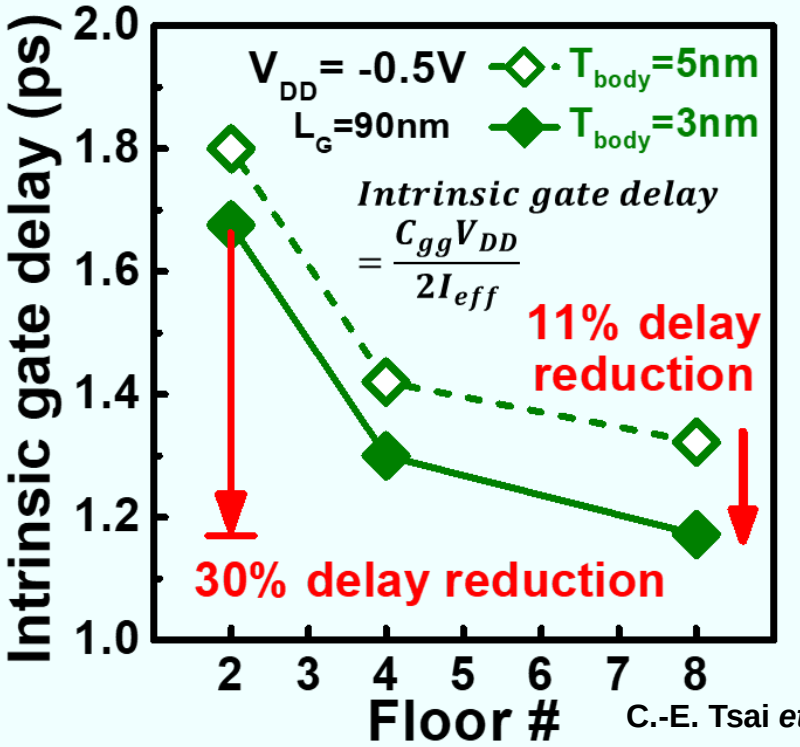
C_{gg}: total gate capacitance
C_{ox}: oxide capacitance
C_{par}: parasitic capacitance

➔ $C_{gg} = C_{ox} + C_{par}$

C.-E. Tsai *et al.*, VLSI, 2022, pp. 401.

- Floor # ↑ ➔ C_{par} per floor ↓ ➔ C_{gg} per floor ↓
- 3nm ultrathin bodies vs 5nm: Reduced gate height (~10%) ➔ Smaller C_{par} and C_{gg}, but similar C_{ox}

Reduction of Intrinsic Gate Delay



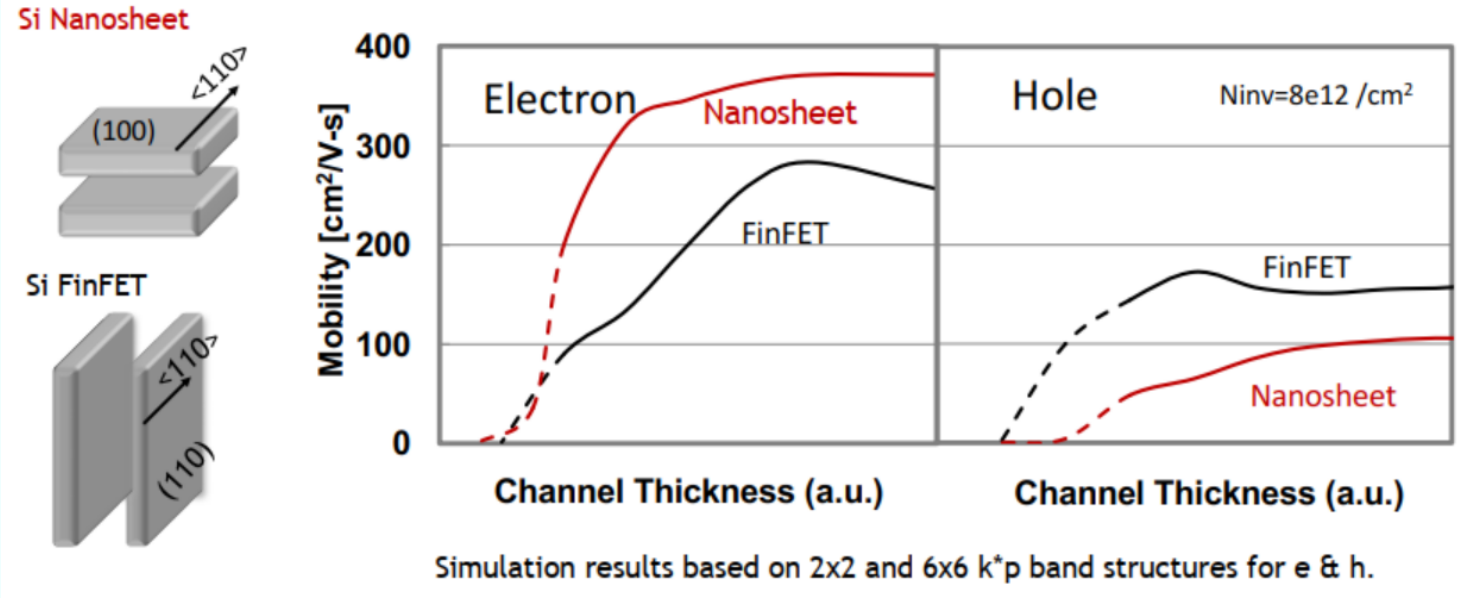
C.-E. Tsai *et al.*, VLSI, 2022, pp. 401.

- T_{body}=3nm has 11% delay reduction of 5nm (8 floors).
- For T_{body}=3nm, 8 floors have 30% delay reduction of 2 floors.

Outline

- Introduction
- Extensions
  - High Mobility Channels
  - Highly Stacked Channels
  - High-κ Gate Dielectric
  - Ultrathin Body
- **Beyond**
  - **TreeFET**
  - **CFET**

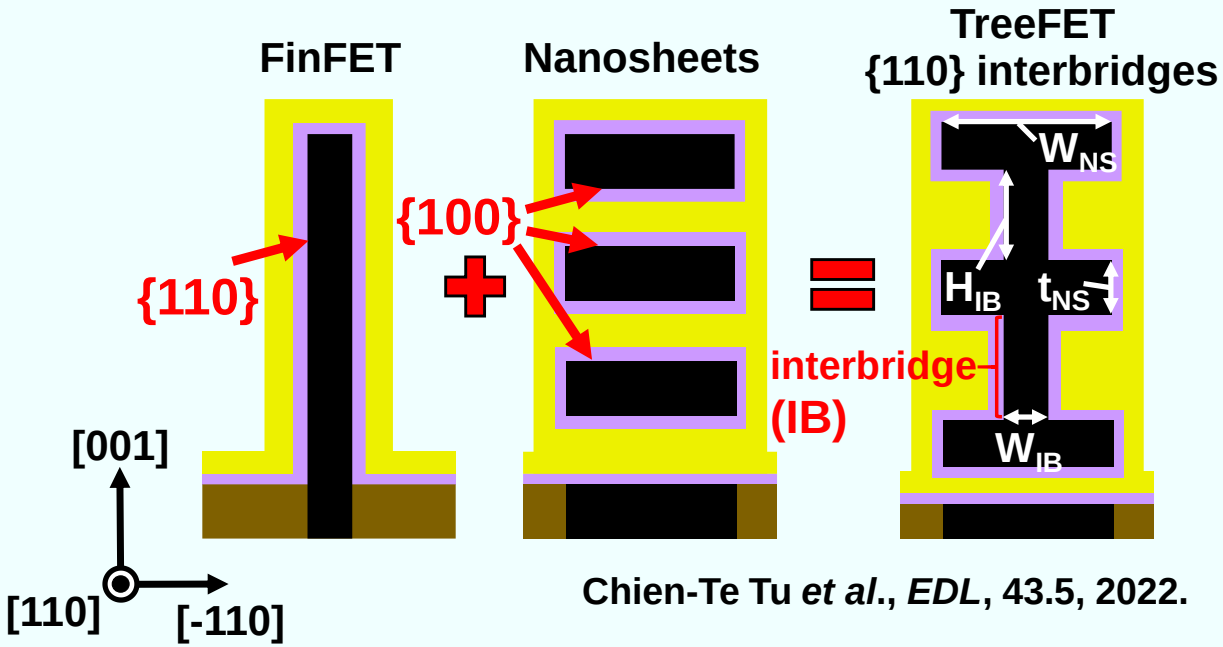
Nanosheet Mobility Mismatch



- μ_e/μ_h: Nanosheet > FinFET
- Nanosheet has more unbalanced electron and hole mobility than FinFET. ➔ potential design challenges of CMOS circuits

J. Cai, VLSI, 2021, SC1-1.

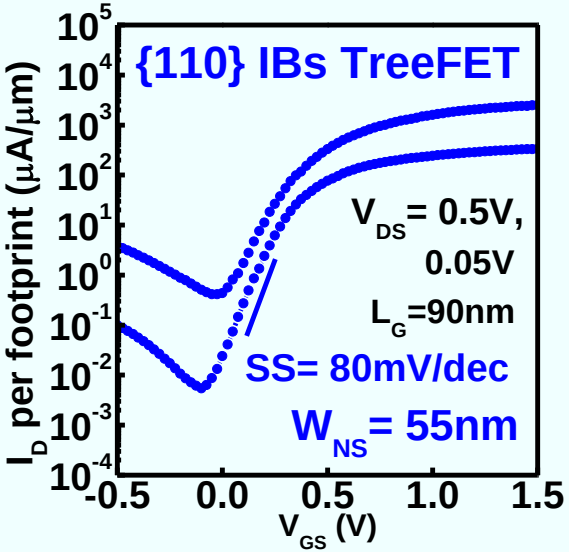
Novel TreeFET Transistor Architecture

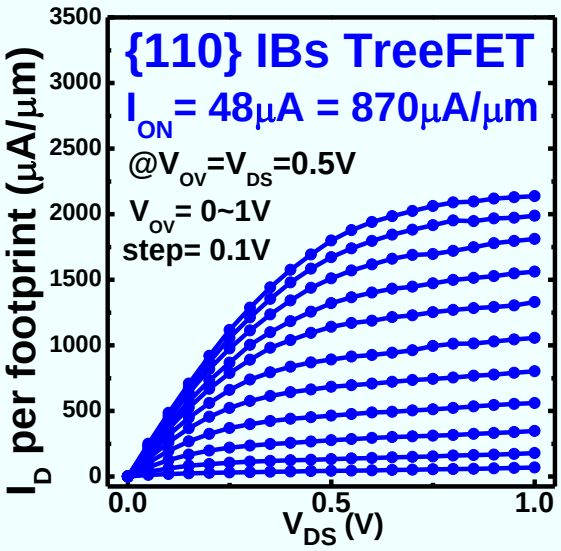


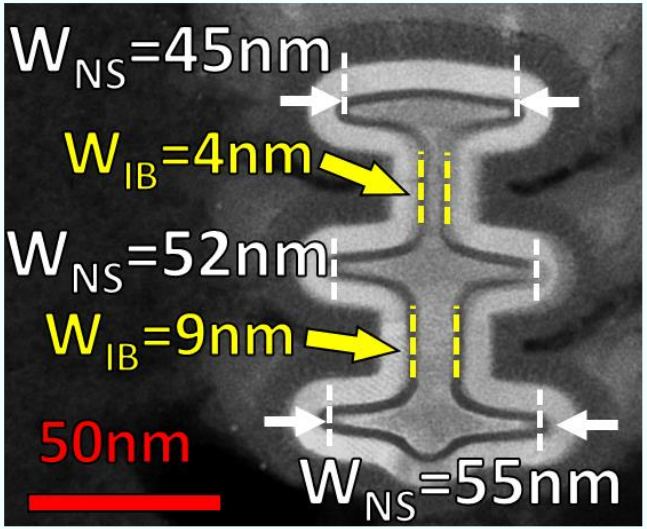
Chien-Te Tu *et al.*, *EDL*, 43.5, 2022.

- TreeFETs increase W_{eff} per footprint for high-performance devices beyond FinFET and nanosheets.
- TreeFET with {100} top/bottom surfaces favor the electron mobility of Si, while {110} interbridges favor the hole mobility.

TreeFET with {110} Straight Interbridges



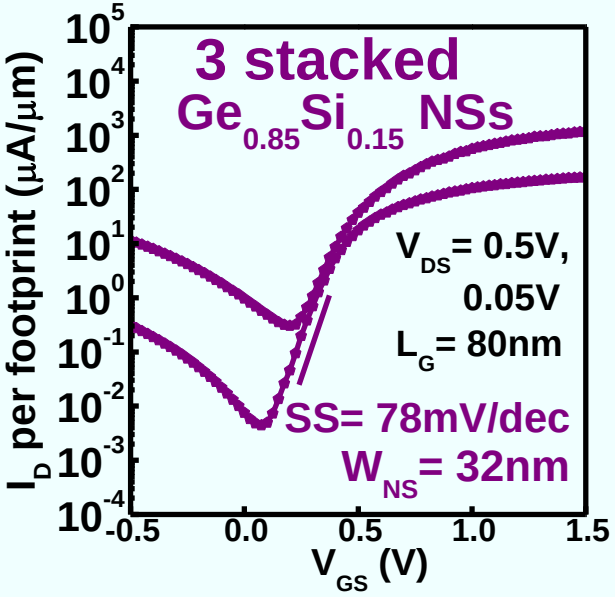


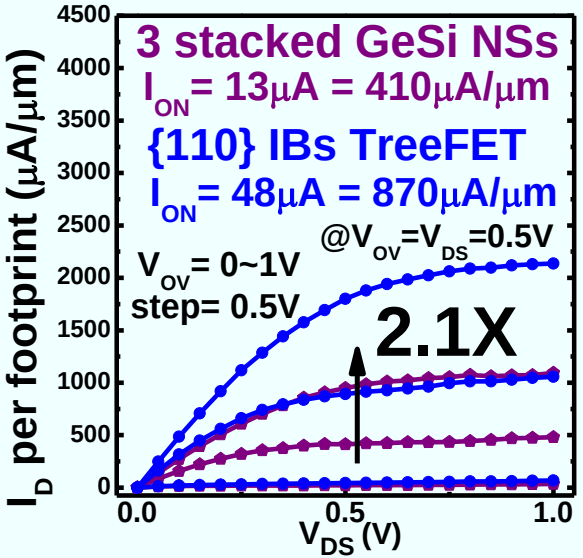


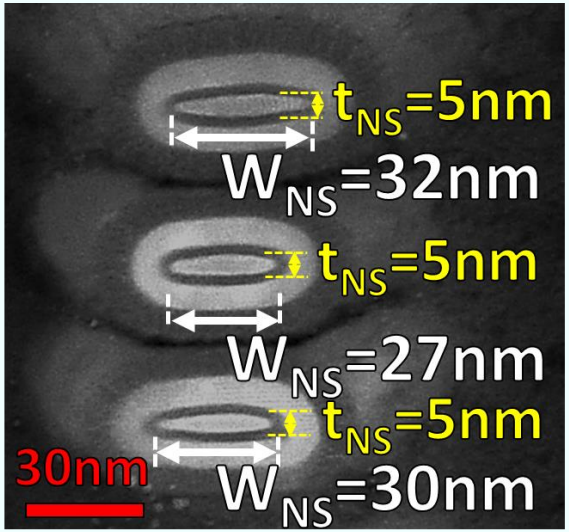
Chien-Te Tu *et al.*, *EDL*, 43.5, 2022.

- Low SS=80mV/dec at V_{DS}= 0.05V.
- I_{ON}=48μA per stack (870μA/μm per footprint) at V_{OV}=V_{DS}=0.5V.
- The channel cross section with W_{NS} = 45nm/52nm/55nm and W_{IB} = 4nm/9nm are confirmed by the TEM.

3 Stacked $Ge_{0.85}Si_{0.15}$ Nanosheets





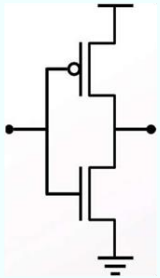


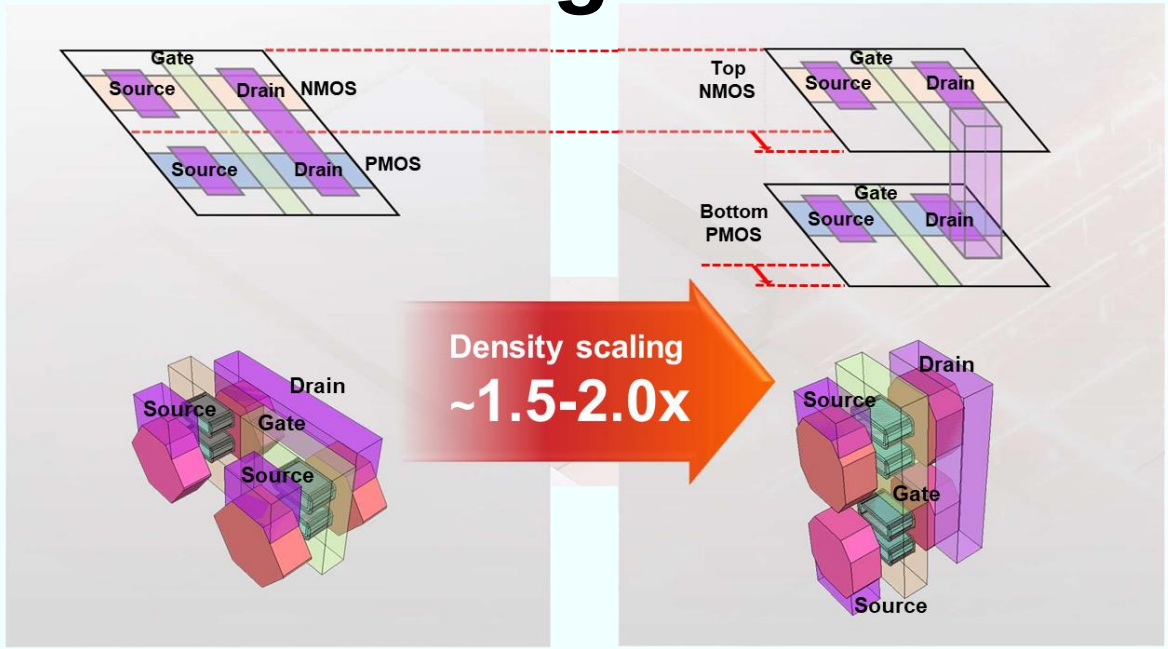
Chien-Te Tu *et al.*, *EDL*, 43.5, 2022.

- SS=78mV/dec at V_{DS}= 0.05V.
- The 2.1X I_{ON} per footprint improvement of the TreeFET is attributed to additional IB conduction.

CFET Scaling Benefit

Inverter

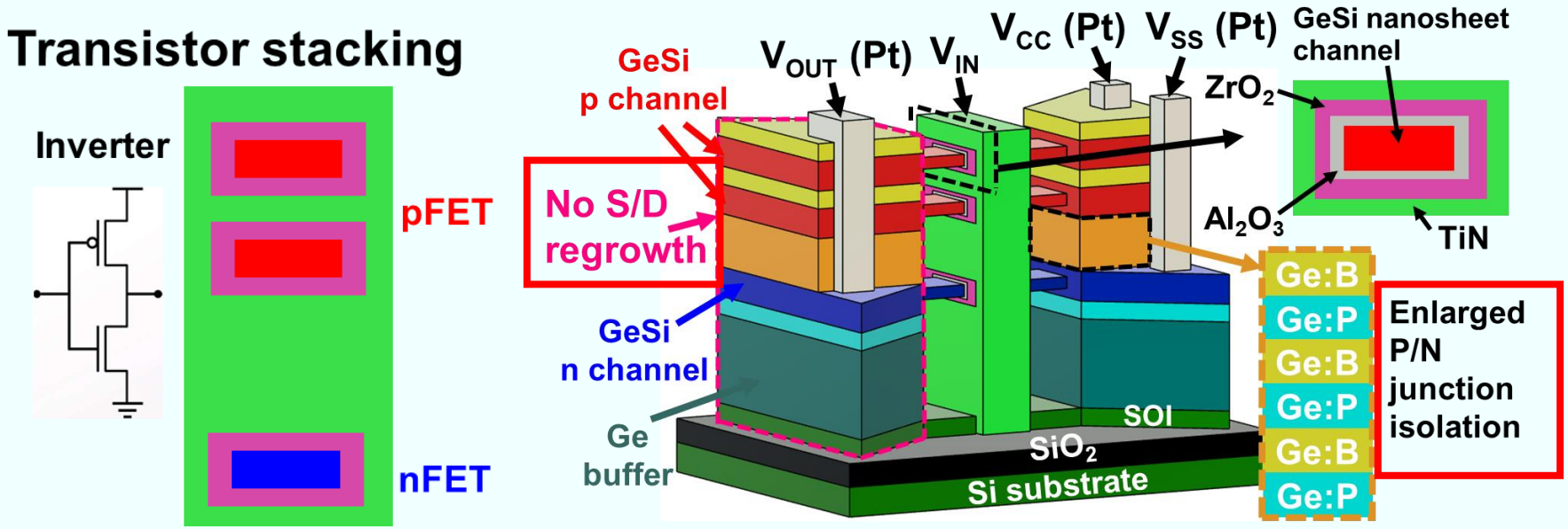




Source: Yuh-Jier Mii, VLSI, 2022, Plenary Session 2-2.

- **Folding a nFET on top of a pFET in CFET structure enables aggressive cell height scaling.**

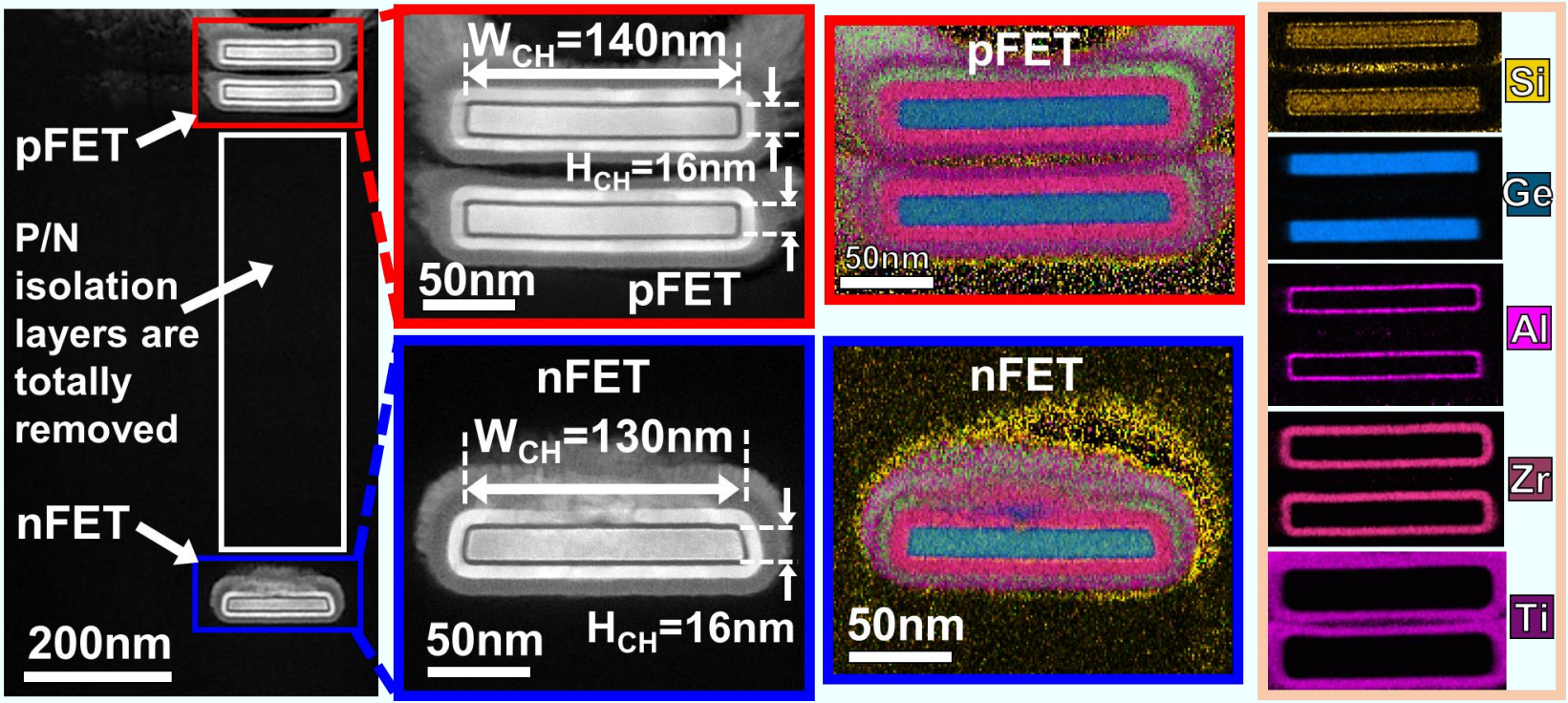
Monolithic 3D Self-aligned GeSi CFET



C.-T. Tu *et al.*, I*EDM*, 2022, pp. 479.

- Monolithic 3D self-aligned $Ge_{0.75}Si_{0.25}$ nanosheet CFETs with multiple **P/N junction isolation** to suppress the leakage current **without extra dielectric layers** are demonstrated.

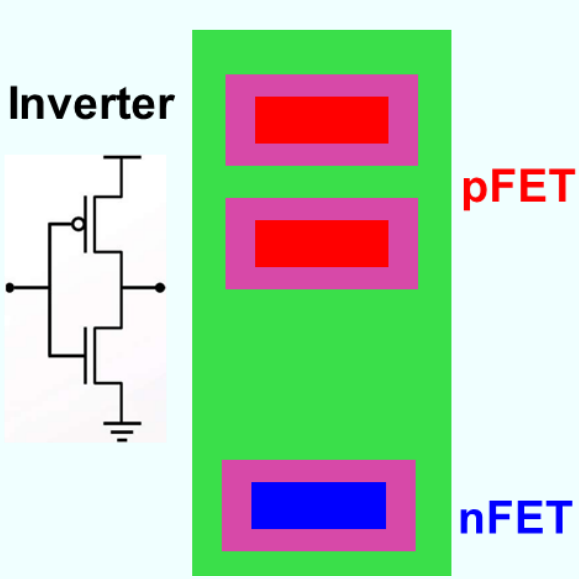
TEM and EDS Mapping of the GeSi CFET

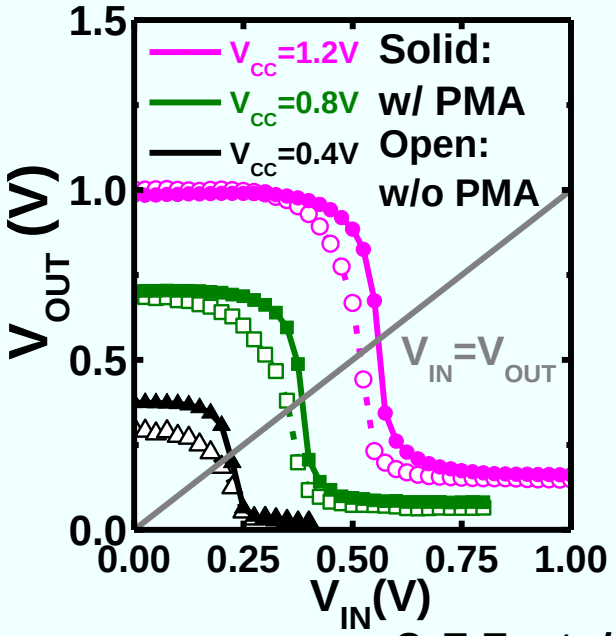


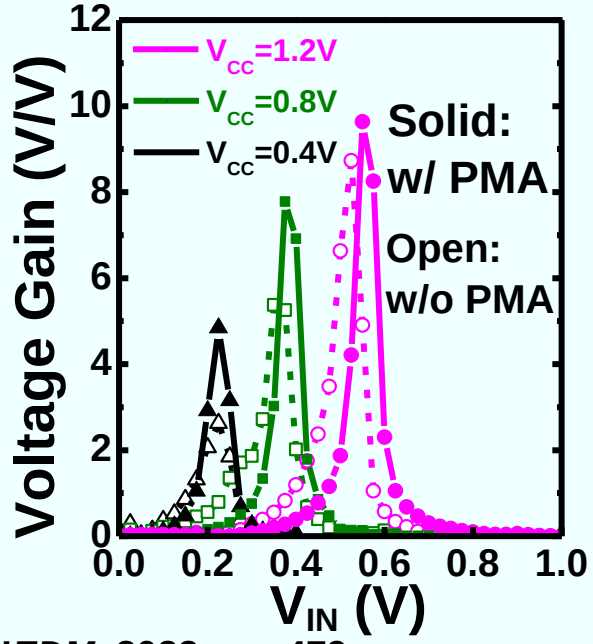
C.-T. Tu *et al.*, I*EDM*, 2022, pp. 479.

- **High inter-channel uniformity of the $Ge_{0.75}Si_{0.25}$ nanosheets**
- **Nanosheets are surrounded by gate dielectrics and *in-situ* TiN.**

Voltage Transfer Characteristics of GeSi CFET





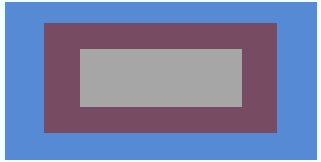


C.-T. Tu *et al.*, I*EDM*, 2022, pp. 479.

- **Common gate CFET structure is fabricated for a CMOS inverter with good voltage transfer characteristics after post-metallization annealing (PMA).**

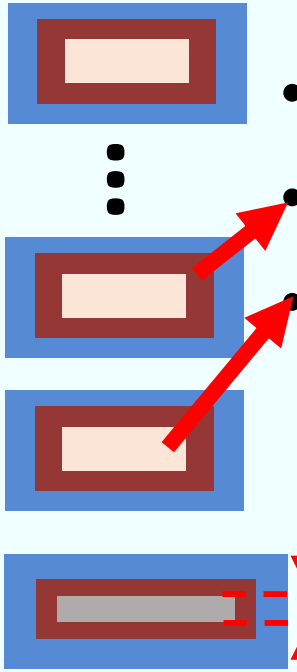
Summary

Si nanosheet



Extensions

Beyond

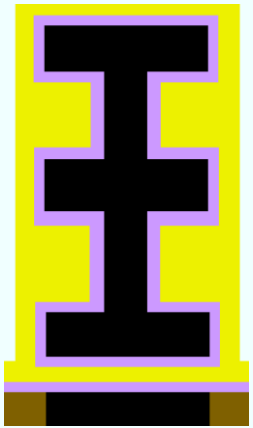


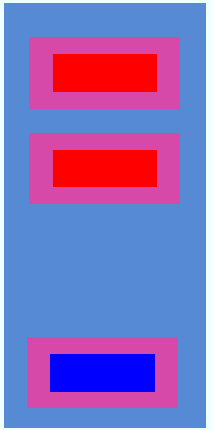
- Highly Stacked
- High-κ Dielectric
- High Mobility (GeSi, GeSn)
- Ultrathin Body (T_{body}< 5nm)

T_{body}

TreeFET

CFET





pFET

nFET

Acknowledgments

- NSTC (111-2218-E-002-040-MBK and 111-2622-8-002-001-), MOST (110-2218-E-002-030-), and MOE (NTU-CC-112L890901), Taiwan.
- The support by Taiwan Semiconductor Research Institute (TSRI), Taiwan, is also highly appreciated.

Thank you for your attention.

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