ICS 2023 | STDM

International Conference on Silicon Epitaxy and Heterostructures
International SiGe Technology and Device Meeting

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Foreword

Four years have passed since the last edition of the 2nd joint ICSi-ISTDM conference, held in Madison-Wisconsin in 2019. We all know the reason of such a long break; the breakout of the COVID 19 pandemic which hampered the organization of the 2021 edition. Now, our Community has the chance to meet again “in person”, the most effective way to interact with colleagues, young researchers and students.

The wish of gathering again is testified by the more than 140 abstracts submitted, which gave rise to a very rich program comprising 12 invited speakers, 70 regular talks and approximately 50 posters.

The topics of the conference echo the most recent advances of semiconductor science and technology. As CMOS technology is approaching the Ångstrom era, quantum technology makes its entrance as one of the more represented subjects at the conference. The latest results on telecom photonics are accompanied by a focus-shift on mid-infrared optoelectronic devices. Beside electronics and photonics, the program is completed by more research-oriented topics such as semiconductor based spintronics, thermoelectric generation, 2D materials and fundamentals aspects of epitaxy and strain relaxation.

The conference venue, the city of Como in Italy, has a long standing scientific tradition. This year we celebrate the 2000 years from the birth of Plinius the Elder, one of the greatest observer of Nature of classical antiquity, and the town is plenty of tribute to Alessandro Volta the inventor of the electric battery. The Organizing Committee is happy to welcome all the participants coming from 18 different countries.

Como May 17, 2023

Giovanni Isella

Monday, May 22nd

Session 1: Lasing in Group IV Materials

Time	Title	Speaker	Affiliation	Code
08:40 09:05	Strain-engineered GeSn light sources for photonic-integrated circuits	**Nam Donguk Invited speaker**	Nanyang Technological University	**S1 - 1**
09:05 09:30	Combining GeSn photonic layers with SiN stressor for advanced infrared laser designs and performances	**Moustafa El Kurdi Invited speaker**	Université Paris-Saclay CNRS	**S1 - 3**
09:30 09:45	GeSn/SiGeSn micro-rings laser diodes on Si	**Teren Liu**	Forschungszentrum Jülich	**S1 – 5**
09:45 10:00	Ex-situ n-type doped carrier-injection layers in direct bandgap GeSn LEDs	**Vincent Reboud**	CEA-LETI	**S1 – 7**
10:00 10:15	First indications for lasing in hexagonal Silicon-Germanium Nanowires	**Jos Haverkort**	Eindhoven University of Technology	**S1 – 9**

10:15 10:35 **Coffee break**

Session 2: Epitaxy I

Time	Title	Speaker	Affiliation	Code
10:35 11:00	Epitaxy of hexagonal SiGe	**Erik Bakkers Invited speaker**	Eindhoven University of Technology	**S2 - 1**
11:00 11:15	Isothermal heteroepitaxy of $Ge_{1-x}Sn_x$ structures for electronic and photonic applications	**Omar Concepción**	Forschungszentrum Jülich	**S2 - 3**
11:15 11:30	In-situ annealing for high crystal quality GeSn growth by solid-source molecular beam epitaxy	**Hui Jia**	University College London	**S2 – 5**
11:30 11:45	Epitaxy of hexagonal SiGe heterostructures: towards hexagonal SiGe quantum wells	**Wouter Peeters**	Eindhoven University of Technology	**S2 – 7**
11:45 12:00	N-type characteristics of undoped $Ge_{0.967}Sn_{0.033}$ fabricated on bulk n-Ge	**Noboru Shimizu**	Kyushu University	**S2 – 9**
12:00 12:15	Characterization of highly tensile strained SiP layer grown by epitaxy	**Joël Kanyandekwe**	Université Grenoble Alpes	**S2 – 11**
12:15 12:30	Nanosecond radiative lifetime of Hexagonal Ge	**Jos Haverkort**	Eindhoven University of Technology	**S2 – 13**

12:30 14:00 **Lunch break**

Session 3: Epitaxy II and defects

Time	Title	Speaker	Affiliation	Code
14:00 14:25	Atomistic modeling of extended defects in 3C-SiC/Si and Ge/Si heterostructures	**Anna Marzegalli Invited speaker**	Università Milano Bicocca	**S3 - 1**
14:25 14:40	Impact of Carbon to Silicon Ratio on the Crystal Quality of Epitaxially Grown 3C-SiC thin film on Si(001) substrate	**Freya Watson**	University of Warwick	**S3 - 3**
14:40 14:55	Mesoporous patterned silicon: a compliant substrate for defect free heteroepitaxy	**Alexandre Heintz**	Université de Sherbrooke	**S3 – 5**
14:55 15:10	Quantification of substitutional and interstitial carbon in thin SiGeC films using in-line X-Ray-Photoelectron spectroscopy	**Jeremy Vives**	STMicroelectronics Univ. Grenoble Alpes	**S3 – 7**
15:10 15:25	Background carrier concentration in intrinsic Ge-rich SiGe/Ge heterostructures integrated on Si(001)	**Henriette Tetzner**	IHP	**S3 – 9**
15:25 15:40	Modeling of Silicon Epitaxy on 300 mm Wafers and Analysis of Thickness Uniformity at Different Scales	**Andrey Smirnov**	Semiconductor Technology Research	**S3 – 11**
15:40 15:55	Emergence of Hyperuniformity in Self-Assembled SiGe Nanostructures	**Marco Salvalaglio**	Technische Universität Dresden	**S3 – 13**

15:55 16:10	Flash Annealing to Reduce the Threading Dislocation Density in Ge Films for CMOS-Compatible Monolithic Integration on Si	**Thomas Hagger**	EPFL	**S3 – 14**

16:10 16:30 **Coffee break**

Session 4: Quantum devices and materials

16:30 16:55	Quantum devices in germanium	**Andrea Hofmann Invited speaker**	Universität Basel	**S4 - 1**
16:55 17:20	Software for the simulation of SiGe devices and recent progress on Flying Electron Qubits	**Stefan Birner Invited speaker**	Nextnano	**S4 - 3**
17:20 17:35	Hole mobility in strained germanium exceeds 4×10^6 $cm^2V^{-1}s^{-1}$	**Maksym Myronov**	University of Warwick	**S4 – 5**
17:35 17:50	Growth of ^{28}SiGe heterostructures with oscillating Ge concentrations for spin qubits by molecular beam epitaxy	**Kevin-Peter Gradwohl**	IKZ Berlin	**S4 – 7**
17:50 18:05	Conductivity type transition in high-purity germanium bulk materials	**R. Radhakrishnan Sumathi**	IKZ Berlin	**S4 – 9**

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18:05 18:20	ASM SCHUNK XYCARB APPLIED MATERIALS ITALIA

Poster Session

Tuesday, May 23rd

Session 5: Spintronics

08:30 08:55	Spin injection, transport, and detection in Ge-based structures	**Carlo Zucchetti Invited speaker**	Politecnico di Milano	**S5 - 1**
08:55 09:10	Molecular beam epitaxy growth of ferromagnetic Heusler alloy films on SiGe(111) grown by Al-Ge-paste-induced liquid phase epitaxy	**Michihiro Yamada**	Osaka University	**S5 - 3**
09:10 09:25	Electric Field Manipulation of Spin Currents in Silicon Platforms	**Francesco Scali**	Politecnico di Milano	**S5 – 5**
09:25 09:40	Enhancement in Spin Transport Length in Strained n-$Si_{0.1}Ge_{0.9}$(111)	**Kohei Hamaya**	Osaka University	**S5 – 7**
09:40 09:55	Optical Spin Injection and Coherent Control in GeSn Semiconductors	**Gabriel Fettu**	École Polytechnique de Montréal	**S5 – 9**
09:55 10:10	Detection of magnetoresistance effect in all-epitaxial $Co_2MnSi/Ge/Co_2MnSi$ vertical spin-valve devices on Si(111)	**Atsuya Yamada**	Osaka University	**S5 – 11**
10:10 10:25	Towards Si-based Topology by Design: The Emergence of Quantum Phases in GeSn Heterostructures	**Fabio Pezzoli**	Università Milano Bicocca	**S5 – 13**

10:25 10:45 **Coffee break**

Session 6: Thermoelectrics and energy harvesting

Time	Title	Speaker	Affiliation	Code
10:45 11:10	Thermoelectric properties of GeSn alloys	**Dan Buca Invited speaker**	Forschungszentrum Jülich	**S6 – 1**
11:10 11:25	Temperature dependence of Raman scattering in Ge and GeSn layers	**Davide Spirito**	IHP	**S6 – 3**
11:25 11:40	Low-temperature Thermoelectric Properties of GeSn Alloys Films	**Masashi Kurosawa**	Nagoya University	**S6 – 5**
11:40 11:55	Polarized-resolved Raman scattering of epitaxially grown GeSn layers with various Sn content	**Agnieszka Anna Corley-Wiciak**	IHP	**S6 – 7**
11:55 12:10	Determining the Superiority of Cavity-Free Thermoelectric Generators Composed of GeSn and Si Wires	**Md Mehdee Hasan Mahfuz**	Waseda University	**S6 – 9**
12:10 12:25	Record-High Electron Mobility in Polycrystalline GeSn Thin Films on Insulators	**Koki Nozawa**	University of Tsukuba	**S6 – 11**
12:25 12:40	GeSn Mid-Infrared Thermophotovoltaic Cells for Power Beaming and Heat Conversion	**Gérard Daligou**	École Polytechnique de Montréal	**S6 – 13**
12:40 12:55	Piezo Resistivity of Epitaxial SiGe	**Yuji Yamamoto**	IHP	**S6 – 15**

12:55 14:00 **Lunch break**

Session 7: MIR photonics and plasmonics

Time	Title	Speaker	Affiliation	Code
14:00 14:25	Silicon Germanium integrated modulator and photodetector in the mid-IR wavelength range.	**Delphine Marris-Morini Invited speaker**	Université Paris-Saclay CNRS France	**S7 – 1**
14:25 14:40	Influence of thickness in Ge-based plasmonic antennas for the detection of human serum albumin	**Elena Hardt**	IHP Germany	**S7 – 3**
14:40 14:55	Ge-on-Si mid-infrared plasmonics	**Paolo Biagioni**	Politecnico di Milano Italy	**S7 – 5**
14:55 15:10	SiGe parabolic quantum wells for strong light-matter coupling at THz frequencies	**Monica De Seta**	Università Roma Tre Italy	**S7 – 7**
15:10 15:25	Mid-infrared nonlinear optics with Ge quantum wells	**Jacopo Frigerio**	Politecnico di Milano Italy	**S7 – 9**
15:25 15:40	Photonic Properties of Self-Assembled Semiconductor Microstructures	**Jacopo Pedrini**	Università Milano Bicocca Italy	**S7 – 11**
15:40 15:55	Exploitation of the natural instability in SiGe-based thin solid films for sensing and photonic applications	**Monica Bollani**	CNR-INFN Italy	**S7 – 13**
15:55 16:10	Suitability of highly Doped Groupe IV semiconductor for spectral narrow plasmonic MIR detection devices	**Fritz Berkmann**	Università La Sapienza Italy	**S7 – 15**

17:30 22:30 **City tour and social dinner**

Wednesday, May 24th

Session 8: Quantum devices and materials II

Time	Title	Speaker	Affiliation	Code
08:30 08:55	How Ge Affects the Valley Splitting in Si Quantum Wells	**Mark Friesen Invited speaker**	University of Wisconsin-Madison	**S8 – 1**
08:55 09:20	Reducing charge noise in quantum dots by using thin silicon quantum wells	**Davide Degli Esposti Invited speaker**	QuTech Delft	**S8 – 3**
09:20 09:35	Epitaxy of group IV semiconductors for quantum electronics	**Jean-Michel HARTMANN**	CEA-LETI	**S8 – 5**
09:35 09:50	Growth and characterization of $Ge/Si_{1-x} Ge_x$ planar heterostructures for spin qubits applications	**Arianna Nigro**	Universität Basel	**S8 – 7**
09:50 10:05	Optical Fingerprint of Subnanometer Interfacial Broadening in SiGe/Si Superlattices	**Anis Attiaoui**	École Polytechnique de Montréal	**S8 – 9**
10:05 10:20	X-ray Nanobeam Mapping of Lattice Strain Modulations caused by CMOS-Processed Gate Electrodes for Quantum Technologies	**Cedric Corley-Wiciak**	IHP	**S8 – 11**
10:20 10:35	Germanium wafers for strained quantum wells with low disorder	**Lucas Stehouwer**	QuTech Delft	**S8 – 13**

10:35 10:55 **Coffee break**

Session 9: Multilayer systems

Time	Title	Speaker	Affiliation	Code
10:55 11:20	Isotope- and strain-engineered germanium quantum wells	**Simone Assali Invited speaker**	École Polytechnique de Montréal	**S9 – 1**
11:20 11:35	Heterogeneous-integrated CFETs Realized by Layer Transfer Technology	**Wen Hsin Chang**	AIST Japan	**S9 – 3**
11:35 11:50	Electron Tomography Analysis of Ge/SiGe Asymmetrically Coupled Quantum Wells	**Ekaterina Paysen**	Paul Drude Institute	**S9 – 5**
11:50 12:05	Epitaxial SiGe/Si Multi-Layers for CFET Devices, Grown with a High Throughput Process	**Roger Loo**	IMEC	**S9 – 7**
12:05 12:20	Electron Emission Properties of Multiple-Stacked SiGe-Nanodots/Si Structures	**Katsunori Makihara**	Nagoya University	**S9 – 9**
12:20 12:35	Multi-micrometer thick Ge/Si-Ge heterostructures for integrated THz photonic devices	**Enrico Talamas Simola**	Università Roma Tre	**S9 – 11**
12:35 12:50	Advanced (opto-)electronic Si devices based on supersaturated epitaxial (Si)Ge layers with high Ge content	**Moritz Brehm**	Johannes Kepler University Linz	**S9 – 13**

12:50 14:00 **Lunch break**

Session 10: 2D, 1D and 0D epitaxy

Time	Title	Speaker	Affiliation	Code
14:00 14:25	1D Van der Waals Nanostructures: Harnessing Defects for New Functionality	**Peter Sutter Invited speaker**	University of Nebraska-Lincoln	**S10 – 1**
14:25 14:40	Van der Waals Epitaxy of Quasi Two-Dimensional GeTe-Rich $(GeTe)_m(Sb_2Te_3)_n$ Layered Alloys on Silicon	**Stefano Cecchi**	Università Milano Bicocca	**S10 – 3**
14:40 14:55	Electronic and morphological properties of the graphene/Ge(110) interface as a function of temperature	**Luciana Di Gaspare**	Università Roma Tre	**S10 – 5**
14:55 15:10	Applications of Graphene-Semiconductor Schottky Junctions to Reconfigurable Field-Effect Transistors	**Luca Anzi**	Politecnico di Milano	**S10 – 7**

Time	Title	Speaker	Affiliation	Code
15:10 15:25	Growth of Nd_2O_3 layers on germanium-rich, (111)-oriented SiGe layers	**Hannah Genath**	Leibniz Universität Hannover,	**S10 – 9**
15:25 15:40	Direct Exchange Interactions in Epitaxially Self-Assembled Heterostructures of Ternary Silicides on Si	**Ilan Goldfarb**	Tel Aviv University	**S10 – 11**

15:40 16:00 **Coffee break**

Session 11: Optoelectronic devices I

Time	Title	Speaker	Affiliation	Code
16:00 16:25	Ultra-fast (>250 GHz) integrated Ge photodetector	**Lars Zimmermann** Invited speaker	IHP	**S11 – 1**
16:25 16:40	Bandgap determination of lattice matched SiGeSn on Ge with pin diodes	**Daniel Schwarz**	IHT University of Stuttgart	**S11 – 3**
16:40 16:55	Monolitically integrated GaAs/Ge/Si visible-infrared photodetector	**Sergio Bietti**	Università Milano Bicocca	**S11 – 5**
16:55 17:10	Tellurium-hyperdoped Si for infrared optoelectronics	**Shengqiang Zhou**	Helmholtz-Zentrum Dresden-Rossendorf	**S11 – 7**
17:10 17:25	Integrated Ge LED for cryogenic quantum applications	**Michael Hack**	IHT University of Stuttgart	**S11 – 5**
17:25 17:40	Control of schottky barrier height at metal/polycrystalline Ge interfaces with fermi-level pinning alleviation	**Kenta Moto**	Kyushu University	**S11 – 7**

Thursday, May 25th

Session 12: Substrate engineering

Time	Title	Speaker	Affiliation	Code
08:30 08:55	Nano-Ridge Engineering - a Versatile Approach for Integration of III-V Devices on 300 mm Silicon	**Yves Mols Invited speaker**	IMEC	**S12 – 1**
08:55 09:10	Overview of Engi neered Germanium Substrate Development for Opto-Electronic devices	**Cho, Jinyoun**	Umicore	**S12 – 3**
09:10 09:25	Ge-on-Nothing as an alternative template to thin Ge wafers	**Roger Loo**	IMEC	**S12 – 5**
09:25 09:40	Evaluation of the physical properties of Ge-on-insulator based on Ge-on-Nothing and layer transfer	**Keisuke Yamamoto**	Kyushu University	**S12 – 7**
09:40 09:55	Unravelling the growth stages on porous substrate and formation of thin detachable Ge membranes	**Tadeáš Hanuš**	Université de Sherbrooke	**S12 – 9**
09:55 10:10	Low-Temperature Germanium Condensation process on SOI for sensing applications	**Luc Favre**	IM2NP Aix-Marseille Univ. CNRS	**S12 – 11**
10:10 10:25	Epitaxial growth of detachable Ge and GaAs/Ge membranes on mesoporous Ge substrate with the PEELER process	**Paupy Nicolas**	Université de Sherbrooke	**S12 – 13**

10:25 10:45 **Coffee break**

Session 13: Optoelectronic Devices II

Time	Title	Speaker	Affiliation	Code
10:45 11:10	A Review of Ge-on-Si Single Photon Avalanche Diode (SPAD) Photodetectors and Applications	**Douglas Paul Invited speaker**	University of Glasgow	**S13 – 1**
11:10 11:25	Strip-Width-Dependent Spectral Responsivity in a Waveguide Photodetector of Ge by Selective-Area Chemical Vapor Deposition on Si	**Yasuhiko Ishikawa**	Toyohashi University of Technology	**S13 – 3**

11:25 11:40	Understanding the Pseudo Planar Geometry Scaling in Ge-on-Si Single Photon Avalanche Diodes	**Ross Millar**	University of Glasgow	**S13 – 5**
11:40 11:55	Electrically tunable Ge-on-Si photodetector	**Andrea Ballabio**	Eye4NIR	**S13 – 7**
11:55 12:10	Photodetectors based on 3D self-assembled Ge and Si microcrystals	**Virginia Falcone**	Politecnico di Milano	**S13 – 9**
12:25 12:40	Position controlled integration of InP nanoislands with CMOS compatible Si using nanoheteroepitaxy approach	**Anagha Kamath**	Humboldt Universität	**S13 – 11**

12:40 13:00 **Closing remarks**

Poster Session

1	Integration of electro-optic barium titanate on Si and SOI	**Alexander Demkov**	University of Texas at Austin	**P – 1**
2	Impact of flows, temperature and pressure on the GeSn growth kinetics with a Ge_2H_6 + $SnCl_4$ chemistry	**Jean-Michel Hartmann**	CEA-LETI	**P – 3**
3	Efficient in-situ p- and n-doping of strained germanium tin epilayers	**Maksym Myronov**	University of Warwick	**P – 5**
4	In-Situ Strain Control of Silicon Carbide for 3D MEMS Applications	**Behzad Jazizadeh**	University of Warwick	**P – 7**
5	Local epitaxial growth of GaAs islands for monolithic integration on Si	**Andre Strittmatter**	Otto-von-Guericke-University Magdeburg	**P – 9**
6	Untwinned Si (111) on Al_2O_3 (0001) Grown by Thermal Laser Epitaxy	**Dongyeong Kim**	Max Planck Institute Stuttgart	**P – 11**
7	Si CVD Fundamentals Revisited	**Pierre Tomasini**	Applied Materials	**P – 13**
8	Growth and Optical Characterization of SiGe QDs on Si Nano-tips	**Diana Ryzhak**	IHP	**P – 15**
9	Deposition of Sn rich islands by Molecular Beam Epitaxy	**Ahsan Hayat**	BTU Cottbus–Senftenberg	**P - 17**
10	Gallium phosphide nanowires grown on SiO_2 by gas-source molecular beam epitaxy	**Songdan Kang**	Humboldt Universität zu Berlin	**P - 19**
11	Heteroepitaxial Growth of High Substitutional Sn-content $Ge_{1-x}Sn_x$ Layer Lattice-matched on InP Substrate	**Osamu Nakatsuka**	Nagoya University	**P - 21**
12	SiGe Fabrication on Si by Al induced liquid phase epitaxy using screen-printing Al-Ge paste	**Shota Suzuki**	Toyo Aluminium K.K.	**P – 23**
13	Fabrication of crack-free strained SiGe/Ge multiple quantum wells on Ge-on-Si(111) by the patterning method	**Kentarou Sawano**	Tokyo City University	**P – 25**
14	Van der Waals heteroepitaxy of Xene 2D Processing and characterization on graphene/6H-SiC	**Adam Arette-Hourquet**	Aix Marseille University	**P - 27**
15	From Plastic to Elastic Relaxation in SiGe Microcrystals	**Andrea Barzaghi**	Politecnico di Milano	**P - 29**
16	Effects of Phosphorous Doping Density on Thin Ge Layers Grown on Si(001)	**Xueying Yu**	University College London	**P - 31**
17	Uniform CVD of graphene on 2’’ SiC wafer	**Chiara Mastropasqua**	Université Côte d’Azur, Aix-Marseille Université	**P - 33**
18	InGaN Growth by PAMBE in the Intermediate Composition Regime on Silicon	**Federico Cesura**	Università di Milano Bicocca	**P - 35**

19	Ge/Si Vertical Separate Absorption Charge Multiplication (VSACM) Avalanche Photo Diodes (APDs): Epitaxial Growth and Impact of Post-Epi Anneal on Excess Carrier Lifetime	**Roger Loo**	IMEC	**P - 37**
20	Influence of Ga concentration on the local atomic structure and material properties of Ga-doped $Si_{0.36}Ge_{0.64}$ epitaxial layers	**Gianluca Rengo**	KU Leuven, IMEC, FWO – Vlaanderen	**P - 39**
21	Modeling of optical absorption in SiGe QCSE modulators including excitonic effects	**Heorhii Yehiazarian**	Nextnano GmbH	**P - 41**
22	Electrical Characterization of Sputtered Monocrystalline GeSn Thin Films for Photodetection Applications	**Louise Webb**	EPFL	**P - 43**
23	Plasmonic TiN nanohole arrays for on-chip refractive index sensors	**Sebastian Reiter**	BTU Cottbus–Senftenberg	**P - 45**
24	Extended short-wave infrared GeSn photodetector realized by ion implantation and flash lamp annealing	**Shuyu Wen**	HZD-Rossendorf Chinese Academy of Sciences	**P - 47**
25	TiN nanotriangle arrays in a CMOS-compatible fabrication process for open plasmonic cavities	**Jon Schlipf**	BTU Cottbus–Senftenberg	**P - 49**
26	Spin pumping in GeSn alloys	**Emanuele Longo**	CNR-IMM	**P - 51**
27	Investigation of the Schottky barrier height in germanium-aluminum heterostructure devices	**Anna Invernici**	Università di Milano Bicocca	**P - 53**
28	Diode characteristics and room temperature EL emission for strained SiGe/Ge quantum well LEDs	**Shuya Kikuoka**	Tokyo City University	**P - 55**
29	Modeling of Selectorless RRAM with Transient Characteristics for Computing-in-Memory Application	**Jia-Wei Lee**	National Cheng Kung University	**P - 57**
30	Impact of substrate doping on the performance of vertically illuminated Ge-on-Si photodetectors	**Raffaele Giani**	Politecnico di Milano	**P - 59**
31	Controllable charge distribution and dynamics of conduction electrons around metallic nanowires	**Ngoc Duy Nguyen**	University of Liège	**P - 61**
32	Structure and electrical property of polycrystalline silicon trap-rich layer by in-situ annealing	**Xing Wei**	Shanghai Institute of Microsystem and Information Technology	**P - 63**
33	First Principles Calculation of Alloy Scattering Parameters and their Effect on the Mobility of GeSn	**Kevin Sewell**	Tyndall National Institute	**P - 65**
34	Voids detection in trenches filled with N-type doped silicon	**Justine Lespiaux**	Univ. Grenoble Alpes, CEA-LETI	**P - 67**
35	Radiative Carrier Lifetime in GeSn Mid-Infrared Emitters	**Gérard Daligou**	École Polytechnique de Montréal	**P - 69**
36	Synthesis of relaxed $Ge_{0.9}Sn_{0.1}$/Ge by nanosecond pulsed laser melting	**Enrico Di Russo**	Università degli Studi di Padova	**P - 71**
37	Strain Analysis of Ge Quantum Well on a Si_xGe_{1-x} barrier	**Alicia Ruiz-Caridad**	Universität Basel	**P - 73**
38	Polarization-Induced Fano Resonances in All-Dielectric SWIR Metasurface	**Anis Attiaoui**	École Polytechnique de Montréal	**P - 75**
39	The layer transfer of Ge-lattice-matched SiGeSn epitaxial films	**Tatsuro Maeda**	AIST	**P - 77**
40	Post growth thermal treatments of Silicon-Germanium-Tin-on-insulator alloys	**Oliver Steuer**	HZD-Rossendorf	**P - 79**
41	Fabrication of Si/Ge microbridges based on Ge-on-Si (110) and effect of bridge length	**Takahiro Inoue**	Tokyo City University	**P - 81**
42	Processing of the stacked n-Si channel over p-Si channel for fabrication of CFETs	**Guang-Li Luo**	Taiwan Semiconductor Research Institute	**P - 83**

43	Revealing very low thermal conductivity of germanium tin epilayers at room-temperature	**Sabur Ayinde**	University of Warwick	**P - 85**
44	Study and reduction of dislocation densities in $Si_{1-x}Ge_x$ virtual substrates for quantum computing applications	**Lucas Stehouwer**	QuTech	**P - 87**
45	Towards anisotropically strained in-plane Ge nanowires for quantum transport experiments	**Orson van der Molen**	Eindhoven University of Technology	**P - 89**
46	Germanium/Silicon Core Shell Nanowires for Spin/Hole Qubits Fabricated by Chemical Vapour Deposition	**Nicolas Forrer**	University of Basel	**P - 91**
47	Germanium Quantum Wells for Spin Qubit Application	**Stefano Calcaterra**	Politecnico di Milano	**P - 93**
48	Optical study of isotopically pure ^{70}Ge-on-Si films	**Ian Colombo**	Università di Milano Bicocca	**P - 95**
49	CVD-grown Nuclear Spin-depleted ^{70}Ge/SiGe Heterostructures	**Patrick Daoust**	École Polytechnique de Montréal	**P - 97**
50	Optimizing Germanium Quantum Wells for Spin Qubits	**Daniel Chrastina**	Politecnico di Milano	**P - 99**

Strain-engineered GeSn light sources for photonic-integrated circuits

Donguk Nam[1]

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1. Introduction

Recently, silicon photonics has emerged as the leading technology for building a practical, fault-tolerant quantum computer. Utilizing the same manufacturing techniques used for electronic chips containing billions of components, silicon photonics enables the creation of millions of quantum photonic devices on a tiny chip to increase the number of photonic qubits for quantum computing. This unique ability of silicon photonics has spurred global competition among universities and companies to develop key quantum photonic devices and circuits. Despite the successful demonstrations of many of the components required for quantum computing, creating an integrated light source—a crucial piece for preparing resources—remains a significant challenge because efficient light emission in silicon-compatible materials is fundamentally prohibited. In this work, we will share our recent results in developing GeSn lasers that can potentially become a strong candidate to complete the missing link for fully integrated photonic circuits.

2. Main Results

We will discuss various types of GeSn lasers that can emit single-mode lasing when pumped well above the lasing threshold, as shown in Figure 1. First, we will discuss strain-relaxed GeSn-on-Si microdisk lasers achieving improved thermal conductivity. By comparing two microdisk laser devices with and without interfacial defects, we also show the significance of defect management in lowering the lasing threshold. 1D photonic crystal cavity GeSn-on-insulator (GeSnOI) lasers attaining a small form factor will also be presented. By harnessing controlled laser annealing, we present the possibility of precisely controlling the level of tensile strain in the gain medium, which determines the emission wavelength. We also demonstrate the alignment of the emission wavelengths from multiple lasers that initially emit different colors. GeSn nanomechanical lasers that can be electrically driven with a radio frequency drive will also be discussed, while strong cavity resonances from a single GeSn nanowire will also be presented. Lastly, we will also show our recent efforts in bonding GeSn layers onto emerging material platforms including aluminum nitride (AlN), which has recently attracted much attention for quantum photonics applications.

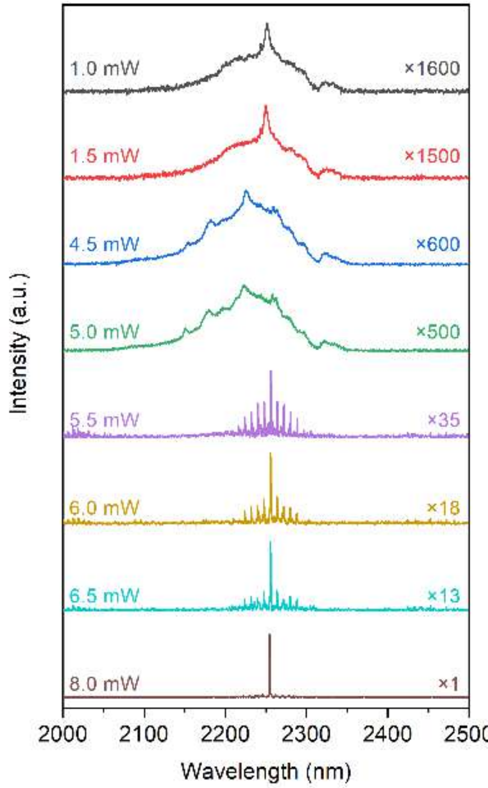

Fig. 1. Evolution of the emission spectra from GeSn lasers from spontaneous emission (top) to single-mode lasing (bottom).

3. Conclusions

In this work, we discuss our latest results on various types of GeSn lasers and also present the bright future for building integrated photonic quantum processors that may be enabled by GeSn lasers.

Acknowledgements

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2017-01). This work is also supported by the iGrant of Singapore A*STAR AME IRG (A2083c0053). This research is also supported by the National Research Foundation, Singapore and A*STAR under its Quantum Engineering Programme (NRF2022-QEP2-02-P13). The authors would like to acknowledge and thank the Nanyang NanoFabrication Centre (N2FC).

Combining GeSn photonic layers with SiN stressor for advanced infrared laser designs and performances

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1. Introduction

Since the first demonstration of GeSn lasing in 2015 [1], researchers aim to enhance performances and enable the integration of Group-IV lasers in Si photonics ICs. However, researchers struggled with material defects and lack of optimized design in terms of optical confinement and thermal management. Moreover, the lasing thresholds were in the MW/cm^2 range when operation temperature increased above 150 K. The highest GeSn lasing temperature was, without defect removal, 273 K [2],[3]. The community was thus confronted to a glass ceiling that prevented room temperature operation despite the successful growth of high crystalline quality GeSn alloys with Sn contents above 16at.%. High tin contents result in large directness of the band structure, e.g. the energy difference between the direct and the indirect electronic state of the conduction band. A large bandgap directness yields an efficient injection of Γ–state carriers needed to generate optical gain up to room temperature. Advances in design and growth of GeSn/SiGeSn heterostructures led to electrically pumped GeSn lasers [4],[5], with operation temperatures of at most 100K, however. We describes here strategies than can be used to improve material gain properties and which enabled us to reach room temperature optically pumped lasing [6],[7]. A high Sn content of 17at.% was used in one case. In another case, a lower Sn content of 14at.% was combined with tensile strain engineering to reach room temperature lasing. In both cases, room temperature lasing was reached thanks to a new strategy relying on GeSn-on-insulator (GeSnOI) technology and possibly the use of a SiN stressor layer as an optical cladding. This platform offers some advantages over conventional approaches, including strain engineering, interface defect removal, optimized optical confinement and better thermal management [8].

2. GeSnOI technology

Figure 1 shows a 500 nm thick GeSn layer grown on a Ge Strained Relaxed Buffer (SRB), itself on silicon. The layer thickness was well above the critical thickness for plastic relaxation of GeSn on Ge. This resulted in a dense array of misfit dislocations mostly present in the first 100 nm away from the GeSn/Ge interface. This thick GeSn layer on a Ge SRB was coated with a SiN/Al bi-layer then bonded onto a host Si substrate to obtain a GeSnOI stack (Figure 1). The aluminum layer yielded a better heat evacuation away from the GeSn layer while the SiN layer with an in-built compressive stress of -1.7 GPa acted as a stressor layer after cavity patterning..

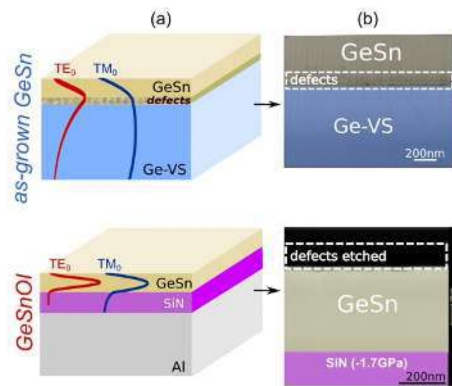

Fig. 1. cavities (a) Schematic diagram of as-grown GeSn on Ge-SRB and GeSnOI stacks together with TE and TM mode profiles of a confined optical wave at a 2.4 µm wavelength. (b) X-TEM images of as-grown GeSn on Ge SRB and of a GeSnOI stack.

After bonding, the Si substrate used to grow the Ge SRB was removed by selective etching. The Ge SRB and the defects at the GeSn/Ge interface were subsequently removed, resulting in a thinner GeSn layer of better crystalline quality.

Thanks to that defective region etching, we expect carrier recombination dynamics to be improved and light emission to be more efficient. Additionally, the GeSn/SiN index contrast is high enough to provide excellent optical confinement of TE and TM polarized modes, favoring the modal overlap between laser modes and GeSn gain medium.

Microdisk mesa cavities were fabricated from the

GeSnOI layer using standard processing. The emission from the disk was analyzed under pulsed optical pumping at telecom wavelength for various temperatures and excitation powers. 300K lasing at a 3.5 µm wavelength was achieved with GeSnOI micro-disks with, as a gain material the GeSn 17% layer. Meanwhile, the maximum laser temperature was 270 K only with similar Sn content GeSn microdisks fabricated directly from GeSn/Ge stacks. Several assets of the GeSnOI technology enabled such an achievement, namely the improved carrier lifetime due to defects removal, optimized thermal cooling and optical confinement [8].

2. Tensile strain engineering

We also demonstrated that room temperature lasing could be also reached for lower Sn content gain media thanks to tensile strain engineering. GeSnOI mesa disks with 14at.% of Sn (Fig. 2-a) were under-eteched, and a second SiN stressor layer was deposited over the whole mesa, resulting in an all-around stressor geometry (Fig.2-b). This approach enabled to transfer about 1.5% of biaxial tensile strain to the GeSn layer, that was originally slightly compressively strained, by -0.5%. The resulting 1% tensile strain was homogenously distributed inside the GeSn strained micro-disk. As shown in Figure 2c, the photoluminescence emission of that strained micro-disk was redshifted by 100 meV with respect to the emission of the as-grown layer on to the SiN stressor.

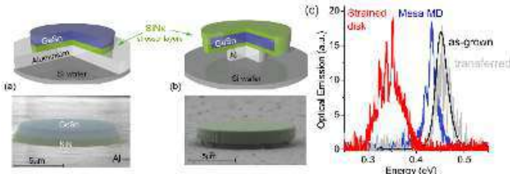

Fig. 2. Schematics and SEM images of (a) mesas and (b) strained microdisks fabricated from a GeSn 14% thick layer grown on Ge-SRB on silicon. (c) Photoluminescence spectra of 9 µm diameter mesas and strained micro-disks compared to PL spectra of blanket GeSnOI and as-grown GeSn layer.

Meanwhile, the PL emission of mesa disks was redshifted by 20 meV compared to blanket GeSn and GeSnOI. Such a redshift was assigned to a vanishing of the residual compressive strain in the as-grown GeSn layer. Emission from the mesa disk was analyzed under pulsed excitation, with lasing up to 265 K. As a comparison, the strained micro-disk with an all-around stressor geometry lased up to 300K (Fig. 3). The improved gain was assigned to the beneficial impact of tensile strain on the band structure, e.g. the directness increase and the lift of the valence band degeneracy making the Light-Hole band the top valence conduction band [7].

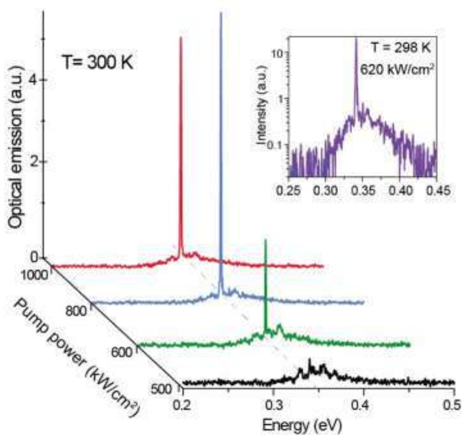

Fig. 3. Power dependence of the PL spectra of 1% tensile strained 9 µm diameter GeSn micro-disk at 300 K. The Sn content of the GeSn alloy is 14%. Inset: 298 K spectrum in log scale.

3. Conclusions

We showed that GeSnOI technology enabled to reach room temperature lasing with GeSn and had a bright future for the integration of efficient infrared emitters on silicon chip.

Acknowledgement:

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GeSn/SiGeSn micro-rings laser diodes on Si

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1. Introduction

Monolithically integrated light sources on Si are the key elements toward energy efficient Si-photonic integrated circuits for on-chip optical communication [1]. Si photonics ICs are considered for future quantum computing systems with optical input-outputs co-integrated on CMOS chips. Recently, Si photonics has been also proposed as a technology platform for neuromorphic computing, thanks to its large bandwidths and multiplexing capabilities. While Si, par excellence an electronics material is not an efficient light emitter, the laser research activity has focused on strain engineering of Ge and its group IV alloys.

Optically stimulated GeSn laser emission at low temperature has already been demonstrated in 2015 [2]. Recent progress on epitaxy and layer transfer technology allowed to reach room-temperature laser emission from high-Sn content GeSn layers or by inducing tensile strain in moderate-Sn containing active material [3-5]. Both approaches lead to a decrease of the energy separation between the Γ and the L-valleys of the conduction band, thus increasing the “directness” of the band energy landscape and, consequently, the radiative recombination efficiency. However, achieving GeSn lasers by electrical pumping is a much more challenging task, as it requires more elaborated layer stacking as well as suitable solutions for high quality electrical contacts.

In this work we present different electrically pumped GeSn laser diodes emitting at a wavelength of 2.7 µm and with a threshold current density at 5K of 10 kA/cm^2.

2. Layer stacking, Material/Device Fabrication and Strain Engineering

Laser diodes were fabricated from SiGeSn/GeSn double heterostructure (DHS) grown on Ge virtual substrate (VS) on 200 mm Si wafers. The Sn content the GeSn gain medium was chosen to be 14 at.% based on previous optical pumping experiments that offered laser emission up to 300K [5]. 3D design sketch of the micro-ring laser is presented in Figure 1. A set of rings with outer radius from 5 µm to 40 µm and inner radius from 0 to 18 µm (depending on outer radius) have been fabricated. The under-etch in the Ge-VS below the GeSn rings, obtained by selectively isotropic CF_4 etching, promotes the relaxation of the rest compressive strain built-in during the epitaxial growth. This leads to an increase of the Γ to L-valley energy difference in the $Ge_{0.86}Sn_{0.14}$ gain medium. The under-etched region is where the whispering gallery modes (WGM) are formed. Comparing with microdisk structure, the center hole of the micro-ring is supposed to reduces the pumped volume and consequently laser threshold.

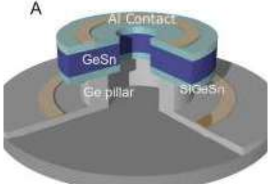

Fig. 1. a) Sketch of a SiGeSn/GeSn micro-ring laser.

3. Laser emission characterization

The microdisk/micro-ring laser diodes were pumped using a pulsed laser-driving source and measured with a Bruker vertex 80v FI-IR spectrometer with a minimum resolution of 1 cm^{-1}. Long pulse (> 250 µs) electroluminescence (EL) was first measured in large disk starting from a current density of 0.2 kA/cm^2. By scaling down the diode geometric dimension and increasing the current density together with decreasing the pulse width, laser emission was successfully

obtained.

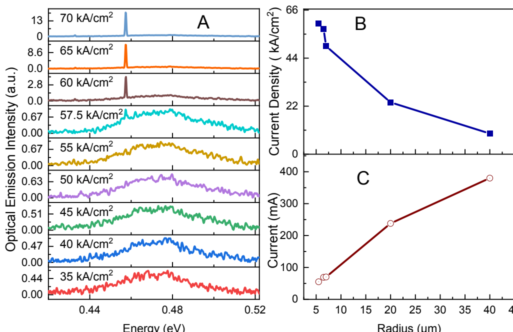

Fig.2: a). EL spectra of a microring laser diode (outer radius 6.5 µm, hole radius 2 µm) under different current density (50kHz, pulse width 100 ns). b,c). Threshold current density/ current of the laser diode under different radius.

Fig. 2a shows exemplarily the EL spectra evolution with the pumping current density for a micro-ring cavity with diode the outer radius of 6.5 µm and inner hole radius of 2 µm, under current pulse of 100 ns. As observed, above a current density of 57.5 kA/cm^2 whispering cavity modes starts forming. After threshold, the FWHM of the optical emission collapse from 43 meV to < 1 meV (measured with resolution 4 cm^{-1}) together with an exponential increase of the intensity. These features are a clear prove of a transition from spontaneous emission to laser emission.

At longer current pulses, degradation of laser emission was been observed in several other diodes, which assumed to be related with the thermal budget of the suspended micro-ring structure. Therefore, for all the micro-ring lasers discussed below, the pumping condition were kept as 100 ns pulse, 50 kHz repeating rate. Under these pumping conditions, all diodes with different geometrical dimensions have shown laser emission at a wavelength of ~2.7 µm with a FWHM of ~250 µeV (~2 nm for wavelength). Several small dimeter diodes were measured at higher temperature, offering laser signal up to 90 K where the diode suffered mechanical/structural damage. [6]. Here we would mainly discuss about sample with larger radius.

3.1 Laser threshold versus outer radius dimension

The threshold current density at 5 K of the micro-ring diodes was reduced from 60 kA/cm^2 to 10 kA/cm^2 when the outer radius increases from 5.5 µm to 40 µm respectively. Data analyses show that the threshold current is proportional to the inverse of the radius instead of the device area. This could be attributed to a lower suspended GeSn/pillar areas ratio, which lead to better cooling of the diode, or the higher carrier recombination rate at the edge of micro-rings due to the improved strain relaxation for larges micro-rings.

3.2. Laser threshold versus GeSn undercut depth

Batches of sample with the same substrate, same fabrication process but slightly different undercut were fabricated. For diodes with same outer radius (5.5 µm and 7 µm) and 1.5 µm undercut showed clear lower thresholds (43.5 kA/cm^2 and 37.5 kA/cm^2) versus (60 kA/cm^2 and 50 kA/cm^2) for 1.2 µm undercut. This indicates that the elastic strain in the GeSn gain medium play a critical important role in determining the micro-ring laser threshold.

3. Conclusions

In summary, we present a set of electrically pumped micro-ring lasers based on SiGeSn/ $Ge_{0.86}Sn_{0.14}$/ SiGeSn double heterostructures grown on Ge buffer layers on Si wafers. The laser effect is studied for a large range of geometrical dimensions. The laser emission is at 2.7 µm, with the minimum current density at threshold of 10 kA/cm^2.

These results show the promising future of GeSn laser sources as key elements for achieving all-CMOS technology based on-chip photonic systems.

Acknowledgements

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Ex-situ n-type doped carrier-injection layers in direct bandgap GeSn LEDs

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1. Introduction

(Si)GeSn group-IV materials foster great attention in the Si photonics community as they are compatible with Complementary Metal Oxide Semiconductor (CMOS) fabrication technology. Bulk, unstrained GeSn alloys with tin (Sn) concentrations higher than 8% have a direct instead of a weakly indirect bandgap for pure Ge. Increasing the Sn content and tensile strain reduce the GeSn bandgap and improve its bandgap directness [1]. NIR, SWIR and MWIR spectral range operations are achievable with GeSn alloys, notably for gas detection. Since 2015, the lasing thresholds of optically pumped GeSn have continuously shrunk and their operating temperatures increased. Recently, room temperature lasing was achieved [2,3]. Nowadays, efforts are directed towards electro-optical devices, such as electrically pumped lasers and photodetectors. It is then interesting to use fabrication processes as flexible and similar to CMOS ones as possible.

Here, we report our first LEDs with ex-situ n-type doped GeSn carrier-injection layers. In particular, we compare direct band gap $Ge_{0.87}Sn_{0.13}$ LEDs with ex-situ doping of the n-type GeSn caps to similar LEDs with in-situ n-type doped Ge caps.

2. Recrystallization of thick implanted GeSn layers

The first challenge was to activate phosphorus ions implanted into an intrinsic GeSn layer. A few years ago, other groups have already investigated the ex-situ doping of GeSn with rear side rapid flash lamp annealing lasting a few milliseconds [4]. Here, we have used instead Ultraviolet Nanosecond Laser Annealing (UV-NLA) with a 308 nm laser wavelength and pulses lasting only 160 ns.

All GeSn stacks were grown here on Ge-buffered 200 mm Si(001) wafers in a Reduced Pressure Chemical Vapor Deposition (RP-CVD) reactor. We started this study by growing a 480 nm thick $Ge_{0.92}Sn_{0.08}$ layer then finding the optimal annealing conditions to reconstruct a GeSn crystal amorphized by P^+ ion implantation. Several laser Energy Densities (EDs) were tested and multiple morphological characterisations used to evaluate the crystalline quality [5]. The dispersion of the phonon frequencies of the Ge–Ge bond was monitored for different incident energy densities. **Fig. 1** shows Raman spectra for as-grown, ion-implanted, and ion-implanted then annealed GeSn layers.

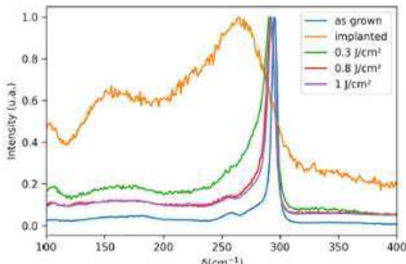

Fig. 1/ Normalized Raman spectra for as-grown GeSn, implanted GeSn, and implanted GeSn annealed at ED = 0.3, 0.8, and 1.0 J/cm^2.

As the incident ED increased, GeSn melted deeper and the Ge–Ge peak became narrower and more intense, demonstrating, together with other techniques (not shown here), the total recrystallization of GeSn close to the surface. We concluded that in specific laser annealing conditions [5], implanted GeSn layers could successfully be re-crystallized, with complex tin spatial redistribution, however.

3. GeSn LEDs fabrication

UV-NLA re-crystallisation was then used on a $Ge_{0.87}Sn_{0.13}$ stack with an ex-situ n-type doped GeSn layer (named Sample A, **Fig. 2a**), to fabricate a LED. This LED was compared to another LED with an in-situ doped Ge:P injection layer (Sample B, **Fig. 2b**). 1.5 µm thick Ge strain-relaxed buffers (SRBs) capped with 1 µm thick in-situ p-type doped Ge:B layers ($[B^+] = 3x10^{19}$ cm^{-3}) were used in both cases to mitigate the lattice parameter mismatch between Si and GeSn.

Sample A: a 740 nm thick intrinsic $Ge_{0.87}Sn_{0.13}$ layer was grown at 325°C with Ge_2H_6 + $SnCl_4$ on top of the p-type Ge layer. Phosphorus was then ion implanted in the top 120 nm of the direct band gap $Ge_{0.87}Sn_{0.13}$ active layer. During UV-NLA, the layer amorphized by ion implantation was recrystallized with the same orientation as the undamaged seed layer underneath.

Sample B: A similar 620 nm thick intrinsic $Ge_{0.87}Sn_{0.13}$

layer was also grown at 325°C on the p-type Ge layer. The active layer was capped at 350°C with 50 nm of Ge:P ([P^+] = $3x10^{19}$ cm^{-3}).

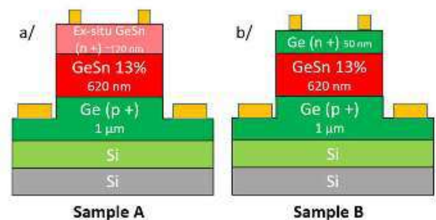

Fig. 2 a/ Schematic cross-sections of GeSn heterostructures grown on Ge-buffered 200 mm Si wafers a/ with an ex-situ n-type doped GeSn carrier-injection layer (Sample A), **b/** an in-situ n-type doped Ge cap (Sample B).

A and B stacks were then processed into mesas with various geometries using conventional microfabrication steps. A $Ni_{0.9}Pt_{0.1}$ alloy capped with TiN was used to benefit from efficient electrical contacts. Metals were deposited at room temperature by magnetron sputtering. A stanogermanide nickel-platinum intermetallic was then formed using some rapid thermal annealing at 350 °C [6].

3. A comparison between in-situ and ex-situ n-type doped injection layers on $Ge_{0.87}Sn_{0.13}$ LEDs

Electrical measurements were performed at room temperature with a voltage varying from -1V to 1V. **Fig. 3a** shows I(V) characteristics for samples A and B. The dark current of the laser-annealed heterostructure (sample A) was significantly higher than that of sample B. It may be explained by the presence of a higher defect density in the recrystallized layer.

The electroluminescence (EL) signal was collected from the top of the device with a commercial mid-infrared optical microscope and analysed with a Fourier transform infrared (FTIR) spectrometer. A careful spectral calibration of the spectrometer photodetectors was performed beforehand [7]. The EL signal was detected with an N_2-cooled InSb photodetector. The current density of plugged devices was set to 0.5 kA/cm² to record electroluminescence spectra **(Fig. 3b)**. A 5-fold decrease in the EL intensity was measured for sample A compared to sample B, most probably due to the complex Sn distribution in the ex-situ doped n-type injection layer and the presence of localized defects. Such results, the first for ex-situ doped GeSn LEDs to the best of our knowledge, nevertheless open up new pathways for (Si)GeSn device integration in Si/Ge photonics platforms.

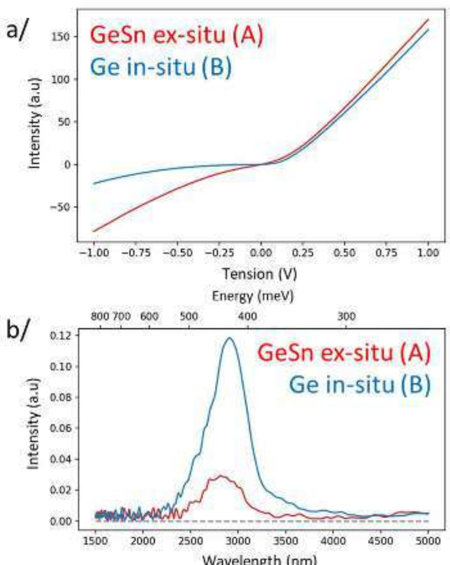

Fig. 3 a/ I(V) characteristics for samples A and B vertical p-i-n junctions versus applied voltage, **b/** Room temperature electroluminescence spectra for samples A and B LEDs.

5. Conclusion and perspectives

We investigated crystalline lattice reconstruction in phosphorus-implanted thick GeSn layers. We showed, under specific conditions, the feasability of recrystallizing the amorphized crystal. MIR direct band-gap light-emitting diodes were fabricated with $Ge_{0.87}Sn_{0.13}$ active layers and ex-situ GeSn:P or in-situ Ge:P contact layers on top. We showed for the first time to our knowledge functional LEDs with an ex-situ doped GeSn injection layer. Investigations are underway to improve their performances for a use in gas sensor cells.

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First indications for lasing in hexagonal Silicon-Germanium Nanowires

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1. Introduction

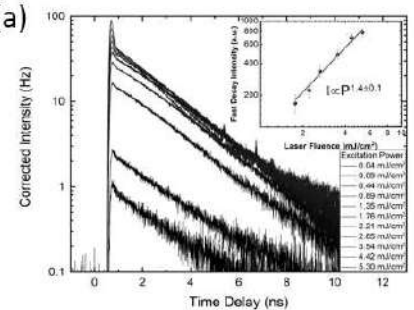
The search for a silicon (or germanium)-based laser has been an important focus in photonics for many years. As both silicon (Si) and germanium (Ge) are known to be indirect semiconductors, a Si-compatible light emitter was still lacking. Recently, we have experimentally shown that hexagonal Silicon-Germanium (hex-SiGe) features a direct bandgap [1]. By growing the crystal in the hexagonal phase, the L-point in the cubic Brillouin zone is folded onto the Γ-point of the hexagonal phase. This creates a direct bandgap for hex-(Si)Ge with Ge contents above 60% with efficient band-to-band emission up to room temperature reported between 0.35eV and 0.7eV [1]. If stimulated emission and lasing are achieved, it will open up many possible applications for integrating hex-SiGe for sensing and telecommunication light sources onto Si-photonics [2].

2. Silicon-on-insulator cavity design.

The hex-SiGe is grown using the crystal transfer method with the core being wurtzite-GaAs, which is used as a template to grow a hex-SiGe shell around it [3,4]. A material can achieve lasing if the resonator around it surpasses the lasing threshold,

$$\Gamma g_{th} = \alpha - 1/(2L)\ln(R_1 R_2), \quad (1)$$

where Γ is the modal overlap between the optical mode and the gain material, g_{th} is the gain threshold of the medium, α is the optical losses per unit length, L is the cavity length, and R_i the reflectivity of the end facets of the cavity. The nanowire geometry itself can act as a resonator, however, the current morphology of the nanowires is not yet of high enough quality, giving rise to too many optical losses. Thus to improve the optical confinement, we fabricate an external cavity around the NW, which will lower the gain threshold, making it easier to reach the conditions for lasing. We use a microstadium resonator as an external cavity, where the NW is placed on top [5]. The stadium cavities were fabricated from a silicon-on-insulator (SOI) wafer and the NWs were subsequently transferred onto the stadium using a mechanical transfer tip. The mode of the NW couples to the microstadium due to the low refractive index contrast between the two materials (silicon and hex-SiGe). In a microstadium resonator, several stable scar modes emerge from a pattern of unstable chaotic modes, which then couple to the Fabry-Pérot modes of the NW. From Finite Difference Time Domain (FDTD) simulations, we obtain a Q-factor of $Q > 2000$ for the NW-stadium coupled cavity.



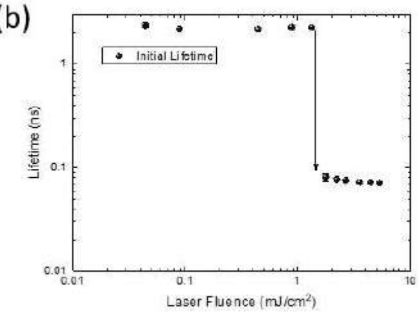


Fig. 1 (a) Photoluminescence time decay from a hex-SiGe NW on a Si-microstadium for different excitation densities. At the highest excitation densities, a very fast initial decay peak ($\tau = 72ps$) can be seen on top of the slow spontaneous decay ($\tau = 2ns$). The inset shows the intensity of the fast decay peak as function of excitation density, highlighting the superlinear increase of this fast component. (b) The initial photoluminescence lifetime as function of the laser fluence. A clear transition between a slow decay, and a fast decay is observed at a laser fluence of $P = 1mJ/cm^2$ which we attribute to the transition towards the ASE regime.

3. Stimulated emission.

The NW-stadium sample is measured in a micro-photoluminescence (micro-PL) setup with a femtosecond pulsed laser with an excitation

wavelength of 1032 nm and a repetition rate of 40 MHz as the excitation source. The sample is investigated with both time-resolved and spectrally-resolved PL experiments. In Fig. 1a, the time-resolved PL signal of a NW on a stadium cavity is shown as a function of the laser fluence. At low excitation densities, the time-decay is governed by a single exponential with a carrier lifetime of $\tau = 2$ ns, which is the spontaneous lifetime previously observed in hex-SiGe [1]. At excitation densities above $P > 1$ mJ/cm^2, the initial lifetime is much faster at $\tau = 72$ ps, shown in Fig. 1b. Initially the fast decay of 72 picoseconds dominates, when lower carrier densities are reached the decay transitions back into the spontaneous emission. This behavior has been described before as stimulated emission in GaAsP NW lasers [6]. The lifetime decreases from 2 ns down to 72 ps, which indicates that the stimulated emission rate in hex-SiGe is nearly 30x larger than the spontaneous emission rate. Moreover, the superlinear behavior of the intensity of the decay with laser fluence is a further confirmation that it is stimulated emission [6,7], shown in the inset of Fig. 1a. So, while Fig. 1 does not provide clear proof for coherent lasing, we clearly observe Amplified Spontaneous Emission (ASE), the precursor to lasing.

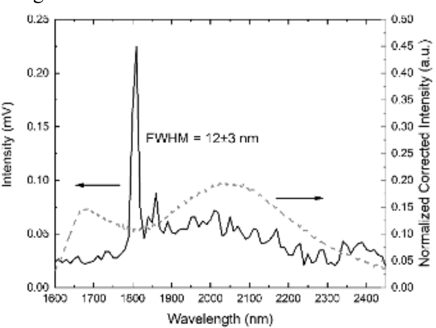


Fig. 2. The spectrum of a single hex-SiGe NW on a microstadium resonator (full curve) at an high excitation density of 3 mJ/cm^2. The sharp peak provides a first indication for the onset of lasing. The dashed curve shows the PL from an ensemble of the same NWs, this shows that the lasing peak is in the same region as the spontaneous PL.

In Fig. 2, a spectrum is shown of the hex-SiGe NW on a stadium cavity measured using a substractive double monochromator with an extended InGaAs detector. The dashed curve is the spectrum at low excitation density for an ensemble of hex-SiGe NWs, showing the fundamental transition centered at 2050 nm as well as the onset of the second valence band transition around 1700 nm. The full curve is the spectrum of a single NW on a stadium cavity recorded at a high laser fluence of 3mJ/cm^2. We observe that the NW-stadium spectrum consists of a single peak with a FWHM of 12 nm which is limited by the monochromator resolution. This sharp spectrum is generally considered as proof for lasing. Unfortunately, the nanowire was damaged by the high laser excitation, excluding more measurements on this nanowire

4. Conclusions.

In conclusion, the combined observation of ASE in the TRPL signal and the observation of a spectrally sharp peak at high excitation, shows that hex-SiGe NWs on a microstadium cavity are exhibiting stimulated emission and are approaching lasing. With further improvement of the optical cavity and better cooling of the hex-SiGe nanowire, a hex-SiGe laser can be realized, opening the way to a silicon-compatible laser.

Acknowledgements

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Epitaxy of hexagonal SiGe heterostructures

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1. Introduction

Silicon and germanium cannot emit light efficiently due to their indirect bandgap, hampering the development of Si-based photonics. However, alloys of SiGe in the hexagonal phase are predicted to have a direct band gap. In this work, we have grown hexagonal SiGe shells on wurtzite GaAs and/or GaP template wires using the crystal structure transfer method [1]. We reveal a new type of defect in this SiGe material system, which is identified as I_3 [2]. We study the formation mechanism using in-situ transmission electron Microscopy [3], and their structural and electronic properties [2]. We find that the defects form when the growth front is roughened, which happens at higher material fluxes and/or lower growth temperatures.

We study the growth kinetics as a function of the SiGe composition, and focus on the growth of planar hexagonal SiGe layers and heterostructures, such as quantum wells.

We show efficient light emission from hexagonal SiGe, up to room temperature, accompanied by a short radiative life time of around a nanosecond, the hallmarks of a direct band gap material [4]. The band gap energy is tunable in the range of 0.35 till 0.7eV opening a plethora of new applications.

The next challenge is to demonstrate lasing from this new material. For this we have to address two challenges: 1) the wires are not terminated by flat facets, which could be used to confine the light within the wire. Therefore, we design and fabricate external cavities with different geometries. 2) the thermal contact between the wire and the substrate. We observe that for high excitation powers, the wires are evaporated. This issue is addressed by more resonant excitation, and increasing the thermal contact. Above a certain excitation threshold, we observe a strong reduction of the radiative lifetime and a superlinear increase of the emission intensity, first indications of amplified spontaneous emission (ASE).

2. Conclusions

Hexagonal SiGe is an interesting new material for light-emitting applications, but a number of important open challenges have to be addressed.

Acknowledgements

We would like to especially thank funding from Europe's Horizon program OptoSilicon (964191), the Dutch foundation for Scientific Research (NWO), and the Bosch foundation.

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Isothermal heteroepitaxy of $Ge_{1-x}Sn_x$ structures for electronic and photonic applications

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1. Introduction

The epitaxy of Group-IV heterostructures, monolithically integrated with the current silicon CMOS technology, constitutes a highly demanded field of research. Optical devices are already available in the near-/mid-infrared region of the electromagnetic spectrum, starting with the experimental demonstration of the emission of an optically GeSn-pumped laser [1]. In addition, Sn-alloys are currently used in electronic devices due to their high electrical conductivity [2] or in thermoelectric research due to their low thermal conductivity [3]. Also, exotic fields of physics such as spintronic [4] and low dimensionality [5] are studied based on Group-IV materials.

The epitaxy of Sn-heterostructures is challenging due to the low solid solubility of Sn and the large lattice mismatch between Sn and the other commonly used group-IV compounds, Ge and Si. This leads to the need for growth far from thermodynamic equilibrium conditions, resulting in epitaxial films of high crystalline quality [1]. However, achieving control of the thickness and Sn content of the alloy while maintaining sharp, well-defined interfaces is challenging. This is even more critical, as the Sn content in the alloy increases, which is necessary for most practical applications.

Different approaches have been explored. For example, decreasing the growth temperature in steps or growing thick films enhances the incorporation of Sn. However, the main limitation of these methods is that once the maximum desired Sn content is reached, its decrease without destroying the epitaxy of the underlying layers or without the unwanted effect of Sn segregation is a challenge.

In this work, we propose a simple method, in which without any change in the growth temperature and the reactor pressure, while keeping the ratio between the precursor flows constant, the Sn content in the alloy can be varied in a wide range, by tuning the total flow of the N_2 carrier gas. The proposed method is put into practice with the design of different heterostructures aimed at electronic, spintronic, and photonic device applications.

2. Experimental Methods and Results

2.1. Isothermal growth conditions

Epitaxy of Sn-based alloys was performed in an industry-compatible reduced-pressure chemical vapor deposition reactor. Before the deposition, the 200 mm wafers were cleaned ex-situ with HF steam using an automated cleaning tool. GeH_4 and $SnCl_4$ were used as precursors. The films were deposited on a 300 nm-thick Ge buffer layer grown before the $Ge_{1-x}Sn_x$ layer deposition (one epitaxy run) and a previously grown 1.5 µm-thick, high quality, cycle-annealed Ge/Si(001) virtual substrate (VS) to decrease the lattice mismatch between the film and the silicon substrate.

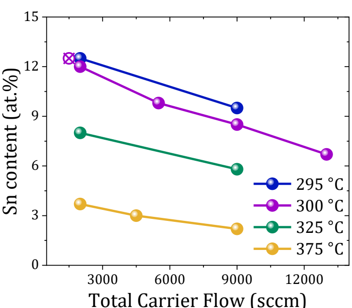

Fig. 1. Sn content as a function of total carrier gas flow at different growth temperatures showing similar behavior.

All the layers were grown under a reactor pressure of 60 mbar and p_{GeH4}/p_{SnCl4} = 1100. Fig. 1 shows the Sn content obtained as a function of the total N_2 flux. Regardless of the growth temperature, it can be observed that a decrease in the carrier gas flow leads to a considerable increase in the incorporation of Sn into

the alloy. The decrease in the total flow of the carrier gas proportionally increases the partial pressure of the precursors, resulting in a decrease in the velocity of the gas, that is, the retention time of the reactive precursors in the reactor increases. As a consequence, the GeH_x radicals that interact with the $SnCl_4$ molecule will increase on the surface.

2.2. *$Ge_{1-x}Sn_x$ heterostructures for electronic and photonic device applications*

The method was extended to the design of different heterostructures (Table I). For example, at 300 °C, a decrease in the total flow results in an increase of the Sn content from 12 to 15 at.% (*Structure I*). The design of this structure is intended for vertical MOSFET devices. If the opposite route is considered, that is, increase the carrier gas flow in steps, the result is *Structure II* with 3 layers of GeSn showing a decrease in Sn content. The design is optimal for ultra-low-power electronics through tunneling field-effect transistors.

Table I. Total carrier gas (Q_T), Sn content, and thickness (d) of different heterostructures. The "bottom layer" corresponds to the layer grown on the Ge buffer layer while the "top layer" is the last grown layer.

		Q_T (sccm)	Sn content (at.%)	d (nm)
Structure I	Top layer	2000	15	60
	Bottom layer	9000	12	100
Structure II	Top layer	13000	8	60
	Middle layer	9000	9	75
	Bottom layer	2000	11	90
Structure III	5 x MQW			
	- Wells	2000	15.5	30
	- Barriers	15000	9.5	12
	Buffer layer	9000	13	40
	Bottom layer	2000	12	310

Finally, the combination of both structures results in a heterostructure with multiple quantum wells (Fig. 2). Such a design reduces the injection threshold current allowing better performance at high temperatures of the light sources. In the TEM micrographs, the high crystallinity of the epitaxial stack is observed without defects in the interfaces between the different GeSn layers.

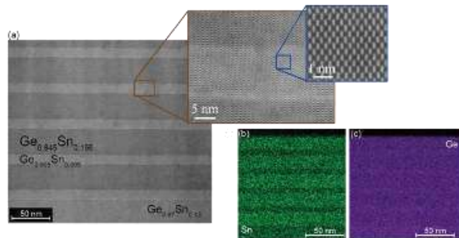

Fig. 2. (a) High-resolution TEM and (b-c) energy-dispersive X-ray spectroscopy high-angle annular dark-field (EDS-HAADF) micrographs of a strained $Ge_{0.845}Sn_{0.155}/Ge_{0.905}Sn_{0.095}$ multiple QW heterostructure (*Structure III*).

3. Conclusions

A simple technical epitaxial growth approach was proposed to isothermally largely vary Sn incorporation in the Ge lattice only by tuning of the N_2 carrier gas flow. The method was applied to design heterostructures for MQW light emitters and nanoelectronic FETs.

Acknowledgments

The authors would like to thank to Patric Bernardy and Karl-Heinz Deussen for their experimental and technical support.

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In-situ Annealing for High Crystal Quality GeSn Growth by Solid-Source Molecular Beam Epitaxy

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1. Introduction

Group-IV alloy GeSn has been receiving increasing research interests in recent years as a promising candidate for applications in Si-based optoelectronic devices including light emitting devices and long-wavelength photodetectors thanks to its bandgap tuneability. However, the low solid solubility of α-Sn in Ge and the metastable nature of GeSn alloy have led to the rough surface and Sn segregation during the epitaxial growth as well as adding thermal limits to the device fabrication. In addition, the large lattice mismatch of 14.2% between α-Sn and Ge induces large heteroepitaxial strain rendering the epitaxial growth of high quality GeSn even more difficult. Therefore, low temperature growth [1], Ge and compositional-graded GeSn buffer layers [2] are generally adopted. Thermal annealing as a well-studied method to reduce residual strain and improve crystal quality has also been substantially investigated for GeSn alloy. However, the thermal budget for GeSn annealing is relative lower than most of semiconductor materials, and the maximum temperature before Sn segregation is highly dependent on the strain and defect level within the layers. Although ex-situ post-growth annealing was reported to improve the crystal quality of GeSn by several groups [3-5], to the best of our knowledge it has not been applied in-situ to facilitate GeSn buffer layer growth for high-quality GeSn active layer.

2. Experiment and initial results

In the current work, in-situ low-temperature annealing (LTA) was performed for the growth of a multi-layer compositional-graded GeSn buffer growth on Ge-buffered Si substrate by solid-source molecular beam epitaxy (MBE). An optimised 500 nm Ge layer was first grown on Si as a buffer layer, followed by a nominal 150 nm $Ge_{0.97}Sn_{0.03}$ grown at 150 °C and annealed at a low temperature of 180 °C. Then a 150 nm $Ge_{0.95}Sn_{0.05}$ layer and a 100 nm $Ge_{0.92}Sn_{0.08}$ layer were grown also at 150 °C and annealed at 170 °C and 160°C, respectively. A reference sample without any LTA was grown for comparison. During the growth, reflection high-energy electron diffraction (RHEED) was used for surface monitoring. An abrupt change of RHEED pattern from spotty patterns symbolising three-dimensional growth dynamics to 3 × 1 streaky patterns was observed just entering the LTA step, as can be seen in Fig. 1(b). The LTA temperature needs to be well controlled to avoid Sn surface segregation.

After the growth, atomic force microscopy (AFM), high-resolution x-ray diffraction (XRD) and transmission electron microscopy (TEM) have been performed for the analyses of surface morphology, composition and strain, and crystal quality, respectively. The XRD results in Fig. 1(a) demonstrates Sn compositions close to the nominal values. 100 μm² Atomic force microscopy images show a surface roughness reduction of ~ 1 nm for the growth with LTA and the root-mean-square roughness of the multi-stack GeSn/Ge/Si is only 1.94 nm. Reciprocal space maps show that the GeSn stacks are pseudomorphically grown on Ge/Si. Multi-quantum-well structure was grown on LTA treated composition-graded GeSn/Ge/Si and TEM investigations show well-defined quantum well profile and good crystal quality, as shown in Fig. 2.

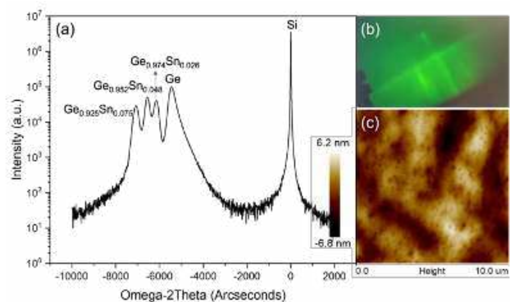

Fig. 1. (a) (004) X-ray diffraction result of the epitaxially grown in-situ annealed compositional-graded GeSn/Ge/Si stack. (b) Reflection high-energy electron diffraction image of the nominal $Ge_{0.92}Sn_{0.08}$ layer after annealing at 160°C. (c) 100 μm² Atomic force microscopy image showing the surface of the multi-layer GeSn/Ge/Si structure grown with the low-temperature annealing. The root-mean-square roughness is 1.94 nm.

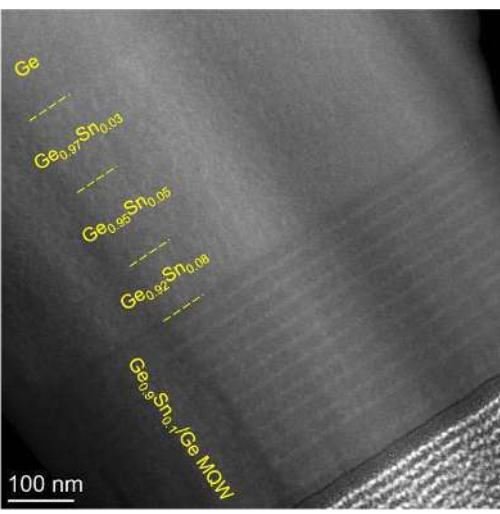

Fig. 2. Transmission electron microscopy image of the GeSn/Ge multi-quantum wells grown on the annealed GeSn/Ge/Si.

3. Conclusions

An in-situ annealing method for high-quality GeSn growth by MBE is developed. Significant surface morphology improvement has been observed by RHEED and verified by AFM. GeSn/Ge MQWs have been grown on such LTA-treated GeSn buffer layer showing well defined profile and excellent crystal quality.

Acknowledgements

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Epitaxy of Hexagonal SiGe Heterostructures: Towards Hexagonal SiGe Quantum Wells

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1. Introduction

The cubic crystal structure is the lowest-energy crystal phase for SiGe alloys. While all cubic SiGe alloys have an indirect bandgap, metastable hexagonal $Si_{1-x}Ge_x$ alloys with at least 65% Ge have a direct bandgap in the mid-near infrared [1]. This makes hexagonal $Si_{1-x}Ge_x$ alloys an interesting candidate for photonic integration with only Group IV materials.

Until now, studies of hexagonal $Si_{1-x}Ge_x$ focused mainly on crystals with a single composition. Heterostructures of hexagonal $Si_{1-x}Ge_x$ are still largely unexplored. For example, the band alignment between different hexagonal $Si_{1-x}Ge_x$ alloys has not been measured experimentally yet. The realization of controlled hexagonal $Si_{1-x}Ge_x$ heterostructures is necessary for probing these optoelectronic properties.

So far, the most convenient method for obtaining hexagonal $Si_{1-x}Ge_x$ alloys is the crystal transfer approach [2], in which the crystal structure is copied from a template, in this case a wurtzite GaAs nanowire. The $Si_{1-x}Ge_x$ then forms a shell around the GaAs core nanowire.

This study focuses on the epitaxial growth and optical characterization of nanowires with a large number of hexagonal $Si_{1-x}Ge_x$ shells. The findings of this research are important for future experiments with single- or multi-quantum wells of hexagonal Ge in between hexagonal $Si_{1-x}Ge_x$ barriers.

2. Hexagonal Ge-$Si_{1-x}Ge_x$ heterostructures

2.1. Epitaxy

Arrays of wurtzite GaAs nanowires have been grown using Au-droplets as catalysts. The GaAs nanowires are overgrown with multiple Ge shells separated by $Si_{1-x}Ge_x$ shells. Ge sections have alternating growth times of 5 and 10 mins, while the $Si_{1-x}Ge_x$ shells all have an equal growth time. Figure 1 shows an overview of the nanowires with the heterostructures in the shell.

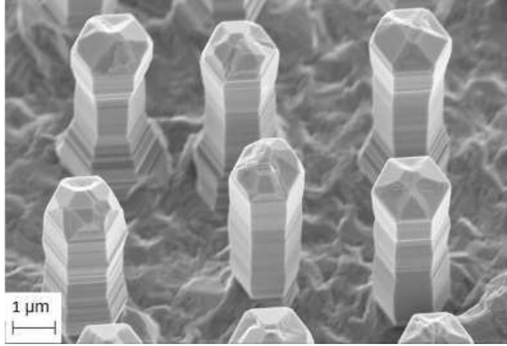

Fig. 1. 30-degree tilted SEM images of nanowires with a Wurtzite GaAs core and Hexagonal Ge - $Si_{1-x}Ge_x$ heterostructures as shells.

2.2. Transmission Electron Microscopy

The thickness of each shell is studied using TEM. A cross-section in the middle of the nanowire is shown in Figure 2. A structure of alternating Ge (light) and $Si_{1-x}Ge_x$ (dark) rings is observed, with the GaAs core at the center.

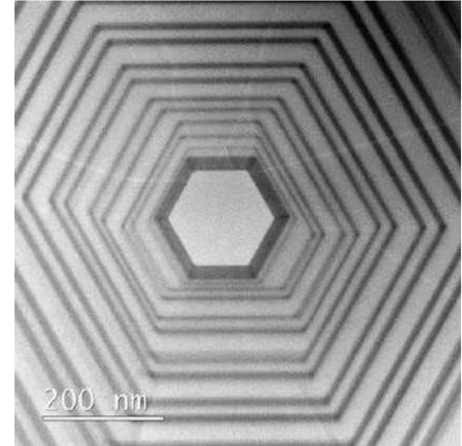

Fig. 2. Cross-sectional HAADF-STEM image along the [0001] zone axis of a nanowire with alternating $Si_{1-x}Ge_x$ and Ge shells. The GaAs core is visible as the center hexagon.

The thickness of the shells increases away with distance from the core. The increasing growth rate is a potential problem if one wants to grow structures with multiple quantum wells of equal thickness. A growth model has been developed to explain the increasing growth rate.

2.3. Growth model

The shell thickness on each facet has been measured and correlated with the distance to the GaAs core (Figure 3). A good fit to the data can be made by assuming a two-stage growth model, where the addition of a monolayer on the nanowire side facet happens by the two sequential processes of nucleation and layer completion.

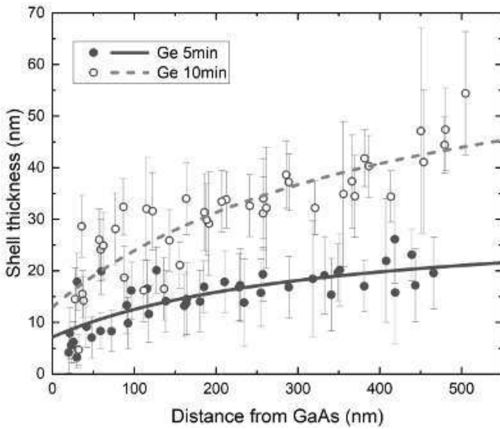

Fig. 3. Thickness of Ge shells that have been grown for 5mins (closed circles) or 10mins (open circles). The shell thickness increases further away from the core, which is explained well by a two-stage growth model (lines).

2.4. Optical characterization

The nanowires are characterized by photoluminescence (Figure 4). A single peak is observed at low excitation powers, while a second peak becomes visible at high excitation.

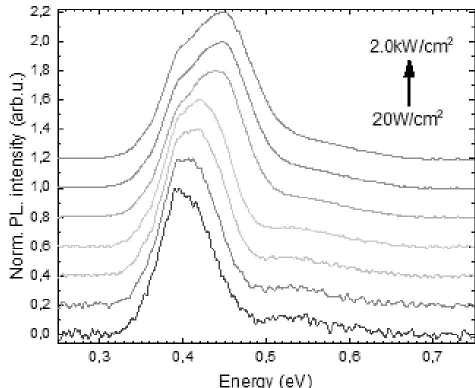

Fig. 4. Low temperature (4K) photoluminescence spectra of nanowires with hexagonal-Ge - $Si_{1-x}Ge_x$ heterostructures. The observation of bright photoluminescence provides proof for the hexagonal crystal phase.

3. Conclusions

Heterostructures of hexagonal Ge - $Si_{1-x}Ge_x$ have been grown. It is observed that the growth rate increases with the distance to the nanowire center. The increase is explained by a two-stage growth model. An optical characterization of these heterostructures has been made.

Acknowledgements

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N-type characteristics of undoped $Ge_{0.967}Sn_{0.033}$ fabricated on bulk n-Ge

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1. Introduction

GeSn is expected to be a next generation semiconductor material due to its notable characteristics such as tunable band structure [1]. In particular, misfit strain and Sn content are used as functions in tuning the band structure. For example, in the case of unstrained GeSn, the band structure is considered to be direct band gap at a Sn concentration about 11 %, and it is predicted that the required Sn concentration can be reduced by applying tensile strain [2, 3]. To fabricate high-performance GeSn devices, it is important to investigate the influence of Sn concentration on physical properties of GeSn.

It is well known that undoped GeSn grown on Si on insulator (SOI) shows p-type characteristics due to acceptor like defects [4]. In this study, however, we found that the GeSn grown on Ge substrates shows n-type characteristics in the low Sn concentration region, which was investigated by measuring current-voltage (*I-V*) and capacitance-voltage (*C-V*) characteristics for Schottky diodes and MOS capacitors fabricated on GeSn/Ge substrates.

2. Experiment

2.1. Formation of undoped GeSn layers on bulk Ge

Undoped GeSn layers were grown by molecular beam epitaxy (MBE) method on bulk n-Ge (N_D~10^{17} cm^{-3}) substrates, and the growth temperature was 150 °C. The layer thickness of GeSn was 200 nm. Based on the X-ray diffraction two-dimensional reciprocal space mapping (XRD-2DRSM), the GeSn layers were pseudomorphically epitaxially grown on bulk-Ge substrates (data not shown). And the substitutional Sn content was 3.3 %.

2.2. Sample fabrication and electrical measurements

Pt/GeSn Schottky diodes were fabricated as shown in Fig. 1. Pt was deposited by sputtering and patterned by lift-off technique. Post Metallization Annealing (PMA) was performed at 400 °C for 10 min. The fabricated samples were measured by *I-V*, *C-V* and current density-temperature (*J-T*) methods.

To eliminated the influence of GeSn/Ge junction on the investigation of GeSn properties, lateral metal/semiconductor (undoped GeSn)/metal (MSM) structures and MOS capacitors were also fabricated, as shown in Figs. 2 and 3, respectively. In the lateral MSM structures, TiN that shows ohmic contact on n-Ge was also used and compared with Pt [5]. In the lateral MOS capacitors, a SiO_2/GeO_2 bi-layer was formed as the insulator [6].

3. Results and discussion

Figure 4 shows the (a) *I-V* characteristics, (b') $1/C^2$-V plot and (c') the Arrhenius plots ($\ln(J/T^2)$-$1/T$) of Pt /undoped GeSn contacts, respectively. By assuming the fabricated samples are Schottky diodes, the electron barrier heights (Φ_{BN}) calculated from three methods are very similar (in the range of 0.53-0.58 eV), implying that the electron barrier is originated from Pt/GeSn contacts.

It is necessary to mention that Pt/p-GeSn contacts are ohmic, which was verified in our previous study. Therefore, there is a possibility that the rectified *I-V* characteristic shown in Fig. 4 is come from GeSn/Ge contact if the GeSn layer is p-type. To clarify it, we carried out *I-V* measurement for lateral MSM samples.

Figure 5 shows the *I-V* characteristics of MSM samples. TiN/GeSn contacts showed lager current values than Pt/GeSn ones (~10^2 at ±2 V). In our previous study, TiN and Pt show ohmic and Schottky contact characteristics on n-Ge, respectively, and Pt/p-GeSn contact is ohmic. Therefore, it is reasonable that Pt/GeSn contacts have higher Φ_{BN} than TiN/GeSn contacts. Consequently, the *I-V* characteristics in Fig. 5 indicate that the undoped GeSn layer is n-type.

The *C-V* characteristic of a lateral MOS capacitor is shown in Fig. 6, which also shows a typical n-type behavior. These results suggest that donor-like defects predominate in undoped GeSn grown on Ge with a relatively low Sn concentration of 3.3%.

4. Conclusions

The undoped GeSn layer grown on bulk Ge by MBE with a low Sn concentration of 3.3% shows n-type characteristics, suggesting that donor-like defects predominate in the low Sn concentration region, which is different from undoped GeSn grown on SOI substrates that predominated by acceptor-like defects.

Acknowledgements

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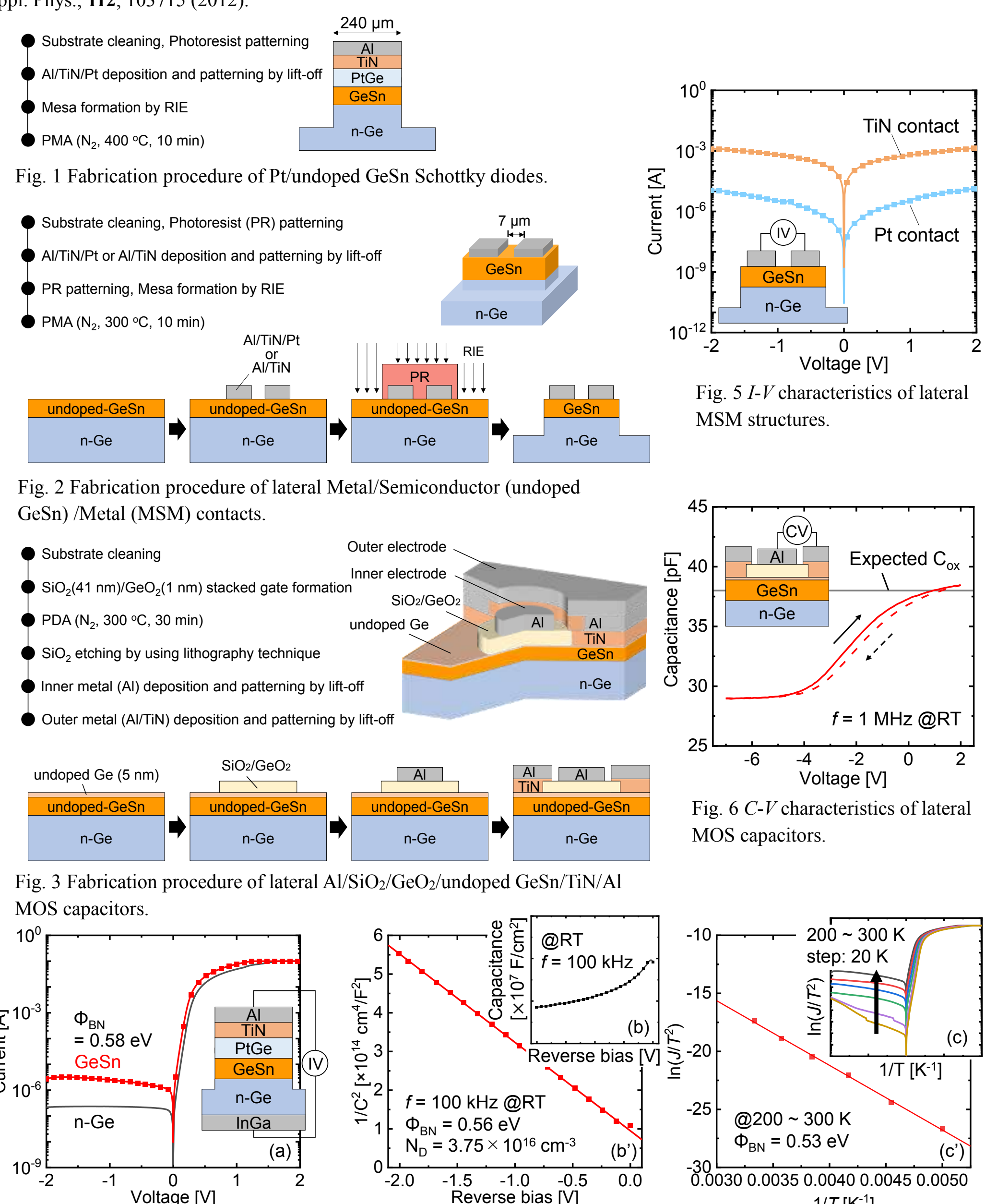

Fig. 1 Fabrication procedure of Pt/undoped GeSn Schottky diodes.

Fig. 2 Fabrication procedure of lateral Metal/Semiconductor (undoped GeSn) /Metal (MSM) contacts.

Fig. 3 Fabrication procedure of lateral Al/SiO_2/GeO_2/undoped GeSn/TiN/Al MOS capacitors.

Fig. 4 (a) *I-V* characteristics of Pt/undoped GeSn and Pt/n-Ge contacts. (b) *C-V* and (b')$1/C^2$-*V* characteristics of Pt/undoped GeSn contacts measured at RT. (c) *J-V* characteristics of Pt/undoped GeSn contacts and (c') its Arrhenius plot ($\ln(J/T^2)$-$1/T$).

Fig. 5 *I-V* characteristics of lateral MSM structures.

Fig. 6 *C-V* characteristics of lateral MOS capacitors.

Characterization of highly tensile strained SiP layer grown by epitaxy

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1. Introduction

Selective epitaxial growth (SEG) is notably used to thicken the sources and drains of advanced CMOS devices and benefit, thanks to some heavy in-situ doping, from low contact resistances.

We have developed a low temperature process [1] for tensile-SiP SEG that would be of use for advanced technological nodes devices such as finFETs or stacked nanowires or for monolithic 3D integration. The low process temperature (550°C) enables to lower the electrical resistivity of such layers and the tensile strain helps in boosting the electron mobility in the Si channel of NMOS devices. In this abstract, we will benchmark various metrology techniques to better understand the physical and electrical properties of such ultra-high P concentration SiP layers (from 0.47% up to 7.86%) and facilitate their use in advanced devices.

2. Experimentals details

Growth were carried out in a 300mm Applied Materials RP-CVD tool. Si_2H_6 and PH_3 were used as silicon and phosphorous precursors, together with H_2 as a carrier gas, for the 550°C, 20-90 Torr deposition of the t-SiP layers. X-Ray Diffraction (XRD) measurements were performed in an automated JV DXM tool from Bruker. Four points probe measurements of the sheet resistivity of our n-type t-SiP layers grown on p-type Si(001) substrates were performed in a WS3000 tool. Raman measurements were performed with a Ultra-Violet (UV) laser emitting at 368 nm and a HORIBA Jobin-Yvon T64000 spectrometer. Finally, Spectroscopic Ellipsometry (SE) measurements were conducted over a 210-2500nm spectral range in a Woollam RC2 tool.

3. Results and discussion

Firstly, we had a look at the epitaxial layer quality and the lattice deformation induced by the incorporation of small size phosphorus atoms in the silicon lattice. Omega-2Theta scans around the (004) XRD order gave us access to those parameters. Increasing the phosphine partial pressure by playing with the reactor pressure, the phosphine flow and the H_2 carrier flow enabled us to inject higher and higher amounts of tensile strain into the lattice, as shown in **Fig.1.** Thanks to Takagi-Tapin dynamical diffraction theory simulations, we were able to convert tensile strains into "substitutional" Phosphorous contents *y*, with the following lattice parameter $a_{SiP}(y) = (1-y)*5.43105 + y*4.94 - y\,(1-y)*0.019$ Å [2]. All t-SiP samples had well defined layer peaks with thickness fringes on both sides. Those features were typical of pseudomorphic, very high crystalline quality epitaxial films.

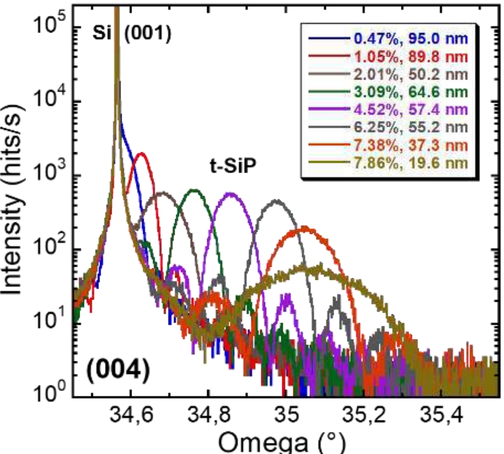

Figure 1: *Omega-2theta scans around the (004) XRD order for the various t-SiP layers grown at 550°C on p-type Si(001).*

We also had a look at the electrical resistivity evolution and thus the P^+ ions concentration when increasing the "substitutional" P concentration in those tensile-SiP layers. In **Fig. 2,** there is a growing discrepancy above $2x10^{20}$ cm^{-3} (0.4%) between the substitutional and ionized P concentrations from XRD and 4 points probe measurements, respectively. It was attributed to the formation of electrically inactive Si_3P_4 and P_xV clusters that contributed solely to tensile strain.

The tensile strain was also characterized with UV Raman, as shown in **Fig. 3a**. **Fig. 3b** frequency shift of the Si-Si Raman peak with the substitutional P concentration was modelled with a parabolic equation *(1)* different from Ref. [3]'s linear one:

$$\Delta\omega_{Si-Si}\,(=\omega_{exp} - \omega_0) = -146.88\,y + 1053.1\,y^2 \qquad (1)$$

It may be due to different growth conditions (550°C-Si_2H_6+PH_3, 550°C and reduced pressures here ⇔ SiH_2Cl_2+PH_3, 700°C and high pressures in [3]).

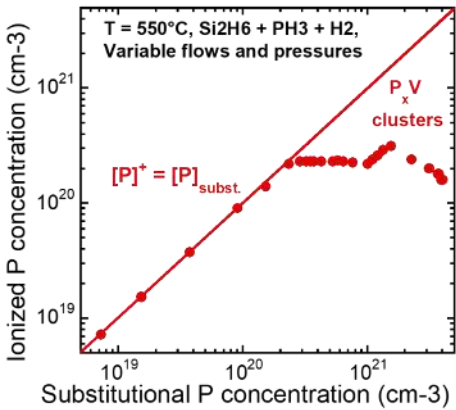

Figure 2: *Ionized P concentration (from 4PP) versus Substitutional P concentration (from XRD).*

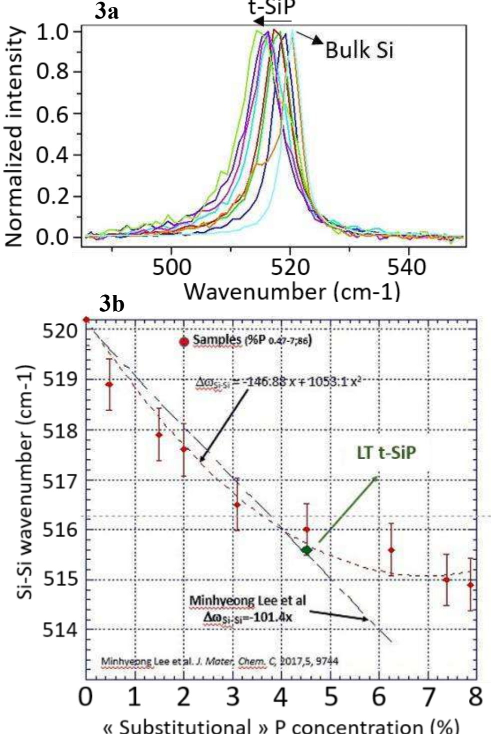

Figure 3a*: Si-Si Raman peaks for our t-SiP layers.* ***3b:*** *Si-Si wavenumber as function of the substitutional P concentration in t-SiP layers and comparison with Ref. [3]*

We also extracted the optical properties of those layers from SE measurements. As shown in **Fig. 4a,** n and k optical constants were impacted by high amounts of P, with a broadening of the critical points of the band structure in the UV-visible range and Free Carrier Absorption in the Near Infra-Red (NIR) range.

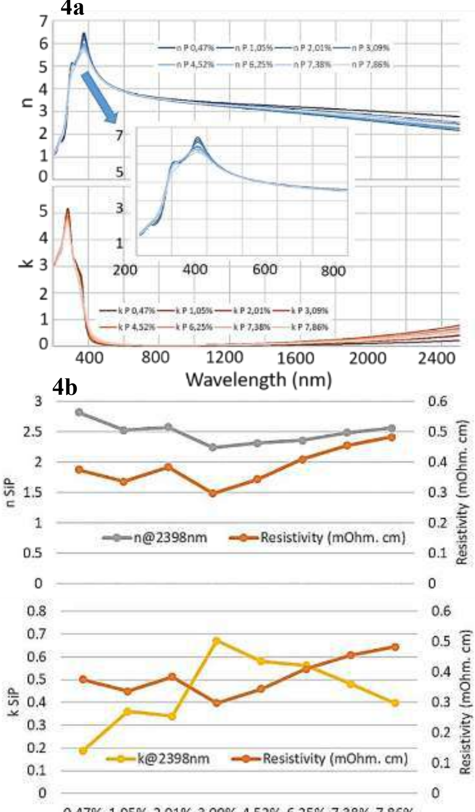

Figure 4a: *n & k optical constants in the 200-2500 nm range for t-SiP.* ***4b:*** *correlation @2398nm between n & k values and electrical resistivity.*

There were as expected clear-cut correlations between the electrical resistivity and n & k optical constants in the NIR. t-SiP layer thicknesses with our SE modelling were in very good agreements with X-Ray Reflectivity values. With a Drude modelling, we were otherwise able to obtain SE resistivity values with a good correlation with 4 points probes measurements (not shown here).

4. Conclusion

XRD, Raman, 4 points probe and SE measurements were used to assess the properties of tensile-SiP layers. Coupling those techniques was interesting to characterize such alloys where composition is intertwined with strain.

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Nanosecond radiative lifetime of Hexagonal Ge

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1. Introduction.

The Hex-$Si_{1-x}Ge_x$ nanowire material system provides a new direct bandgap semiconductor which is promising for Si-compatible lasers and optical amplifiers [1]. Due to the change in crystal structure from cubic to hexagonal, a direct bandgap emerges as the L-point is folded towards the Γ-point as shown in Fig 1 [2]. For hex-Ge however, theoretical calculations predict a very long 20µs radiative lifetime [1,2], implying that hex-Ge is theoretically predicted to have very poor photoluminescence quantum yield. A short radiative lifetime is a requirement for efficient light emission.

The optical absorption strength close to the bandgap is directly connected with the value of the matrix elements. For device applications, the absorption strength should be comparable to III/V semiconductors to enable efficient stimulated emission for enabling laser action or for use as a modulator. Our lineshape analyses will yield both the radiative lifetime and the absorption strength.

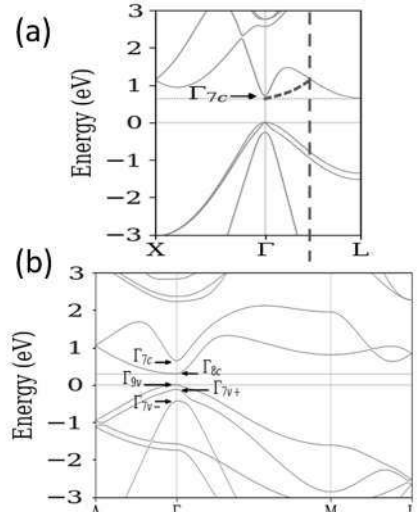

Fig. 1: (a) Band structure of cubic Ge, indicating zone folding of the L-minimum towards the Γ-point. (b) Band structure of Hex-Ge, featuring a direct bandgap.

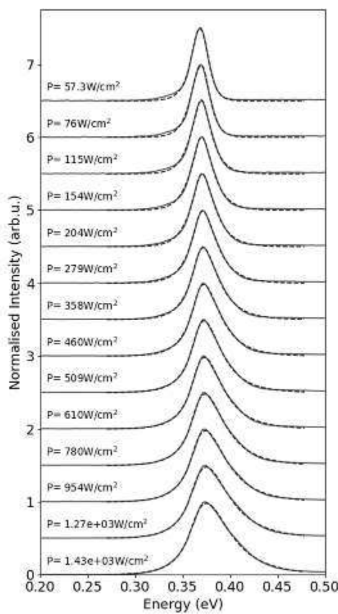

Fig. 2: Measured photoluminescence (PL) spectrum of Hex-Ge between 75.3 W/cm² and 1.43 kW/cm² fitted with the Lasher-Stern-Würfel (LSW)[3,4] model (dashed line).

2. Photoluminescence lineshape.

It has experimentally been shown that Hex-$Si_{0.2}Ge_{0.8}$ features a subnanosecond radiative lifetime [1]. Measurements of the lifetime of Hex-Ge remain challenging due to lack of available detectors and the presence of a blackbody radiation background in the mid-infrared. Since a direct measurement of the radiative lifetime in hex-Ge is not readily available, we present an indirect method to deduce the lifetime of hex-Ge by using the fact that the amount of Burstein-Moss bandfilling is proportional to the carrier generation rate and inversely proportional to the carrier lifetime. Therefore it is possible to extract the radiative lifetime by measuring the amount of bandfilling at a known carrier generation rate. The amount of bandfilling can be accurately determined by overlaying the low temperature (4K) photoluminescence spectra as a function of excitation density with an extended Lasher-Stern-Würfel (LSW)

model [3,4], which is basically a generalized Planck law. The Photoluminescence spectra and the LSW fits are shown to be in agreement in Figure 2.

Using the LSW model the steady-state carrier distributions can be determined which, when combined with the generation rate estimated from the excitation density and the nanowire geometry, can be used in a rate equation model to calculate the radiative lifetime.

3. Recombination lifetime of hex-Ge.

Given that hex-SiGe is shown to be in the radiative limit at 4K and hex-Ge is of similar optical quality [1], a LSW fit to the spectral lineshape provides the amount of Burstein-Moss bandfilling, which yields a radiative lifetime of τ=(5±2)ns for hex-Ge. This lifetime is in stark contrast to the 20μs lifetime expected from the theoretical predictions [2]. Moreover our LSW fits also provide values for the matrix element in the form of the transition's Kane energy $E_K \approx 4.68eV$. The Kane energy is derived from the absorption strength fitted in the LSW model. The Kane energy is much larger than the $E_K \approx 0.002eV$ expected from the pseudo-direct bandgap expected by theory [2]. The Kane energy obtained is close to the $E_k = 4.78eV$ as predicted by

$$E_K = E_g\left(\frac{m0}{m_r^*} - 1\right), \quad (1)$$

where E_g is the bandgap energy of hex-Ge, m_0 the free electron mass and m_r^* the reduced effective mass [5]. The large Kane energy implies that the optical absorption strength close to the bandgap is large and comparable to a III/V semiconductor. This directly implies that we expect a strong stimulated emission probability when hex-Ge is population inverted. Moreover, this implies that hex-Ge is usable for e.g. an optical modulator or a photodetector.

The combination of a high Kane energy and a fast radiative lifetime shows that the model is self-consistent which reinforces the confidence in the result. Combining the lifetime and the n-doping density of $\approx 10^{19}\ cm^3/s$ estimated from Atom Probe Tomography (APT) [1], we calculate an order of magnitude estimate of the coefficient for radiative recombination of $B_{rad} = \frac{1}{\tau_{rad}n_0} \sim 2 \cdot 10^{-11} cm^3/s$.

4. Conclusions.

In conclusion we observe a (favorable) discrepancy between theory and experiment for Hex-Ge, where theory predicts a slow lifetime of 20μs and a low Kane energy while the LSW fits to the experiment show both a high Kane energy and a nanosecond radiative lifetime. This implies that Hex-Ge allows bright light emission and promises to be a building block for hex-Ge lasers as well as for active optical component in silicon integrated opto-electronics.

Acknowledgements

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Atomistic modeling of extended defects in 3C-SiC/Si and Ge/Si heterostructures

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1. Introduction

Extended defects are unavoidably related to heteroepitaxy. Indeed the difference in lattice parameters and/or in thermal expansion coefficients between the substrate and the growing material causes deformation of the epilayer subsequently released by defect nucleation. Extended defects may have a crucial impact on the electronic properties of semiconductors and, as a consequence, deleterious effects on device performances. Therefore, their reduction and the control of their evolution and interaction is of utmost importance in all the growth processes.

Simulations able to predict dislocations behavior are a useful tool to address this problem. Different simulation methods allow to deal with different aspects: the collective evolution of a dislocation population in realistic-sized films (microns) is effectively modeled by Dislocation Dynamics (e.g. [1]), the atomistic process driving the motion and the interaction of dislocations is reliably predicted by Molecular Dynamics (e.g. [2]), the impact of dislocations on the electronic properties of a material is successfully computed by *ab initio* calculations (e.g. [3]). A strict comparison with experimental data is always necessary to fully catch a realistic description of the system, allowing for predictions.
This contribution will present examples of investigations of defect behavior in 3C-SiC/Si and Ge/Si heterostructures carried out via a joint approach of simulations (mainly Molecular Dynamics) ab initio calculations and experiments.

2. Killer defects in 3C-SiC/Si

Cubic silicon carbide (3C-SiC) is one of the most promising materials for innovation in high power and high-frequency electronics, due to its unique physical and chemical properties. For example, 3C-SiC combines a large bandgap value (2.35 eV) with a high bulk and channel electron mobility (up to 1000 and 250 cm^2/Vs, respectively). Moreover, it offers the possibility of a direct integration in the Si technology. In fact, 3C-SiC layers can be heteroepitaxially grown on (001) and (111) silicon substrates, thus offering an advantage over other SiC polytypes. However, structural and thermal differences between the two materials (20% in lattice parameter and 8% in thermal expansion coefficient at room temperature) hinder the possibility to obtain high-quality crystalline layers on Si substrates. Indeed, a high density of extended defects appears at -or close to- the 3C-SiC/Si interface both during the high temperature deposition and the cooling down. In particular, the low formation energy of stacking faults (SFs) in SiC favors the nucleation of partial dislocations to release strain and the associated SFs propagate into the 3C-SiC layer. Their presence, even in the low densities achieved (of the order of 10^4 cm^{-1}), has a detrimental impact on the electrical layer properties. However, an open question still remains how the SFs can be responsible for the detrimental leakage currents affecting the layers because theoretical predictions show they do not introduce mid-gap electronic states in the 3C-SiC phase. We use a multiscale approach, based on both classical molecular dynamics (MD) simulations and first-principle calculations, to investigate in-depth the origin, nature and properties of most common 3C-SiC/Si(001) extended defects, individuating the real candidates to be the killer defects in the system.

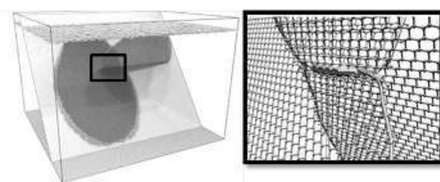
2.1. Triple stacking faults

Experiments show that SFs in 3C-SiC layers turn to be mostly grouped in three adjacent planes, forming microtwins [4]. Our MD simulations revealed a natural path for the formation of such defect based on the interactions between the bounding partial dislocations of dislocation loops nucleating at the surface. The dislocation complexes terminating triple SFs individuated by MD are used as an input for DFT calculations, allowing us to better determine the core structure and to investigate electronic properties. It turns out that the partial dislocation complexes terminating triple SFs are responsible for the introduction of electronic states significantly filling the band gap so that they can be ascribed as killer defects in terms of leakage currents. [3]

2.2. Dislocation forest

Leakage current has been also linked to a high density of crossing SFs (called dislocation forests) [2]. We performed a set of classical MD simulations

aimed at understanding the atomic-scale mechanisms leading to SF intersection for single and double SFs. Based on the trajectories observed in our MD simulations we have understood how dislocation forests are formed, providing new interesting details on a mechanism poorly investigated so far in the literature. A snapshot of a simulation is reported in the figure below. The whole simulation cell is shown on the left and the zoomed image of the intersecting SFs is reported on the right, the dislocation threading arms are highlighted.



A new defect is formed at the crossing point and MD reveal its complex structure. We then exploited ab initio calculations to analyze its electronic properties showing that if the crossing happens between two double-dislocation loops the related defect has several intragap defect states, which are very likely detrimental to the properties of the material.

3. New insight on extended defects in Ge/Si heterostructures

Germanium has attracted widespread attention in the last decades due to its compatibility with standard silicon technology and to several superior properties with respect to Si. Ge displays high carrier mobility, a small difference between its direct and indirect band gaps, and a strong absorption band at near-infrared wavelengths. Unsurprisingly then, Ge/Si(001) heteroepitaxial films are appealing for optoelectronic applications. However, the integration of Ge/Si(001) is not straightforward due to the large lattice mismatch between film and substrate (4.2%).

3.1. Ordered arrays of edge dislocations

It has been experimentally demonstrated that a suitable choice of the growth parameters involving deposition under out-of-equilibrium conditions followed by a higher temperature deposition or annealing, allows for the formation of a nicely ordered net of edge dislocations at the Ge/Si interface, improving the overall film quality and strain relaxation uniformity [5]. However, the mechanisms leading to such an outcome were unclear. We performed a set of classical MD simulations shedding light on the full set of atomic-scale processes driving to the experimentally findings. In particular, these mechanisms include vacancy-promoted climbing of dislocations so that the complex vacancy-dislocation interactions have been introduced in the simulation and analyzed [6].

3.1. Defects in Hexagonal Ge

Because of the small difference between the gaps in Γ and L points, the Ge band-related characteristics can be tuned via strain engineering. However, efficient light emission has not been fully achieved in this pathway. Instead, it has been realized by exploiting the metastable hexagonal crystal structure that naturally holds a direct band gap for Ge and Ge rich-SiGe alloys.

Hexagonal Ge has been obtained as shell material epitaxially grown around almost lattice-matched wurtzite (GaAs) nanowires. Extended defects are observed in the new realized crystal structure even if no lattice mismatch is present there. We identify a previously unknown partial planar defect and investigate its structural and electronic properties. Electron microscopy and atomistic modeling have been used to reconstruct this stacking fault and its terminating dislocations in the crystal. From band structure calculations we have concluded that the defect does not create states within the hex-Ge band gap. Therefore, the defect is not detrimental to the optoelectronic properties of the hex-SiGe materials family. [7]

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Impact of Carbon to Silicon Ratio on the Crystal Quality of Epitaxially Grown 3C-SiC thin film on Si(001) substrate

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1. Introduction

Silicon carbide (SiC) is a wide bandgap semiconductor which shows high potential in a world which relies so heavily on electronics. The high electric field breakdown and low switching losses of SiC make it ideal for high voltage and high frequency applications such as devices used in electric vehicles. High thermal conductivity (360 W $m^{-1}K^{-1}$)[1] allows SiC devices to conduct current with much greater efficiency. High hardness (9.3 Mohs hardness)[1] and resistance to all wet and gaseous chemical etchants mean that it is suitable for producing devices designed to withstand extreme conditions. There exists over 250 different crystalline forms of SiC called polytypes[2]. The hexagonally structured polytype of SiC, 4H-SiC, currently dominates the market due to well-developed homoepitaxial growth processes. SiC can also exist in a cubic, zinc-blende structured polytype 3C-SiC (β-SiC). The similar crystal structures of 3C-SiC and silicon (Si), and the ability to stabilize 3C-SiC at low temperatures (below 1410°C) make it suitable for growth on Si substrates, via heteroepitaxy. This is not the only advantage of 3C-SiC over 4H-SiC, for example, 3C-SiC possesses a lower bandgap of 2.4 eV (comparing to 3.2 eV for 4H- and 6H-SiC) and the highest theoretical electron mobility of ~1000 $cm^2V^{-1}s^{-1}$ at 293 K[1]. Both are properties that improve the efficiency of a power MOSFET. The ability to grow 3C-SiC on Si substrates makes the compound semiconductor compatible with the already well-established Si material system and presents the opportunity for heterogeneous integration with other group-IV semiconductors.

Despite its highly desirable properties, the production of high quality monocrystalline 3C-SiC for device manufacture is challenging because of the lattice defects, which occur during growth, caused mainly by the lattice mismatch between the substrate and the layer deposited[3]. Additionally, ratio of carbon (C) to Si atoms, which is altered by adjusting partial pressure of chosen reactive precursors, could impact material quality. However, all previous studies disregarded this parameter and the effect that this C/Si ratio may have on material quality. In literature, C/Si ratio varies over a very wide range, from as low as 0.3:1 up to 3:1[4,5]. Since the stoichiometry of monocrystalline SiC, independent on polytype, i.e. requires exactly 1:1 C/Si atom ratio reacting during growth, incorrect ratio of precursors could result in amorphous or polycrystalline material, as well as very defective and most likely rough thin films. Thus, perfecting this parameter is essential for epitaxial growth of 3C-SiC.

This study investigates the effect of changing C/Si ratio on the quality of heteroepitaxially grown 3C-SiC, and establish an effective method for the identification of the optimum C/Si ratio for 3C-SiC thin film growth[6].

2. Experimental Methodology

3C-SiC epilayers of thicknesses up to ~450 nm were grown on on-axis 100 mm diameter 525 μm thick Si(001) wafers within an industrial type ASM Epsilon 2000 RP-CVD cold wall system with the capability to grow on up to 200 mm diameter wafers. Schematic cross-section of the 3C-SiC/Si heterostructure is shown in Fig. 1c. The C to Si ratio was controlled through the ratio of Si to C gaseous precursors partial pressure injected into the growth chamber. Growth rates of over 10μm/hr were obtained. Details of growth can be found in reference [6].

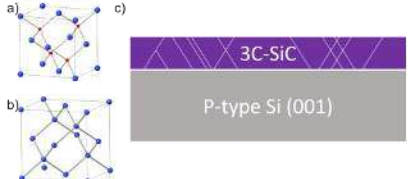

Fig. 1. The crystal structure of a) Si and b) 3C-SiC, where blue atoms are Si, and red atoms are C. c) The cross-sectional view of samples analyzed.

The 3C-SiC epilayer's thickness was measured by reflectance Fourier Transform Infrared Spectroscopy (FTIR) using a FTIR Bruker Vertex 70v. Surface morphology was measured by Bruker Dimension Icon AFM on peak force tapping mode over a 5x5 μm^2 area. State of strain and crystallinity was determined via analysis of High-Resolution X-ray Diffraction (HR-XRD) RSMs measured on Panalytical X'Pert pro diffractometer. 3C-SiC epilayer's thickness, crystallinity, surface roughness, type and density of defects were determined via analysis of Transmission electron microscopy (TEM) images acquired on a JEOL 2100+ microscope.

3. Results and discussion

Initially, it is necessary to use a C/Si ratio larger than 1 because some C is lost during growth. It is likely this is caused by side reactions between methyl radicals forming alkanes within the growth chamber. Growth time was kept constant for all materials grown, thus the only parameter affecting thickness was C/Si ratio. From Fig 2, it can be seen that initially 3C-SiC thickness decreases with increased C/Si ratio with a gradient of 2340 nm per unit of C/Si ratio. The decrease in thickness then slows from a C/Si ratio of 1.098 onwards, with a gradient of 531 nm per unit of C/Si ratio. This suggests the presence of 2 distinct reaction mechanisms. Initially there is a large excess of Si available in the gas phase. At the growth temperatures used Si is forms readily. This may explain the high growth rate, as Si deposits forming within the structure increase thickness. This growth rate drops quickly with increased C partial pressures, as this excess Si is utilized for the growth of SiC.

The second growth mechanism has much lower reaction rates. This suggests that it is dominated by the rate of decomposition of the C containing precursor, which has strong C-Si and C-H bonds, since Si deposits no longer form. Increasing C partial pressure still induces a drop-in reaction rate; however, it is by a much lesser amount. As this change in reaction rate is not caused by the depletion of excess Si, an alternative explanation may be that either excess C within the reaction mixture is included into the structure interstitially, or that the C containing precursor is decreasing the amount of available reaction sites, by surface terminating groups such as methyl groups.

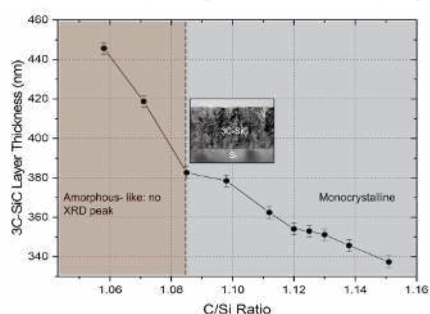

Fig. 2. C/Si ratio dependence on thickness of 3C-SiC epilayer.

In the ω-2θ XRD scans, it was found that samples with C/Si ratio of 1.098 and above produced spectra with peaks at 3C-SiC 002 and 004 crystallographic plane peak positions only, indicating that monocrystalline material was achieved. These peaks were absent for the samples grown with a lower contribution of C. This suggests that an excess of Si during growth results in amorphous-like material being produced. This supports the growth mechanisms determined by thickness measurements, as Si inclusions growing within the material could cause this amorphous structure to form. Roughness analysis of AFM scans reveals that excess C and Si both increase surface roughening equally, with the smoothest surfaces found in the range from ~1.098 to ~1.112 C/Si ratios as shown in Fig. 3. The results from AFM measurements are in agreement with the ideal C/Si ratios identified by thickness measurements. FWHM of ω HR-XRD scans reaches a maximum at this C/Si ratio, see Fig. 3. This is to be expected when perfect crystallinity is achieved, as more stacking faults form to relieve strain caused by the lattice mismatch. TEM imaging was used to confirm this.

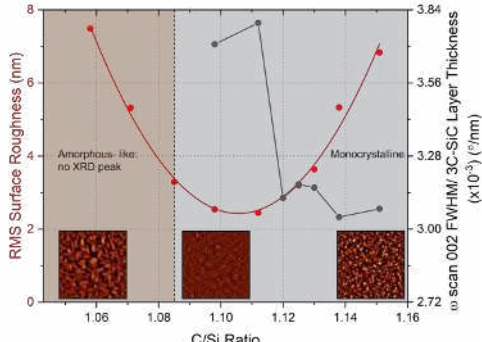

Fig. 3. C/Si ratio dependence on surface roughness of 3C-SiC wafers plotted with the C/Si ratio dependence on the FWHM of the 3C-SiC 002 ω peak. Surface images recorded are displayed as inserts.

4. Conclusion

Thickness measurements provided evidence for the existence of two different growth mechanisms which occur at different C/Si ratios. HR-XRD scans identified that excess Si inhibits the growth of monocrystalline material when the first growth mechanism applies. AFM measurements show that the surface morphology of samples is roughened equally by excess Si and C. The ideal C/Si ratios found by the presented techniques are in agreement. Once a combination of techniques has been identified for the quick and accurate identification of ideal C/Si ratio, this method may be adopted for all methods of epitaxial growth of 3C-SiC, removing the need for
expansive characterization.

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Mesoporous patterned silicon: a compliant substrate for defect free heteroepitaxy

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1. Introduction

Monolithic integration of group IV and III-V semiconductors on silicon platform allows the incorporation of high efficiency devices with advanced functionalities at low cost such as light-emitting diodes, photodetectors, lasers, and solar cell. However, high quality crystal growth remains restrained by the difference in lattice parameter between the epilayer and the substrate as well as the difference in thermal expansion coefficients [1]. Beyond a critical thickness, the epitaxial layer will release the strain energy giving rise to defect nucleation such as misfit and threading dislocations [2], which are detrimental to device performance and must therefore be avoided or at least minimized [3].

In theory, compliant substrate can be used to obtain defect free heteroepitaxy [4]. However, achieving an effective and practically useful compliant substrate remains a challenge.

In this work, we propose a fully compliant Si substrate as a practical way towards the long-standing goal of defect free heteroepitaxy of lattice mismatched materials on the industry-standard silicon substrates. The method relies on the deep patterning of the Si substrate to form micrometer scale pillars [5] and subsequent electrochemical porosification [6].

2. Methods

Typical cross section SEM micrograph of the compliant Si substrate is shown by Fig. 1. The substrate is formed by deep patterning and porosification to obtain porous silicon pillars (PSiP).

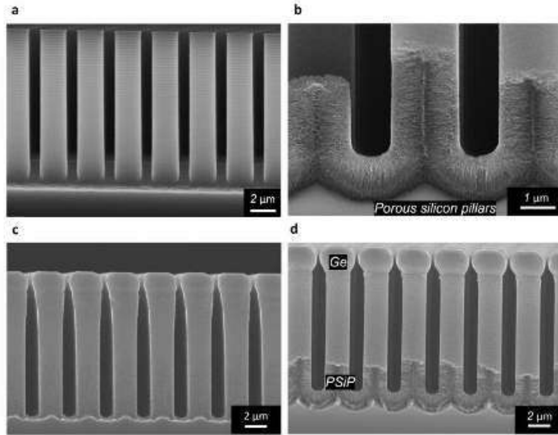

Fig. 1 | Compliant substrate realized using patterned Si(001) porous substrate. **a**, Cross section SEM image of a 10 µm tall deeply patterned silicon wafer using Bosch process. **b**, Cross section SEM image of the bottom part of anodized silicon pillars. **c-d**, 2 µm tall self-limited Ge microcrystals grown at 500°C by Chemical Beam Epitaxy using Ge solid source on SiP (**c**) and on PSiP(70%) (**d**).

SEM image of Bosch process [7] deeply patterned p-type Si(001) wafers (10-20 mOhm.cm) with ordered square-based arrays of Si pillars separated by 1 µm trenches have been used as substrates is shown in Fig. 1a. The obtained Si pillars (SiP) were anodized (Fig. 1b) in an O-ring electrochemical cell with an electrolyte composed of HF (49%) and anhydrous ethanol and a direct current density to form a 2 µm thick mesoporous Si pillars with 70±5% porosity.

A 200 nm thick Ge buffer layer has been first deposited at 200°C prior to the growth of 2 µm

thick Ge layers by Chemical Beam Epitaxy reactor at 500 °C (TC) using a solid source of Ge. An identical growth procedure has been used to deposit Ge on a patterned substrate which did not underwent the porosification procedure. The structural quality and defect density of the Ge microcrystals have been investigated using etch-pit counting (EP), High resolution x-ray diffraction (HRXRD) and transmission electron microscopy (TEM).

3. Results and discussions

A full elastic strain accommodation should be accompanied by the absence of threading dislocations. To validate this, etch-pit (EP) counting, and TEM cross-sectional observations has been performed on both Ge epitaxial material deposited on SiP and PSiP.

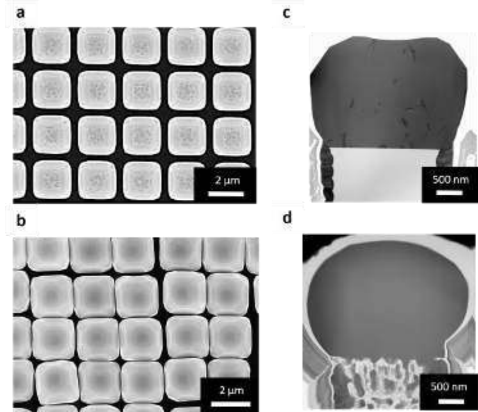

Fig. 2 | SEM and TEM characterization of Ge microcrystals. a,b, Top-view SEM image of Ge/SiP (**a**) and Ge/PSiP(70%) (**b**) after Etch-pit (EP) method. **c,d**, Low magnification BF-TEM images of the Ge/SiP reference substrate (**c**) and of the defect-free germanium grown on Porous silicon pillar (PSiP) (**d**).

As shown by the SEM (Fig. 2a) and TEM (Fig. 2c) micrographs, relatively high TDD around 5.10^{8} cm^{-2} is found to reach the surface for Ge grown on reference SiP. Meanwhile, for the Ge grown on PSiP, the entire microcrystal appears completely defect free (Fig. 2b,d). This constitutes a direct proof of porous Si pillars properties being able to accommodate the mismatch strain.

4. Conclusions

We report the synthesis of a fully compliant substrate for the epitaxial growth of lattice mismatch material on silicon. Combining micro-patterning of silicon substrate and mesoporous crystalline structure allow full accommodation of both lattice and thermal stress. The porous structure allows to avoid formation of any defect at the interface, which not only yields a high-quality material but also allows the synthesis of devices requiring very low thickness and would decrease the cost and time associated to the growth process of metamorphic structures.

This study provides a proof of concept for the synthesis of effective compliant substrate for heteroepitaxy and the integration of lattice mismatch microcrystals on Si platform.

Acknowledgements

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Quantification of substitutional and interstitial carbon in thin SiGeC films using in-line X-Ray-Photoelectron spectroscopy

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1. Introduction

The incorporation of germanium (Ge) and carbon (C) into silicon (Si) results in a large variety of silicon-based devices due to its ability to tailor the properties, whether structural, electronic, optical, chemical, mechanical …[1]. Consequently, the incorporation of C and Ge is of great benefit for device applications. One of the most crucial questions concerning the epitaxial growth of $Si_{1-y}C_y$ or $Si_{1-x-y}Ge_xC_y$ is the ratio of carbon incorporated into substitutional and interstitial sites, which is highly dependent on growth conditions [2]. Commonly, the total carbon concentration (C_{tot}) is measured using off-line Secondary-Ion Mass Spectrometry (SIMS) and the amount of substitutional carbon (C_{sub}) using in-line X-ray-Diffraction (XRD). However, this approach requires two characterization techniques, one being destructive.

In this work, the potential of non-destructive and in-line X-ray Photoelectron Spectroscopy (XPS) to determine the substitutional and interstitial carbon incorporation in a single measurement is investigated. The XPS results are then compared with the reference approach, which combines XRD and SIMS.

2. Experimental details

2.1. Epitaxy processes

A 300 mm Epi Centura Reduced Pressure-Chemical Vapor Deposition (RP-CVD) reactor from Applied Material was used to grow the SiGeC layers at 10 Torr and 550 °C with H_2 as carrier gas. Silane (SiH_4) and Disilane (Si_2H_6) were used as Si precursors. Germane (GeH_4) and Methylsilane (SiH_3CH_3) were used as Ge and C sources. All layers were grown on slightly p-type doped 300 mm Si(001) blanket wafers.

2.2. Metrology control

Conventional ω-2θ scans around the (004) X-ray diffraction (XRD) order were used to determine the crystalline quality and the substitutional carbon concentration (C_{sub}) using a Ge:C strain compensation ratio of 11.75. Secondary Ions Mass Spectrometry (SIMS) using Cs^+ primary ions, at 1 keV, was used for depth profiling. SIMS measurements gave access to atomic Ge (i.e real) and total C concentrations (C_{tot}). C atomic quantification C_{tot} were determined thanks to carbon implanted SiGe reference samples.

The surface composition was analyzed shortly after epitaxy by in-line X-ray Photoelectron Spectroscopy (XPS) using a Revera/Nova Veraflex II at $1x10^{-8}$ Torr. The X-ray source was a monochromatic Al K-α source radiating at 1486.6 eV. The hemispherical detector was operated at a pass energy of 35 eV and a collection angle of 90° to the surface (normal). The CASAXPS software program was used to fit all XPS spectra and atomic sensitivity factors were provided by the XPS supplier. After removal of a Shirley background [3], the spectra envelopes for narrow scans were fitted with a sum of photoelectron peaks constrained in position and Full Width at Half Maximum (FWHM) and with 70/30% Gaussian/Lorentzian line shape.

3. Experimental results

3.1. XPS data analysis

XPS measurements can be altered by the presence of adventitious carbon due to air exposure. The presence of contamination carbon could be detrimental since the aim is to quantify the amount of carbon incorporated into the SiGe film. The effect of waiting time between epitaxy and XPS measurement was thus assessed by measuring 1 and 50 hours after epitaxy for a $Si_{1-0.80-y}Ge_{0.2}C_y$ layer with y = 1 at% of fully substitutional carbon atoms (i.e C_{sub}=C_{tot}).

The 1 hour C 1s signal can be deconvoluted into two subpeaks. The first minor peak at 284.90 ± 0.1 eV, is most likely related to surface contamination (C_{Conta}) accumulated after the deposition. Indeed, after a waiting time of 50 hours, the intensity of this minor peak increases with time after deposition. Thus, because only substitutional carbon is present in this layer, the main peak at 283.95 ± 0.05 eV is attributed to substitutional carbon atoms (C_{sub}). Similar XPS assignment were reported for $Si_{1-y}C_y$ layers (with y < 2 at%) grown on Si, as in [4,5]. Consequently, all XPS results described here

below are generated spectra acquired shortly after SiGeC epitaxy (typically less than 3 hours) and the contamination peak area was excluded from all atomic concentration calculations.

3.2. Results

Fig. 1 shows the measured C 1s signals of $Si_{1-0.8-y}Ge_{0.2}C_y$ layers grown using Si_2H_6 (a) or SiH_4 (b) for various carbon concentrations. It can be observed that the signal-to-noise ratios are good, even for low carbon content (<1 at%).

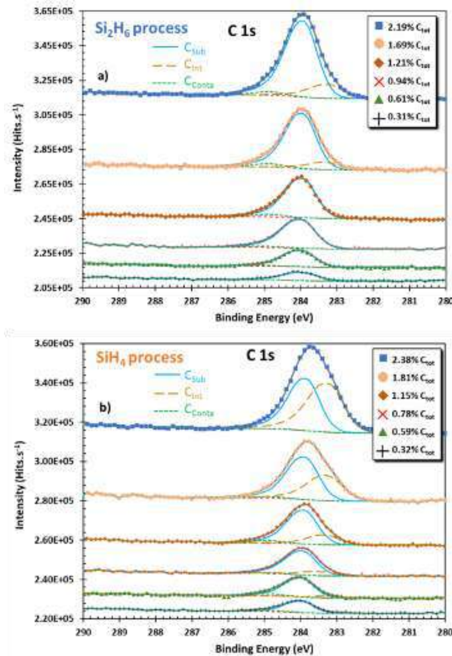

Fig. 1. Sets of C 1s photoelectron binding energy spectra or $Si_{1-0.8-y}Ge_{0.2}C_y$ layers grown using the Si_2H_6 (a) or SiH_4 (b) process with different carbon concentrations. Spectrums are superimposed for clarity. C_{tot} concentrations given in the inset are SIMS results.

For Si_2H_6 (**Fig. 1a**), when only substitutional carbon atoms are incorporated (y < 1.21 at%), the C 1s signal intensity increases proportionally with the carbon content, without a shift in the binding energy. However, it is observed that a further increase of the C concentration leads to a shift and broadening of the C 1s signal towards lower binding energies. At this point, a third component appears. This third component located at 283.35 ± 0.1 eV, is assigned to interstitial carbon atoms (C_{int}).

Using the SiH_4 (**Fig. 1b**) process, a much higher shift and broadening of the C 1s signal towards lower binding energies is observed than when using the Si_2H_6. Indeed, a very small C_{int} component appears for C_{tot} = 0.58 at% and it increases progressively with the total carbon concentration, up to 2.38 at%. This suggests a progressive increase in the amount of C atoms in interstitial sites which is much greater than with Si_2H_6.

The relative atomic percentages of C_{sub} and C_{tot} (i.e C_{sub} + C_{int}) using XPS are plotted in **Fig. 2** ((a) using Si_2H_6 and (b) using SiH_4) together with atomic percentages of C_{sub} measured by XRD and C_{tot} measured by SIMS, as functions of the SiH_3CH_3 mass flow ratio.

In both cases, the XPS results are in good agreement with the coupled XRD and SIMS results.

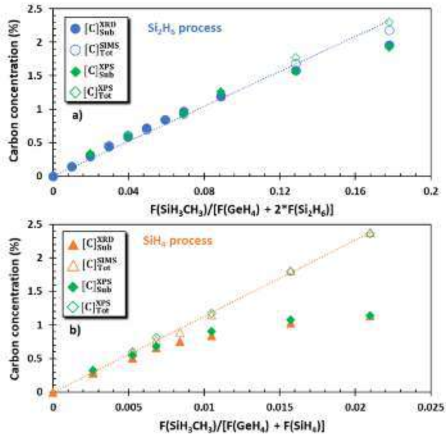

Fig. 2. C concentrations (C_{sub} measured by XRD and XPS, C_{tot} measured by SIMS and XPS) in $Si_{1-0.8-y}Ge_{0.2}C_y$ layers grown using the Si_2H_6 (a) or SiH_4 (b) process as functions of the SiH_3CH_3 mass flow ratio.

4. Conclusions

A high sensitivity of in-line XPS was demonstrated to monitor changes in carbon incorporation as a function of SiH_3CH_3 flow, even for low carbon concentration (i.e y < 1 at%). The compositions of C using XPS are in good agreement with reference values determined by XRD and SIMS. Thus, XPS can give access to the relative carbon concentration present in different chemical states (i.e substitutional and interstitial) with only one single in-line and non-destructive measurement. Therefore, this technique shows potential to monitor carbon concentrations in $Si_{1-y}C_y$ or $Si_{1-x-y}Ge_xC_y$ layers on blanket and electrical wafers.

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Background carrier concentration in intrinsic Ge-rich SiGe/Ge heterostructures integrated on Si(001)

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1. Introduction

Ge-rich silicon-germanium (SiGe) heterostructures are promising candidates for novel devices in the field of optoelectronic and photonic applications [1]. The possibility to manufacture those using CMOS-compatible materials and processes is an outstanding advantage.

As an example, the n-type Ge/SiGe material system has been proposed as a potential candidate for the realization of THz quantum cascade laser sources working at room temperature [2]. Here, the realization of the several mm-thick active layers, made of hundreds of quantum wells and barriers, are mandatory but extremely challenging to deposit since the strain balancing conditions have to be carefully achieved. Beside the effect of lattice strain on the band alignment of the complex quantum cascade structures, the plastic relaxation via the insertion of extended defects occurring in the growth process plays a major role in the charge profile existing in the device, which, in turn, strongly impacts the correct operation of devices. In fact, the existence of extended defects generates an electrical charge background that can combine with the intentional doping in the device design inducing a compensation or increase of the active carrier concentration. Therefore, the actual background carrier concentration needs to be known in order to counteract this problem during fabrication and to correctly describe the device electrical properties in the simulations.

In this work, we comprehensively studied the active carrier concentration in as-grown intrinsic $Si_{0.06}Ge_{0.94}$/Ge/Si heterostructures grown by reduced-pressure chemical vapor deposition (CVD) in a 200 mm CMOS pilot line. We conveniently use these Ge-rich SiGe virtual substrates because they are a promising foundation for the integration of n-Ge/SiGe superlattices on Si [3].

2. Results and Discussion

In order to identify the residual carrier concentration in the investigated heterostructure three complementary characterization techniques are applied: by Hall effect measurements we investigate the transport dynamics due to the defect-originated doping, while by capacitance-voltage (C-V) profiling and deep level transient spectroscopy (DLTS) the fixed charge distribution and the capture/release dynamics are investigated, respectively.

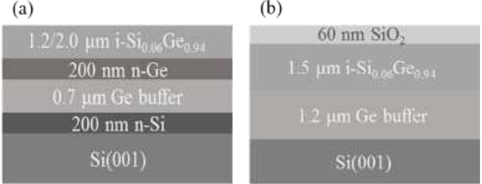

Fig. 1. The designed $Si_{0.06}Ge_{0.94}$/Ge/Si heterostructure used for (a) Hall effect and (b) C-V and DLTS measurements.

The investigated $Si_{0.06}Ge_{0.94}$/Ge heterostructures aligned for the different characterization techniques are schematically shown in Fig. 1. Measurements on both devices reveal a p-type conductivity of the intrinsic $Si_{0.04}Ge_{0.96}$ material in the operating temperature range of many optoelectronic devices.

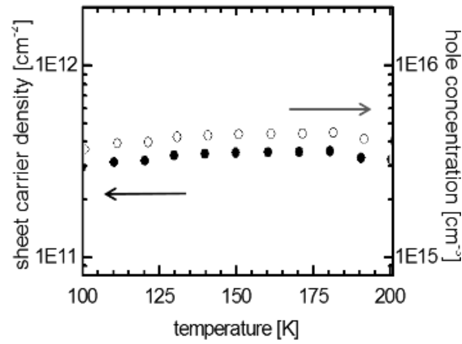

Fig. 2. The temperature dependent sheet carrier density and corresponding hole concentration of the $Si_{0.06}Ge_{0.94}$ layer as measured by the Hall effect.

Figure 2 demonstrates the temperature dependent sheet carrier density estimated by Hall effect measurements of the two investigated samples with different layer thicknesses. According to the differential Hall approach, a sheet carrier density of 3-4x10^{11} cm^{-2} is estimated in the temperature range between 100 K and 250 K corresponding to a constant hole density of 4x10^{15} cm^{-3} in the as-grown intrinsic $Si_{0.06}Ge_{0.94}$ layer (Fig. 2(b)).

Based on pulsed C-V characteristics of the fabricated MOS capacitors, the carrier density profiles at temperatures below 200 K are calculated from the slope of a $1/C^2$-V plot and are shown in Fig. 3. Again, a constant majority carrier density of approximately 5x10^{15} cm^{-3} of the nominal intrinsic $Si_{0.04}Ge_{0.96}$ layer is extracted. The existence of a free hole concentration including ionized acceptors and compensating donors in the nominally intrinsic $Si_{0.04}Ge_{0.96}$ layer might be related to deep acceptor-like defect states inside the semiconductor bandgap [4].

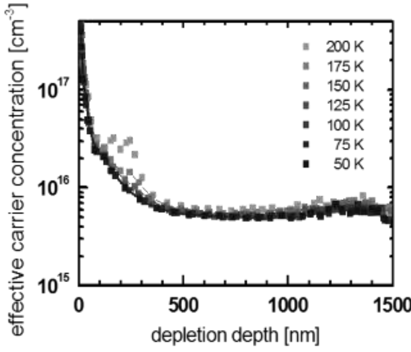

Fig. 3. The temperature dependent effective carrier concentration in dependence of depletion depth of the studied $Si_{0.06}Ge_{0.94}$ layer.

In addition, the source of the included defect states is examined by DLTS. One dominant hole trap is found in the DLTS spectra at 225 K as shown in Fig. 4. This bulk trap is associated with a thermal activation energy E_T of 0.325 eV above the valence band edge E_V estimated by an Arrhenius plot. Carrier capture kinetics of the observed trap level indicate a point as well as an extended defect character. Therefore, the observed acceptor-type bulk trap may be correlated with native point defects that accumulate in the long range strain field around threading dislocations (2x10^7 cm^{-2}) introduced during epitaxial growth of the $Si_{0.04}Ge_{0.96}$/Ge heterostructure.

The mid-gap position of the observed defect level implies an attractive trapping center for free carriers and/or effective generation-recombination centers. This will impact the active carrier concentration in the final devices build using similar Ge-rich SiGe/Ge heterostructres and should be taken into consideration during fabrication and simulation.

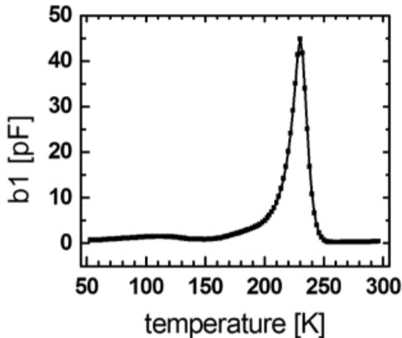

Fig. 4. DLTS spectra of the fabricated MOS capacitor on the studied $Si_{0.06}Ge_{0.94}$/Ge/Si heterostructure.

3. Conclusions

A background hole concentration in the mid 10^{15} cm^{-3} range is found in $Si_{0.06}Ge_{0.94}$/Ge/Si heterostructures. A hole trap at mid-gap position might be the reason for the residual p-type conductivity caused by acceptor-like bulk defects.

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Modeling of Silicon Epitaxy on 300 mm Wafers and Analysis of Thickness Uniformity at Different Scales

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1. Introduction

Epitaxial growth of silicon layers on silicon wafers in CVD reactors is an important step in production of silicon wafers for memory, logic and other microelectronic devices. Modern requirements for silicon layer thickness uniformity require optimization of gas flow patterns and temperature distribution, while experimental investigation of these processes is challenging.

2. Work description

2.1. Model description

In present work we demonstrate a numerical model of silicon epitaxy process on a single 300 mm wafer within a simplified geometry of a CVD reactor based on published data [1-3]. Presented numerical model includes calculation of global heat transfer, taking into account effect of lamp heating, specular reflection from curved reflectors, absorption and refraction of radiative heat at quartz domes, and multiple heating zones above and below the susceptor and silicon wafer. The results of the global temperature distribution are used for calculation of gas flows, chemical reactions, and the growth rate in the flow zone of CVD reactor (Fig. 1). The chemical model used for calculation of bulk chemical reactions, surface chemical reactions, and finally the growth rate has been presented in [4, 5]. The model accounts for coupled effect of temperature distribution, and flow rate of TCS and H2 flow rates on the flow structure and details of the growth rate distribution over the wafer. All computations have been performed using CVDSim3D software.

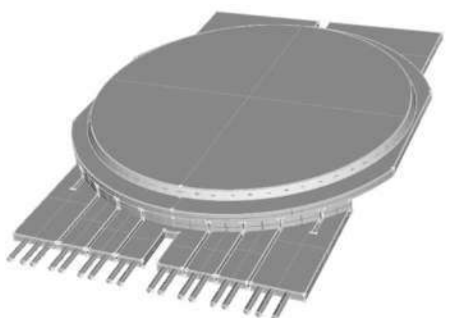

Fig. 1. Flow Zone geometry.

2.2. Modeling results

To demonstrate model sensitivity to variations of process parameters, computations of growth rate have been performed for different ratio of precursor gas concentration at the inlet, and for different wafer temperature. In the present abstract, we will make a more detailed overview of the effect of TCS to H_2 ratio on growth rate over the wafer and its uniformity. To evaluate this effect, TCS growth rate in the reference process was increased and decreased by 20%. Calculated instantaneous distribution of the growth rate over the wafer have been averaged by angle due to wafer rotation in the real process, and presented in the Fig. 2.

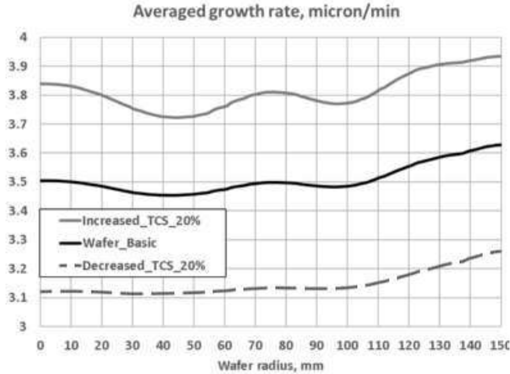

Fig. 2. Angle-averaged distributions of the growth rate over wafer radius.

For quantitative comparison of growth rate uniformity between different processes, the uniformity was calculated for each process using the expression (1), and obtained values of growth rate uniformity are summarized in the Table I.

$$Uniformity = (max-min)/(max+min) \cdot 100\%. \quad (1)$$

Table I. Growth rate uniformity.

Process	Growth rate uniformity
TCS increased by 20%	2.8%
Reference process	2.5%
TCS decreased by 20%	2.3%

2.3. Discussion

Obtained distributions demonstrate that the increase of TCS flow rate, while keeping the same hydrogen flow rate, results in increase of the averaged growth rate over the wafer, due to a more active supply of silicon-containing species to the wafer. On the other hand, higher flow rate of TCS results in increase of observed growth non-uniformities due to variations in the gas flow structure above the silicon wafer. Higher TCS flow rate increases intensity of secondary vortexes above the silicon wafer, which results in increase of instantaneous growth rate fluctuations observed over the wafer surface (Fig. 3) and increase of growth rate and thickness non-uniformity at the angle-averaged growth rate distributions (Fig. 2).

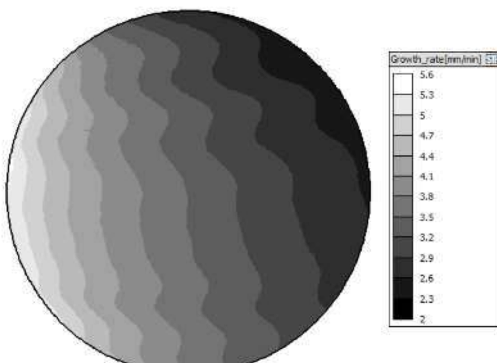

Fig. 3. Instantaneous distribution of the growth rate over silicon wafer.

In addition to the effect of TCS flow rate on the uniformity of the growth rate, this paper discusses the effect of temperature on growth rate and epi layer thickness uniformity. Lastly, the final part of the paper discusses the factors responsible for the observed growth rate non-uniformities and reviews possible ways to optimize the process to increase the uniformity of the epilayer thickness.

3. Conclusions

A new tool for modeling of silicon CVD processes both in the entire reactor and in the flow zone, CVDSim3D, has been tested for the silicon epitaxy process in a geometry similar to industrial reactors for the production of 300 mm silicon epitaxial wafers.

Variations of different process parameters on the growth rate and its uniformity were studied. It was demonstrated that the model can resolve fine non-uniformities of the growth rate at the scale of a few percent, and can calculate the effect of the process parameters on the growth rate and its uniformity. This creates promising opportunities for the application of computer modeling in the optimization of industrial processes and reactors.

Acknowledgements

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Emergence of Hyperuniformity in Self-Assembled SiGe Nanostructures

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1. Introduction

Disordered hyperuniform (HU) materials [1,2] are a class of systems featuring strongly suppressed density fluctuations on large scales, similar to ordered crystals, while not having any Bragg peaks in diffraction like a liquid. These materials exhibit interesting properties, such as topologically protected electronic states, glassy electronic quantum state transitions, Anderson localization of light, polarization selectivity, lasing, and full photonic band gaps for light propagation. Fabrication of materials featuring HU characters is, therefore, of high interest. However, tuning such properties to be effective at specific sizes and frequencies for the targeted applications is generally challenging. Moreover, most of the fabrication of HU patterns relies on top-down techniques, with severe limitations in the scalability of the resulting structures.

Patterns featuring correlated disorder and a HU character are commonly found in nature, such as in morphogenesis in biological systems, thin-layer wrinkling, and phase separation [2]. Often, they result from the interplay of short-range interactions and non-linear dynamics of the underlying physical processes. For instance, ideal phase separation by spinodal decomposition produces HU patterns [3]. Exploiting such spontaneous processes may then represent a viable pathway to produce hyperuniform materials in a hybrid top-down/bottom-up fashion. Here, the self-assembly of SiGe nanostructured materials featuring HU characters is discussed.

2. Results

After introducing the basics of hyperuniformity and the tools exploited to assess them in experimental patterns, a few representative systems are discussed. As the pivotal case, we show how mono-crystalline $Si_{1-x}Ge_x$ layers deposited on silicon-on-insulator substrates can undergo a spinodal-like solid-state dewetting featuring correlated disorder with an effective HU character [4]. Nano- to micrometric-sized structures targeting specific morphologies and HU character can be obtained, proving the generality of the approach and paving the way for technological applications of disordered HU metamaterials. Three-dimensional, phase-field simulations of surface diffusion assess the underlying non-linear dynamics and the physical origin of the emerging patterns [4]. Applications and perspectives are then discussed, pointing at exploiting the obtained pattern with other materials [5], and the emergence of HU character in other fabrication processes involving amorphous and polycrystalline SiGe thin films.

2.1. Hyperuniformity

The notion of hyperuniformity has been first introduced for point patterns via the structure factor $S(\boldsymbol{k})$. Ideal HU characters correspond to $S(\boldsymbol{k}) \sim |\boldsymbol{k}|^\alpha$ for $|\boldsymbol{k}| \to 0$ with $\alpha > 0$ and $\boldsymbol{k}$ the reciprocal-space coordinates. Generalizations have been proposed to account for such a property in scalar fields, where, in brief, the role of $S(\boldsymbol{k})$ is played by the spectral density $\psi_F^*(\boldsymbol{k})$, namely the Fourier transform of the autocovariance function of the field $F(\boldsymbol{r})$, with $\boldsymbol{r}$ the real space coordinates [2]. The quantification of the ideal HU character for experimental patterns is usually not accessible due to the inherent lack of information for $|\boldsymbol{k}| \sim 0$ (as this would require the analysis of an infinitely extended sample). Estimation can be given by looking at $H = S(k_{\text{small}})/S(|\boldsymbol{k}|)$ (or analogous for ψ_F^*) with k_{small} a small accessible value of $|\boldsymbol{k}|$. While the correlated disorder can be identified by deviation of $S(\boldsymbol{k})$ from 1, conditions $H < 10^{-2}$ and $H < 10^{-4}$ are commonly denoted as nearly and effective HU characters, respectively [6,7]

2.1. Spinodal-like solid-state dewetting of SiGe films

A $Si_{1-x}Ge_x$ film, typically with $x = 0.3 - 1$ and thicknesses ranging from a few nanometers up to hundreds of nanometers, is deposited by molecular beam epitaxy (MBE) on 14nm thick monocrystalline UT-SOI (on 25nm thick buried oxide, BOX). The surface of such a multilayer structure is crystalline. Surface diffusion is then expected to be activated by high-temperature treatments such as annealing under vacuum. A representative set of structures obtained by annealing is reported in Figure 1(a). They correspond to the morphologies obtained in different positions of the same sample having different annealing

temperatures due to temperature gradients in the experimental setup. While corresponding to a solid-state dewetting regime - namely the substrate (BOX) is uncovered - this process deviates from standard solid-state dewetting [8,9]. Indeed, it features homogeneous nucleation of holes and breakup of the film and leads to spinodal-like structures (observed in the so-called spinodal dewetting, which is however expected in different systems). Different morphologies can be obtained by changing annealing time, Ge content, and thickness, from holes to connected structures, and eventually, isolated islands. Residual strain before annealing is observed, as well as dislocations for thick samples. The obtained patterns feature strongly correlated disordered and, for some of them, values of H approaching the effective HU regime are obtained, c.f. Fig. 1(c).

Three-dimensional, phase-field simulations of surface diffusion, including capillarity and elasticity effects [4,10] due to the mismatch between SiGe and SOI, reproduce the main features of the process, see Fig. 1(b). Good agreement is obtained in terms of topological features (Minkowski functionals [4,11]), as shown in Fig. 1(d), also pointing to peculiar fingerprints of spinodal patterns. These simulations assess the role of elasticity in triggering the dewetting instability through a homogeneous breakup of the thin film.

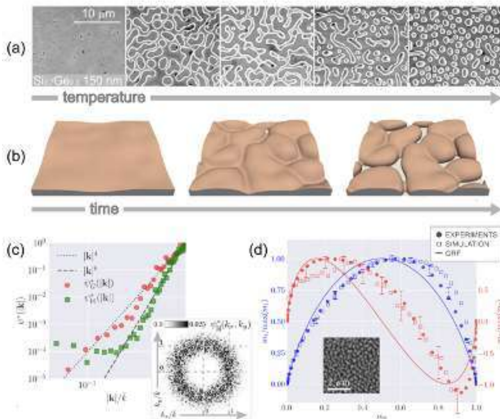

Fig. 1. *Spinodal-like solid-state dewetting and effective hyperuniformity*. (a) SEM images of 150 nm $Si_{0.7}Ge_{0.3}$ on UT-SOI after 4h annealing at increasing temperatures (estimated in the range 800-850°C from left to the right). (b) A representative phase field simulation reproducing the homogeneous breakup of a perturbed film. (c) Spectral density $\psi_H^*(\boldsymbol{k})$ for the height profile $H(x,y)$, compared to a representative Gaussian Random Field (GRF). (d) Analysis by Minkowski functionals for simulated and experimental patterns compared to an analytic prediction for a GRF [4].

2.1. Applications and Perspectives

The process described above is exploited to produce disordered patterns entailing correlations for high- and low-dielectric constant metal oxides, such as titania and silica, on silicon and glass wafers combining sol-gel dip-coating and nano-imprint lithography (soft-NIL) [5]. The correlated disordered is characterized by measuring the bidirectional reflectance distribution function under laser and white light illumination. Note that, differently from previous investigations on these systems, here we directly measure the HU character through light scattering rather than inferring it from the morphological analysis of the emerging patterns [5].

Dewetting of amorphous and polycrystalline SiGe/SOI layers is also shown to deliver morphologies similar to the monocrystalline counterpart. In these systems, recrystallization dynamics and interfaces (grain boundaries) among crystalline domains contribute to the onset of dewetting and the morphological evolution of thin films, still retaining interesting correlations among self-assembled structures.

Finally, nano architectures fabricated by impacting thin layers of amorphous Ge deposited on thin SOI with a Ga+ ion beam are shown to feature correlated disorder. While single ion beam scans may be used to produce uniform patterns with some degree of periodicity, multiple scans are shown to deliver nearly HU structures.

3. Conclusions

With this contribution, we discuss different SiGe systems where correlated disorder approaching nearly and effectively HU characters is achieved. They represent the first demonstration of such property for group-IV nanostructured systems and are shown to be transferrable to other materials. Moreover, the discussed evidence sheds new light on the basic mechanisms at play during solid-state dewetting and their control for hybrid fabrication techniques.

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Flash Annealing to Reduce the Threading Dislocation Density in Ge Films for CMOS-Compatible Monolithic Integration on Si

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1. Introduction

Optimized manufacturing processes make Si the material of choice in the electronics industry. However, for optoelectronics Si cannot be used in short-wave infrared range (SWIR) due to its indirect bandgap at 1.1µm. A way to access the SWIR is by monolithically integrating Ge on Si and use the Ge thin film as an absorber layer. One of the main challenges is that Si and Ge have a relatively high lattice mismatch of 4.2%, which leads to relaxation defects in the Ge thin film. Among these defects, threading dislocations (TDs) are a source of deep traps in the bandgap of Ge and are highly detrimental for optoelectronic device performance [1]. Upon annealing Ge thin films at temperatures above 750°C, TDs diffuse in the film and annihilate, decreasing the total TD density (TDD). These temperatures are however incompatible with CMOS processing.

A possible solution to the implementation of monolithic Ge devices on Si it the use of millisecond heat pulses, also known as flash lamp annealing (FLA) [2]. These millisecond pulses allow the optically active Ge film to heat above 800°C and decrease its TDD, while maintaining a high temperature gradient with masked regions in the chip, suitable for CMOS integrated circuitry.

With our research, we show that the quasiequilibrium TDD of Ge thin films epitaxially grown on Si can be reached with heat pulses of millisecond duration using FLA. The quasiequilibrium TDD is defined as in Ref. [2]. We determine the optimal pre-heating temperature, investigating its effects on crystal quality and Si-Ge interface intermixing.

2. Experimental Methods

Molecular beam epitaxy (MBE) has been used to deposit Ge in a two-step process on Si(001) substrates with a resistivity of 300-500Ohmcm. The substrate preparation before growth is similar to Ref. [3]. After a bakeout of the substrate, the first step was a 70nm deposition of Ge at nominal 350°C followed by a nominal substrate temperature growth at 550°C for the remaining thickness.

Samples with a Ge film thickness of 450nm were then loaded in to the Rovak Semi-line 3.0 flash lamp annealing system and pre-heated to a fixed substrate temperature. The film was then flashed with one or multiple 7.65ms pulses, each of energy density of 48.1 J/cm^2. One sample was loaded and annealed at 800°C without flashing to determine the quasiequilibrium TDD of the 450nm Ge film.

The annealed Ge films have then been characterized with AFM, SEM, TEM and XRD. Symmetric Bragg-Brentano scans of the Ge(004) peak are used to evaluate the intermixing between Si and Ge. The Full Width at Half-Maximum (FWHM) of the Ge(004) rocking curve (RC) is used to estimate the crystal quality improvement after annealing as the RC FWHM is proportionally related to the TDD [4].

3. Results

3.1. Ge TDD reduction with a single FLA step

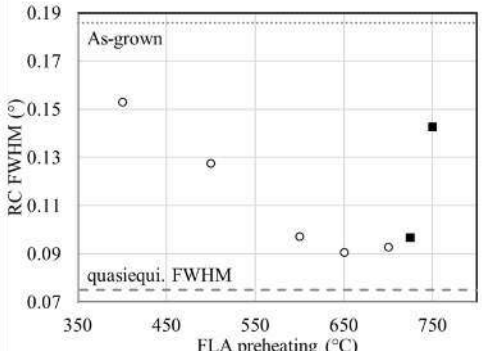

Fig. 1. XRD RC FWHM of Ge films flashed with a single pulse with different preheating temperatures. The dotted line shows the as-grown film FWHM, and the dashed line the quasiequilibrium FWHM, obtained by annealing the as-grown sample at 800°C for 5 minutes. Filled squares represent films that have melted during FLA.

Fig. 1 reports the FWHM of 450nm thick Ge films obtained with a single FLA step using different pre-heating temperatures. The results show that single flashes of millisecond duration can significantly increase the crystal quality of epitaxially grown Ge on Si. We observe a RC FWHM improvement when increasing the preheating temperature from 400°C to

650°C due to the higher temperature obtained in the film during the flash. However, the opposite trend is observed when further increasing the preheating temperature. This is attributed to the intermixing between Si and Ge, which hinders the diffusion of TDs due to higher Peierls stress [5]. No matter the preheating temperature, we notice that a single flash is not sufficient to attain the quasiequilibrium RC FWHM.

3.2. Ge TDD reduction with multiple FLA steps

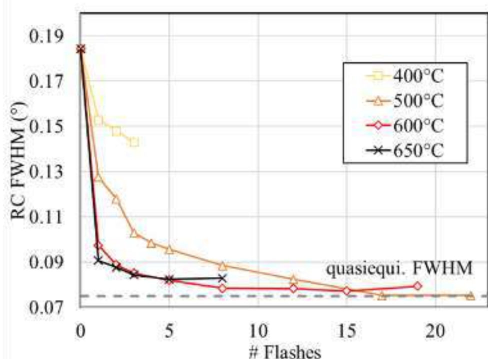

Fig. 2. XRD RC FWHM of Ge films flash-annealed with multiple pulses, using different pre-heating temperatures ≤ 650°C to avoid strong intermixing with the Si substrate. The dashed line represents the quasiequilibrium FWHM.

Fig. 2 shows the RC FWHM of the Ge thin film in function of the number of flashes for different preheating temperatures. After each set of flashes, the sample was cooled down and the RC FWHM was measured. This process was repeated until no improvement in RC FWHM was observed.

In Fig. 2 we can observe that with a pre-heating temperature of 500°C, 600°C and 650°C after multiple flashes a saturation point in RC FWHM is reached. It can be noticed, however, that the saturation FWHM depends on the pre-heating temperature, and only with 500°C the quasiequilibrium FWHM is attained. This can be attributed to the different levels of intermixing occurring with different pre-heating temperatures, as shown in Fig. 3. In particular, with a pre-heating temperature of 500°C, intermixing is avoided, as the absence of shoulder in the Ge(004) peak shows in Fig. 3, even after 22 pulses. On the other hand, the 600°C preheated Ge film shows a pronounced tail in Fig. 3 which increases with the number of flashes applied. For higher preheating temperatures, the intermixing is even more pronounced as seen for the 650°C preheated sample, already after 8 pulses. These results indicate that TDs reorganization will be limited by any Si-Ge intermixing occurring at the interface before the saturation TDD value is reached.

3. Conclusions

We have shown that a single flash can significantly

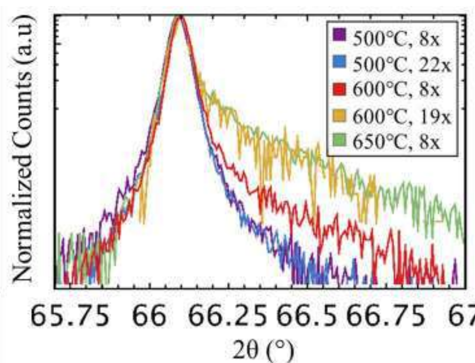

Fig. 3. Symmetric Bragg-Brentano scans of the Ge(004) peak for different preheating temperatures and amount of flashe pulses. The scans have been normalized to facilitate comparison. Intermixing between Ge and Si generates a shoulder towards higher angles of the Ge(004) peak.

increase the RC FWHM of monolithically integrated Ge thin films on Si. Still, a single flash is not sufficient to reach the quasiequilibrium RC FWHM but multiple flashes are needed. We have shown that for a preheating of 500°C, the quasiequilibrium RC FWHM can be reached with 18 flashes while samples annealed at higher preheating temperatures saturate at higher FWHM. This effect was attributed to the intermixing of Si and Ge, and demonstrated with XRD Bragg-Brentano scans.

We expect that with pulses of even higher energies the preheating temperature could be lowered further as the higher pulse energy heats the Ge film more. Furthermore, this also would require a lower number of flashes to reach the quasiequilibrium FWHM.

To complete the study, there are ongoing experiments with different film thicknesses, TDD quantification and modeling of the RC FWHM improvement. Furthermore, simulations of the heat distribution in the device during the flash are being performed to demonstrate the compatibility of FLA with CMOS devices. We expect to present also these additional results at the conference.

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Quantum Devices in MBE-grown Ge

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1. Introduction

High-mobility two-dimensional carrier systems provide a uniform, low-noise and scalable platform for quantum information processing. Especially, single electrons (conduction band states) and holes (valence band states) confined in quantum dots are promising candidates for qubits. The quantum information can be encoded in the charge or the spin degree of freedom of such an electron (hole). Generally, spins have longer relaxation times due to their smaller coupling to fluctuations in the electric environment.

While various material systems are under consideration for hosting high-quality two-dimensional carrier systems, we focus on undoped quantum wells of Ge between SiGe barriers. Under application of proper electric fields, these quantum wells host high-quality two-dimensional hole system (2DHS) [1, 2]. Two techniques to grow crystalline Ge/SiGe heterostructures have been studied: chemical vapour deposition (CVD) and molecular beam epitaxy (MBE). Undoped CVD-grown Ge/SiGe heterostructures have recently gained increasing attention as a host for qubits [3, 4, 5].

The 2DHS, due to a large Fermi level pinning of Ge close to the valence band, is easily contacted with metals. The absence of a Shottky barrier between the metal and Ge also allows for high-probability Andreev reflection when the metal turns superconducting. Therefore, hybrid devices, where superconductivity has been induced into the Ge 2DHS, have been studied with some success [6, 7, 8]. Nevertheless, the interface between Ge and the superconductor remains to be optimized.

2. Main

2.1. Aim of the study

The main goal of this work consists in building up a qubit platform in Ge, which includes semiconducting quantum dot charge and spin qubits and various types of superconductor / semiconductor hybrid qubits.

2.2. Approach

Ge/SiGe heterostructures are grown by MBE and their transport properties are characterized at low temperatures. As a starting point, different types of heterostructures are grown for the semiconducting and for the hybrid qubits. To achieve low-noise quantum dot qubits, the quantum wells for the former are grown with a large barrier separating the 2DHS from the interface. For the latter, our approach to achieve a highly transparent superconductor-semiconductor interface consists in growing the superconductor in-situ, directly after growing the quantum well, and without breaking the vacuum. Also, to ensure a strong coupling between the 2DHS and the superconductor, the top SiGe spacer separating the quantum well from the superconductor is much smaller as compared to the purely semiconducting heterostructure.

2.3. Results

We first test the quality of the deeply burried 2DHS using magnetotransport of standard hall-bar shaped devices. We achieve a mobilies of ~80’000 cm^2/Vs at a density of ~ $4x10^{11}$ cm^{-2}, which is a considerable improvement compared to previous MBE-grown heterostructures and comparable to CVD-grown heterostructures. The results are shown in Fig. 1.

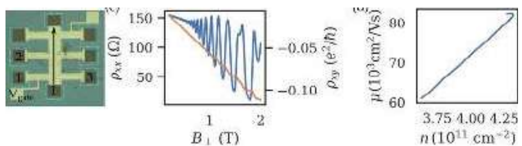
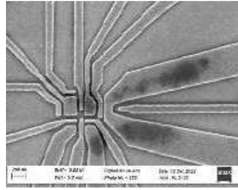


Fig. 1. The optical microscope image of a Hallbar device similar to the one measured is shown on the left. The dependence of the longitudinal and transverse resistivities on the applied magnetic field are displayed in the middle panel. The right panel shows the extracted densities and mobilities.

We move on to fabricate quantum dot devices using combined optical and electron-beam lithography techniques. The device is shown in Fig. 2, together with transport data showing the characteristic bias triangle features of transport through double quantum

dots.



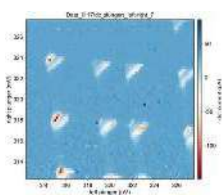
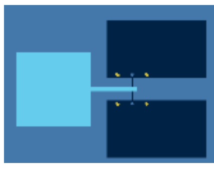


Fig. 2. The SEM image of a double quantum dot device is shown on the left. Transport measurements on the right show the typical finite bias triangles expected for a double quantum dot.

Next, we set up fabrication schemes to build Josephson Junctions from the shallow quantum wells. This includes the development of recipes for oxide deposition at low temperatures and selective etching of Al. The schematics of a finished device is shown in Fig. 3 together with the corresponding transport data: measuring the voltage drop upon applying a current across the junction, we clearly see the signatures of a Josephson Junction, indicating success in proximization.



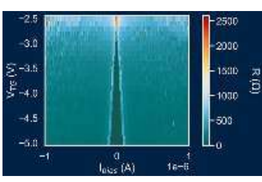


Fig. 3. A schematics of the Josephson Junction device is displayed on the left hand side, and a measurement of the resistance (voltage drop / applied current) is shown on the right. At low enough top-gate voltages, when the 2DHG is accumulated, the resistance vanishes for applied currents below the critical current.

3. Conclusions

We have shown that MBE-grown Ge/SiGe heterostructures can host high-mobility quantum wells, in which double quantum dots and Josephson Junctions can be formed, the basic ingredients for semiconductor and hybrid qubits, respectively. While quantum dots and Josephson Junctions have been shown on CVD-grown Ge before, we present a novel approach of in-situ growing the superconductor to provide a clean superconductor-semiconductor interface.

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Software for the simulation of SiGe devices and recent progress on Flying Electron Qubits

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1. Introduction

Quantum computers require millions of qubits on a single chip. A scalable implementation with silicon-based technology is needed. The manufacturing workflow includes computer-aided design tools for quantum-technology hardware. Here we present our recent work on modeling qubits with the nextnano [1] software. We present two concepts where the simulation of the electrostatic potential landscape is of utmost importance: Flying Electron Qubits [2] and Quantum Dot Qubits [3, 4]. Both share the similarity that the qubits are formed and manipulated by applying voltages through external gates (Fig. 1). The layout of these gates is in general very complex. Thus, an accurate calculation of the potential energy landscape is required. A self-consistent solution of the 3D Schrödinger and Poisson equation is needed to obtain the position-dependent two-dimensional electron gas (2DEG) density (Fig. 2). We present a workflow that has been used to optimize the qubit layout [5].

2. nextnano Software

2.1. Summary of physical models

Numerous SiGe devices can be modeled using the nextnano software. In this work we summarize the physics implemented into the nextnano software relevant for simulations of SiGeSn-based nanostructures. First, we discuss the calculation of the band structure using several approaches: parabolic, 6-band, 8-band, 30-band k.p, and the tight-binding method. Then we describe the implemented models, which include strain, shift and splitting of the bands due to strain and deformation potentials. A self-consistent solution is needed for the Poisson equation, single-band or multi-band Schrödinger equations, and the drift-diffusion current equation. Some devices require the calculation of the quantum transport using the nonequilibrium Green's function method (NEGF). We will show several simulation examples such as modulation doped quantum wells, capacitance-voltage calculations, optical absorption in quantum wells, and QCLs. The nextnano software serves both as an educational and a research tool.

2.2. Flying Electron Qubit

We introduce a novel qubit concept which has been realized in a semiconductor heterostructure. The concept is similar to that of a photonic quantum computer but, instead of photons, electrons are used as carrier of quantum information. The progress of charge manipulation in semiconductor-based nanoscale devices opened up a novel route to realize a flying qubit with a single electron (Fig. 3). We discuss its most promising realizations, and show how numerical simulations are applicable to accelerate experimental development cycles, namely the calculation of the electron density, the pinch-off voltage and the conductance. We review the full stack of numerical simulations needed for fabrication of the flying qubits: Electrostatic simulations and (time-dependent) quantum transport. The transmission and the partial local density of states (Fig. 4) provide valuable information on quantum interference occurring in the tunnel-coupled wire and the Aharonov–Bohm (AB) interferometer. We discuss applications of open-source (KWANT) [6] and commercial platforms [1] for modelling the flying qubits.

2.3. Quantum Dot Qubit

Finally, we present results of 3D Schrödinger–Poisson calculations of gated quantum dots. This work was inspired by Ref. [3, 4, 7] where silicon-based spin qubits were investigated.

3. Conclusions

We highlight some of the important features of the nextnano software in terms of modeling silicon-germanium-based nanostructures. The tool is easy to use in order to learn about the physics of these devices. We showed that sophisticated modeling is important for the design and optimization of qubits. The discussion points out the large relevance of software tools to design quantum devices tailored for efficient operation.

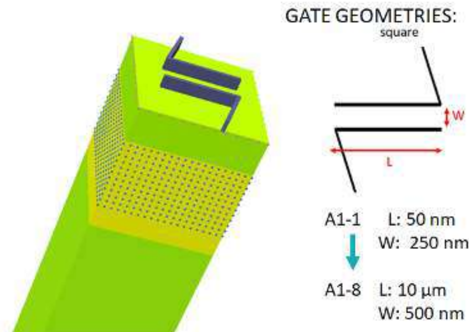

Fig. 1. Schematics of a modulation-doped heterostructure with a typical shape of gates forming a quantum point contact inside the 2DEG.

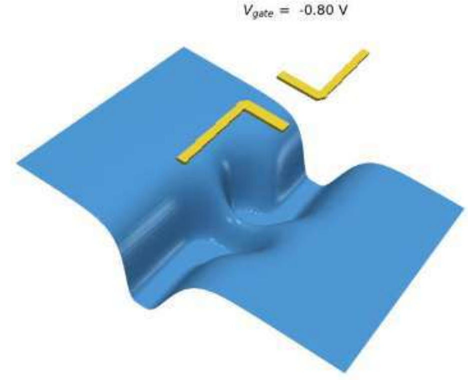

Fig. 2. By applying a negative bias to the gates, the electron density in the 2DEG can be locally depleted forming a quantum point contact.

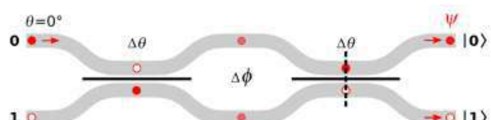

Fig. 3. A Flying Electron Qubit is an electron two-path interferometer allowing precise adjustment of the qubit state via tunnel-coupling (Δθ) in the tunnel-coupled wires and the quantum phase (Δφ) picked up along transport across the central island (Aharonov–Bohm ring).

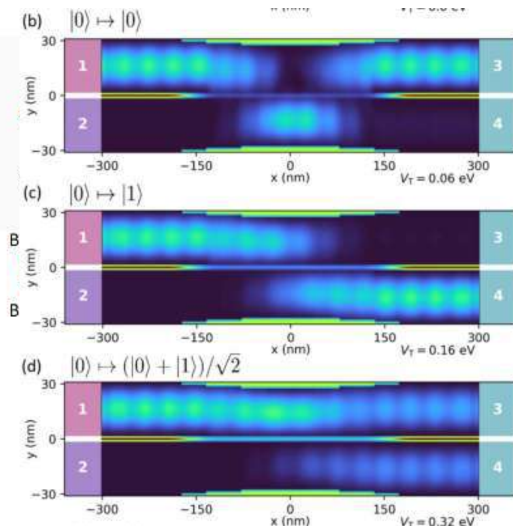

Fig. 4. Calculated partial local density of states in a tunnel-coupled wire. Electrons enter the wire in lead 1 and exit in (b) lead 3 (|0> state), (c) lead 4 (|1> state), or (d) lead 3 and 4 (superposition of |0> and |1>).

Acknowledgements

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Hole mobility in strained germanium exceeds 4×10^6 $cm^2V^{-1}s^{-1}$

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1. Introduction

Mobility of free carriers in conduction (electrons) or valance (holes) bands, along with a reasonably large energy band gap, is one of the most important quality measures of any semiconductor material, determining its suitability for applications in a large variety of classical electronic, optoelectronic and sensor devices, as well as for novel applications in emerging quantum devices. Higher mobility enables faster operation of a device at lower power consumption and thus leading to reduced Joule heat dissipation, which is essential to minimize for continues circuit scaling as well for increasing the speed of current electronic devices. This is even more important for those devices and electronics to operate at cryogenic temperatures, for example, to control distributed registers of quantum processors.[1] Also, carrier mobility is the critical quality of a semiconductor material for quantum devices, often playing a key role towards new discoveries.[2]

Over the last 4 decades research and development of epitaxial growth techniques like Molecular Beam Epitaxy (MBE) and Chemical Vapour Deposition (CVD) and technologies along with understanding physics of carrier transport in low-dimensional systems resulted in appearance of strained Si, SiGe and Ge quantum well (QW) heterostructures, epitaxially grown on a standard Si(001) substrate with high mobility electrons and holes at both cryogenic and room-temperatures.[3-5] In this work we present a major breakthrough in achieving the record high hole mobility of 4.3×10^6 $cm^2V^{-1}s^{-1}$ in strained Ge (s-Ge) QW heterostructure.

2. Results and discussion

For the presented research, an undoped s-Ge QW heterostructure was grown by Reduced Pressure CVD (RP-CVD) on the standard Si(001) wafer of 150 mm diameter, via relaxed $Si_{1-x}Ge_x$/Ge buffer.[3] Epitaxy of the relaxed buffer layers and active region of the s-Ge QW were carefully optimised to substantially improve the material quality. All epilayers were intentionally undoped. For transport characterization of 2D hole gas (2DHG) at varied density, gated Hall-bars were fabricated using standard UV lithography, dry etching, and thin film deposition techniques.

The experimentally obtained 2DHG mobility as a function of the 2DHG density at temperature 290 mK is plotted on log-log scale in Fig. 1. The mobility varies from 1.2×10^6 $cm^2V^{-1}s^{-1}$ to 4.3×10^6 $cm^2V^{-1}s^{-1}$ at density from 3.2×10^{10} cm^{-2} to 1.8×10^{11} cm^{-2}, respectively. The mean free path of holes, for these data, increases from ~5 µm, in lower density range, up to ~30 µm for higher densities. The maximum mobility of $4.3x10^6$ cm^2 $V^{-1}s^{-1}$ exceeds by over 3 and 4 times the previously reported record values of $\sim1.3\times10^6$ $cm^2V^{-1}s^{-1}$ at $p=2.7\times10^{11}cm^{-2}$ in modulation doped (MOD) s-Ge QW heterostructure [3] and $\sim1\times10^6$ $cm^2V^{-1}s^{-1}$ at 1×10^{11} cm^{-2} in undoped gated s-Ge QW heterostructure,[4] respectively. Analysis of the mobility versus carrier density slope indicates the mobility at lower carrier density range, i.e. below 1×10^{11} cm^{-2} is limited by scattering on background ionised impurities with an estimated volume density of $\sim3\times10^{14}$ cm^{-3}.[6] This very low background impurity density is manifested as an exceptionally high mobility in the whole range of 2DHG densities, i.e., the sample show record-high 2DHG peak mobility $4.3x10^6$ $cm^2V^{-1}s^{-1}$ in the high density range of $\sim1.8\times10^{11}cm^{-2}$, and also very high mobility over 1.2×10^6 $cm^2V^{-1}s^{-1}$ in the low density range down to 3.2×10^{10} cm^{-2}. Fitting of the experimental data in low-density range i.e. $<1\times10^{11}$ cm^{-2} shows an almost linear increase of the mobility with the density, i.e. $\mu\sim p^{0.85}$. At higher than $1x10^{11}$ cm^{-2} carrier density, the mobility increase slows down, following a power-law dependence with a smaller

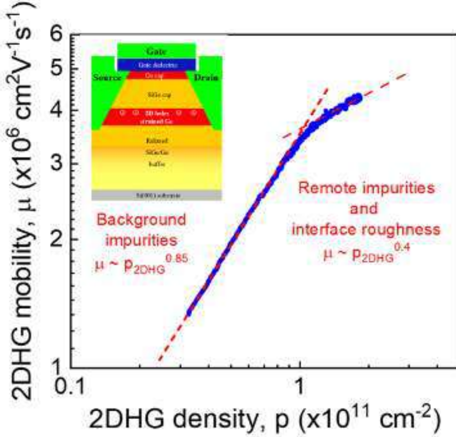

Fig. 1. 2DHG mobility versus 2DHG density in s-Ge QW measured at temperature of 290 mK. Insert shows a cross-section of the fabricated gated Hall-bar.

exponent, $\mu \sim p^{0.4}$. This dependence indicates that hole mobility in the high-density range is limited by some additional scattering mechanisms. Most likely, they are due to remote ionised impurities at the gate dielectric/semiconductor interface; or/and interface roughness at the s-Ge QW and $Si_{1-x}Ge_x$ barrier interface, or possibly other crystal imperfections.

We believe that the maximum mobility has still not been reached in s-Ge QW heterostructures and there is room for further improvements. Clearly, more detailed experimental and theoretical studies are required to understand microscopic mechanisms that limit hole mobility in s-Ge heterostructures. However, it is clear that the higher quality epitaxial growth provided by RP-CVD is the key factor that contributed to obtaining ~80 times higher 2DHG mobility in s-Ge QW structure grown by RP-CVD compared to the best one grown by solid source MBE (SS-MBE). This technology also results in improved quality of interfaces and a reduction in background ionized impurities and defects, not only in s-Ge, but also in the surrounding relaxed SiGe epilayers of the heterostructure. The value of RP-CVD technology becomes even more clear considering growth pressures are relatively high at 10-100 Torr, compared to the SS-MBE ones, which utilises ultra-high vacuum in the range of 10^{-9} – 10^{-10} Torr. This makes RP-CVD epitaxy more robust and economical and thus provides a credible path to large-scale fabrication technologies.

In order to appreciate the reported breakthrough, the historic evolution of 2DHG mobility in the group IV semiconductors at low temperatures is shown in Fig. 2.[7] The first MOD strained $Si_{1-x}Ge_x$ (s-$Si_{1-x}Ge_x$) QW heterostructures reported in 1984 were grown by SS-MBE and had 2DHG mobility of just 3,300 $cm^2V^{-1}s^{-1}$.[8] By 1996, this value was improved up to 16,800 $cm^2V^{-1}s^{-1}$ in a low Ge-content $Si_{0.87}Ge_{0.13}$ QW.[9] The large lattice mismatch between Ge and Si (4.17% at

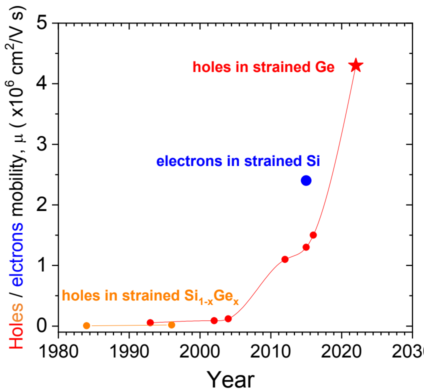

Fig. 2. The historic evolution of the highest 2D hole mobility in the group IV semiconductors at low temperatures, i.e. ≤4.2 K. The star marks result of this work. The highest 2D electron mobility in s-Si QW is shown for comparison (blue solid point).

293 K) made it impossible to grow QW heterostructure with high Ge content coherently on a Si substrate. For this reason, relaxed $Si_{1-x}Ge_x$ buffers were developed and utilized to produce high-quality s-Ge structures on Si. By 1993 the highest 2DHG mobility in s-Ge QW heterostructure was 55,000 $cm^2V^{-1}s^{-1}$ and the material was grown by SS-MBE.[10] The next improvement was achieved by using the Low Energy Plasma Enhanced CVD (LEPE-CVD). This growth technology was able to enhance hole mobility by a factor of ~2 up to ~100,000 $cm^2V^{-1}s^{-1}$, by 2002.[11] Development of RP-CVD provided a breakthrough in 2012, resulted in a x10 enhancement of 2DHG mobility up to ~10^6 $cm^2/V^{-1}s^{-1}$.[12] For comparison, we also show the highest mobility of a 2D Electron Gas (2DEG) in tensile strained Si (s-Si) QW. [5]

3. Conclusions

In conclusion, a record high mobility of free holes reaching 4.3×10^6 $cm^2/V^{-1}s^{-1}$ in strained germanium grown on a standard silicon wafer has been demonstrated that sets a new quality benchmark for the group-IV semiconductor materials. As a consequence, electrons are outperformed by holes in the group-IV semiconductor materials. The reported hole mobility in s-Ge is twice that of the best mobility of electrons in state-of the art strained Si QW. A similar situation has not been observed for any other semiconductor material. Due to the four-fold material quality improvement we reach a unique situation when holes outperform electrons by a combination of parameters, including, carrier mobility, effective g-factor, spin-orbit coupling. Therefore, it can be stated that the novel class of materials for cryogenic electronics as well for the quantum physics research and applications has emerged. This superior material system with a combination of unique properties, which are large and tuneable effective g*-factor, strong and tuneable spin-orbit interaction, low percolation density and small effective mass will lead to new opportunities for innovative quantum device technologies and applications in quantum as well as in classical electronics, optoelectronics, and sensors.

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Growth of ^{28}SiGe heterostructures with oscillating Ge concentrations for spin qubits by molecular beam epitaxy

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1. Introduction

Gate-defined quantum dots in isotopically engineered ^{28}SiGe heterostructures are a fast developing and promising material platform for quantum computing [1]. These heterostructures consist of strained Si quantum well (QW) layers coherently grown on relaxed $Si_{0.7}Ge_{0.3}$, where there strain partially lifts conduction band valley degeneracy. However, the remaining two-fold band energy degeneracy poses a challenge. A reliable integration of a big number of qubits in this material platform will require a technology that allows for a large and controllable valley splitting.

Several approaches to achieve this have been proposed and explored in the past, including atomically-flat interfaces and modifications of the QW barriers [2, 3]. However, most recently, an oscillating Ge concentration in the QW, a so called 'Wiggle QW', was proposed and demonstrated to achieve a large and tunable valley splitting, in heterostructures grown by chemical vapor deposition (CVD) [4]. Here we demonstrate and investigate the potential of growing such by ^{28}SiGe Wiggle QW test structures by molecular beam epitaxy (MBE), which allows for growth at lower temperatures and better compositional control.

2. Heterostructure Growth

$^{28}Si_{0.7}Ge_{0.3}$/^{28}Si/$^{28}Si_{0.7}Ge_{0.3}$ heterostructures were grown on fully-relaxed $Si_{0.7}Ge_{0.3}$ virtual substrates by MBE. Here, isotopically enriched ^{28}Si solid source material from the Avogadro project with a ^{29}Si concentration below 30 ppm and a high chemical purity, is employed [5]. The relaxed $Si_{0.7}Ge_{0.3}$ virtual substrates were covered with a Si cap, consequently a standard Si ex-situ wet-chemical cleaning procedure was utilized [6]; involving degreasing 5 min in acetone and isopropanol, 10 min in hot Piranha solution, 5 min in 0.5% HF solution, and a dip in deionized water. The substrates are loaded into an ultra-high vacuum system (~10^{-10} mbar base pressure) with less than a minute of air exposure in-between. In-situ annealing at 700°C for 10 min in vacuum and for 5 min including atomic hydrogen exposure at $3\cdot10^{-7}$ mbar was executed to get rid of most oxygen and carbon interface contamination. Growth was conducted at a constant temperature of 500°C for both $Si_{0.7}Ge_{0.3}$ and the Wiggle QW. A low and constant evaporation rate of 0.02 nm/s and 0.01 nm/s for the ^{28}Si and natural Ge was chosen, respectively. The Wiggle QW layer in $^{28}Si_{0.7}Ge_{0.3}$ was implemented by source shutter control. Shutter-free approaches were investigated, using a pure modulation of the evaporation rate, but these yielded less pronounced Ge oscillations.

The heterostructure surfaces exhibit an rms-roughness of around 200 - 300 pm, as determined by topography atomic force microscopy on a 2x2 µm scale. On a larger lateral scale, surface undulations in the nm-scale, associated to the cross-hatch pattern of the virtual substrate, are visible. No other topographic defects were noticed.

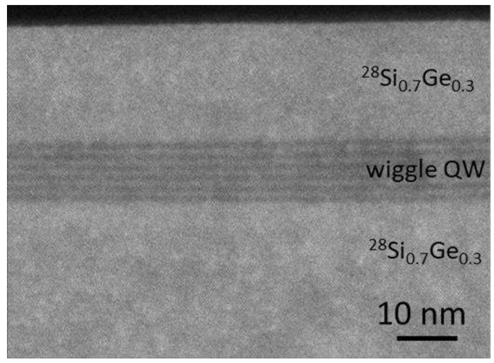

Fig. 1. High-angle annular dark-field (HAADF) image of a cross-section of a ^{28}SiGe heterostructure with a 'wiggle QW' layer exhibiting an oscillation wavelength of around 1.8 nm grown by MBE.

A (1 1 0) cross-section transmission electron high-angle annular dark-field image of a grown heterostructure is shown in Fig. 1. The oscillating Ge

concentration in the QW layer is striking and the wavelength of the oscillation is on average 1.85 nm.

The Ge concentration oscillations of the Wiggle QW layer were detectable in X-ray reflectivity measurements, but quantitative evaluation was difficult due to the cross-hatch pattern being in a similar order of magnitude as the oscillation wavelength of the Ge concentration.

3. APT analysis

The Ge concentration in the heterostructure was investigated by atomic probe tomography (APT) on the nm length scale, which is shown in Fig. 2a. For this purpose, a test structure with a shutter control to achieve a Ge oscillation with 1.8 nm (bottom QW layer) and 0.32 nm (top QW layer) wavelength was grown. In the test structure the average concertation of Ge in layers was around 20%, where the oscillation in the bottom layer goes from around 16 to 24%, while no oscillations can be observed in the top layer. The ^{29}Si concentration in the layers was around 70 ppm. Furthermore, APT revealed some carbon contamination on the interface to the virtual substrate.

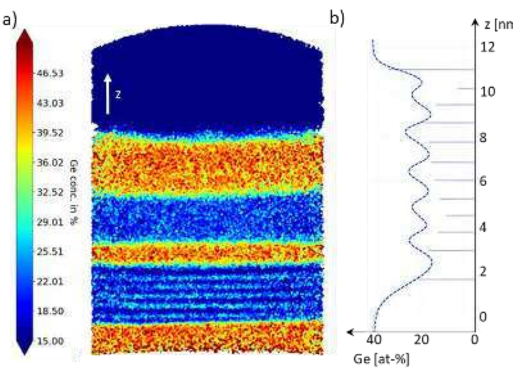

Fig. 2. a) shows the atom probe tomography on a ^{28}SiGe test structure exhibiting controlled Ge oscillations and b) shows the average steepness of the interfaces of the bottom layer.

4. Conclusions

^{28}SiGe heterostructures realizing a so called Wiggle QW with well-defined Ge concentration oscillation was demonstrated. While shutter-free epitaxy was feasible, the results utilizing partial growth interruptions and shutters were more promising. The heterostructures were of high structural quality. It is possible to achieve a high control of the wavelength of the Ge oscillations by MBE. However, full compositional control was not achieved yet.

Acknowledgements

We acknowledge Nikolay Abrosimov for providing us with highly-pure float zone grown ^{28}Si materials. This work was performed in the framework of the ”SiGe-Quant” project funded by the Leibniz Association.

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Conductivity type transition in high-purity germanium bulk materials

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1. Introduction

The invention of the point-contact germanium (Ge) transistor is one of the significant technological achievements of the 20th century with a profound impact on the revolution of electronic devices, computers, and communications during the past 75 years. But silicon (Si) soon dominated the semiconductor industry by replacing the Ge in transistor technology even though it possesses a lower intrinsic carrier mobility, but substantially better native oxide and more importantly its very high abundance in earth. Ge was later once again considered for n- and p-channel MOSFETs for higher mobility CMOS because the advent of high-k dielectrics material allowed the consideration of channel materials irrespective of the native oxide quality. Another important application of Ge, in which still dominating is the very high sensitivity radiation detectors operatable at low temperatures, since Ge is the purest material that could be prepared among all other known semiconductor materials. Fundamental properties such as purity, dislocation density, point and deep-level defects play an important role in the performance of the fabricated detectors. High-purity Ge (HPGe) crystals will generally have an unintentional impurity concentration in the range of 10^{10} to 10^{11} cm^{-3}. In this work, the electrical characteristics of the HPGe crystals (with a long-term view of a detector fabrication) were examined by HALL effect, current-voltage (I-V), and capacitance-voltage (C-V) measurements. Usually a p-type to n-type conversion is reported in the literature. Interestingly, we have observed in some crystals an n- to p-type transition that is encountered in a single growth experiment of HPGe.

2. Methods and Results

2.1. Crystal growth

High purity germanium crystal with 3-inch diameter was grown by the Czochralski (Cz) technique, the most preferred melt growth method for growing bulk crystals. The more details of the growth process were published elsewhere [1]. The starting Ge material for crystal growth was purified by the zone refining process. Both the zone refining, and crystal growth were carried out in a pure hydrogen (H_2) gas atmosphere. The crystals are usually grown in [100] direction. For investigations, square samples (7mm x 7 mm) with a thickness 1mm, from the wafers were prepared, by cutting of the crystal perpendicular to growth direction, (i.e. (100) plane). The crystals show n-type conductivity (Fig. 1), and some crystals exhibit p-type. For the examinations, three wafers were taken from top (A), middle (B) and bottom (C) parts of the crystal.

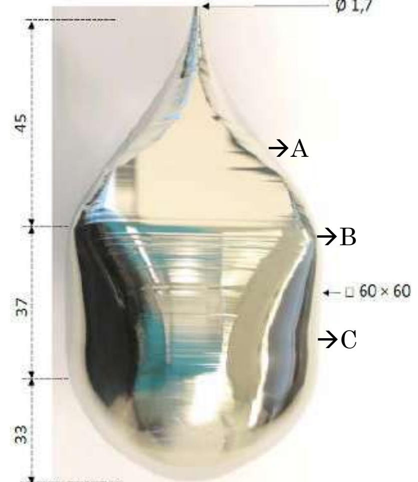

Fig. 1. A high purity Ge (n-type) single crystal.

2.2. HALL, I-V, C-V, PTIS and DLTS measurements

Hall effect measurements using the van der Pauw geometry were used to investigate the free carrier density, mobility, and resistivity of the grown HPGe crystals. The measurements were done on square-shaped samples taken from the center of the wafer from all the three parts of the crystals as mentioned above. The samples were etched with HNO_3 + HF and dried using nitrogen gas. The ohmic contacts are made at the corners of the samples using In-Ga eutectic alloy. Table-1 shows the Hall-effect measurements performed at liquid nitrogen (77K) temperature, displaying carrier type-transition within one crystal (samples 119). Carrier concentration with negative sign means n-type, with positive sign indicates p-type. Further, the measurements such as photo thermal ionization spectroscopy (PTIS) and deep level transient spectroscopy (DLTS) will also be performed to understand the unintentional impurities and the deep level defects present in the crystalline wafers. The electrical characteristics of the HPGe Schottky diode studied is shown in Fig. 2.

Table-1. 77K HALL effect measurement results

Samples	Resistivity (Ω·cm)	Carrier Concentration (cm^{-3})	Mobility ($cm^2/(V{\cdot}s)$)
119-A	390	-8.10×10^{11}	25,000
119-B	180	-1.20×10^{12}	32,000
119-C	38	$+6.20 \times 10^{12}$	38,000
121-A	4080	-5.85×10^{10}	33,900
121-B	2420	-1.83×10^{11}	19,800
121-C	331	-8.22×10^{11}	29,300

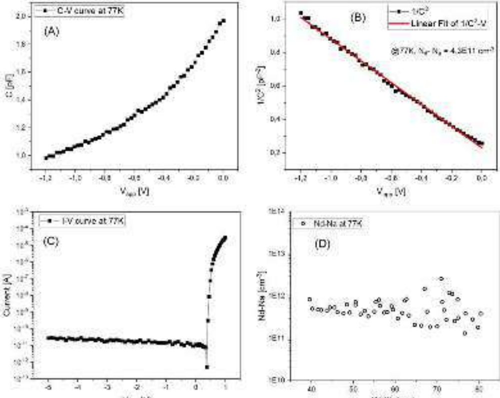

Fig. 2. HPGe (sample 119-B) Schottky diode characteristics.

2.3. Results and discussion

The Schottky contact was made using Au metal and the obtained built-in potential (V_{bi}) is 0.34V. Both the I-V (Fig. 2C) and C-V measurements (Fig. 2A) has been done at liquid N_2 temperature. The diode shows nonlinear I-V curve with very low leakage current of 50 pA range and the plot of $1/C^2$ Vs V curve gives a straight line showing uniform distribution of charge carriers across the sample (Fig. 2B). In the measured sample (119-B) the carrier concentration calculated from C-V curves is about 4.3×10^{11} cm^{-3}. But this value is one order less than those obtained by the Hall measurements in the similar samples. The space charge width of the fabricated diodes (Fig. 2D) is found to be 80 micrometers at -1.2V bias.

As mentioned earlier and can be seen from the table-1, some crystal shows an n-type at the top portion and then changing into a p-type at the tail portion during the single growth run (n-type to p-type transition) unlike the generally encountered p-type to n-type transition reported in the literature [2]. This may be attributed to the anomalous segregation of dominant acceptor impurities at the later stage of the growth process. The differences in the concentration of shallow donors or acceptors in the used starting material before the crystal growth might also play a dominant role and further, the reduction of defects like complex donors such as D (H, O) could be responsible for the change in the conductivity type along the crystal length within a crystal. It was also reported that the vacancy-group-V-impurity atom complexes (or the so-called donor-vacancy (DV) complexes) could lead to a n → p transition of the material as observed in the gamma-irradiated n-type Ge [3]. Such vacancy-type defects give raise to deep acceptor levels in the forbidden gap and their thermal stability depends on the size and concentrations of the group-V-impurity atoms. The DLTS investigations are being carried out. Presently, we are also working on to find a suitable ohmic material, larger contact area and to optimize the surface preparation procedure for these measurements.

The qualitative assessments of impurities in the ultra-low-level (ULL) concentrations by the PTIS technique showed the presence of common shallow acceptor/donor impurities like, Boron (B), Aluminum (Al), Phosphorus (P). Al and P are mainly found as dominating impurities. The existence of a complex donor D (H, O) may be suspected since hydrogen- and oxygen- complexes are expected to form while growing the crystal in H_2 gas atmosphere. The oxygen might likely come from the starting source material and might react with hydrogen on the surface of the melt. However, we didn't see D(H,O) related peaks in PTIS for the sample A and measurements on the other samples will also be continued.

3. Conclusions

An unusual carrier type conversion (i.e., n-type to p-type transition) in HPGe crystal grown by the Cz method under a H_2 gas atmosphere has been reported. The net free carrier concentration of the crystals is in the range of 6×10^{10} to 6×10^{12} cm^{-3} by HALL effect measurement. The concentration values obtained by the C-V measurements is 4×10^{11} cm^{-3}. The noted change in the conductivity type (n- to p- type) along the crystal length within a crystal could be attributed to the anomalous segregation of dominant acceptor impurities at the later stage of the growth process.

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Spin injection, transport and detection in Ge-based structures

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1. Introduction

The aim of spintronics is to exploit the spin degree of freedom to add new functionalities to electronic devices and boost their performances. Among semiconducting materials, germanium is one of the most appealing candidates for spintronic applications thanks to the 4% of lattice mismatch with Si that makes it compatible with the Si platform, the long electron spin lifetime and the optical properties matching the conventional telecommunication window. This latter feature calls for the investigation of spin-related properties of Ge by means of optical techniques. High efficiencies in spin generation and detection and reduced losses in spin transport are the fundamental building blocks in the perspective of embedding spintronic functionalities in the actual electronic technology. Here, we report on the investigation of spin generation, transport and detection in Ge-based platforms.

2. Methods

The absorption of circularly-polarized light at the direct bandgap of Ge generates a spin-polarized electron population in the semiconductor with a polarization as large as 50% [1]. Here, we exploit such a technique, the so-called optical orientation, to locally generate a spin-polarized electron population in Ge. The detection of such a population is performed by means of spin-charge interconversion (SCI) phenomena like the inverse spin-Hall effect [2] or the inverse Rashba-Edelstein effect [3], which provide for the conversion of a spin current in a detectable charge signal. Since both effects are produced by the spin-orbit coupling (SOC), we exploit several high-SOC materials (heavy metals or topological insulators) as spin detectors. It is worth mentioning that the SCI allows detecting a spin-polarized electron population without employing ferromagnetic materials.

2. Discussion

The exploited spin generation/detection scheme allows us to (i) gain insights into fundamental spin-related properties, and (ii) devise architectures for spin-transport modulation via external electric fields.

An example for the first case is the investigation of the dynamics of a spin population directly excited in Ge [4]. In this study we have probed the dependence of the SCI of Ge as a function of the electron's kinetic energy. The inferred SCI efficiency has been found to increase by about 3 orders of magnitude when the impinging photon energy was varied between 0.8 and 2.2 eV, reaching, in the best-case scenario, a value of about 0.1. Since, for increasing photon energies, the phonon contribution to spin scattering exceeds that of impurities, our findings indicate that the spin-to-charge conversion mediated by phonons is much more efficient than the one mediated by impurities.

In another experiment, [5] we have investigated SCI in a Bi/Ge structure as a function of the thickness of the Bi layer in the ultrathin film limit. In this study, we have unraveled the fundamental role of quatum confinment in tuning the SCI efficiency of Bi. Indeed, a sizable spin-charge interconversion has been shown to take place only in the ultrathin film limit (1 nm – 3 nm) in which Bi grows in the form of nanocrystals at the surface of Ge. Due to three-dimensional quantum confinement, those nanocrystals exhibit a highly resistive volume separating metallic surfaces where SCI takes place by inverse Rashba-Edelstein effect. As the film size increases, the Bi film becomes continuous and semimetallic, leading to the cancellation of SCIs occurring at opposite surfaces, which results in an average SCI that progressively decreases and disappears.

We have also employed the prototypical topological insulator Bi_2Se_3 as a spin detector [6]. Again, we probe the spin properties of the Bi_2Se_3/Ge interface by optically orienting a spin-population in Ge the diffuses toward the Bi_2Se_3, which acts as a spin detector. The comparison between experimental results and first-principles calculations allows us to ascribe the SCI signal to the hybridization of the topological surface states of Bi_2Se_3 with the Ge bands. Our results demonstrate that semiconductors constitute a very promising platform for the exploitation of topological insulators in spintronics, where, by gating the heterostructure, spin-to-charge conversion could in principle be tuned in magnitude and sign.

Alternatively, we explore nonlocal geometries

where the spin injection and detection points are spatially separated [7]. We employ a lithographycally defined Pt pad as spin detector, and a focused light beam raster scanning the sample as a spin source. In this way, we directly map the spin diffusion paths in Ge, demonstrating lateral spin transport in bulk Ge with spin-transport lengths as long as 10 μm in lightly n-doped Ge. This geometry is particularly interesting since it allows, in principle, spin manipulation in the channel between the spin injector and detector.

Indeed, we have recently expanded the nonlocal architecture to perform such a modulation by means of external electric fields [8]. A field directed antiparallel (parallel) to the spin-diffusion velocity can, in fact, largely increase (decrease) the spin-transport length compared with the zero-field case. We find that applying an electric field $E = 24$ V/cm along a 40 μm-long path in germanium results in about one order of magnitude modulation of the spin-polarized electrons entering the detector. Moreover, in the best-case scenario, we directly image a spin-transport length of about 40 μm. Comparable values in semiconductors have been predicted and observed only at cryogenic temperatures. The investigated scheme could thus modulate spin transport over long distances and is expected to reach fast timescales. Preliminary simulations predict that, for realistic electric field amplitudes, carrier mobility, and spin lifetime, modulation frequencies reaching 10 GHz can be attained. Our platform combines all the following characteristics, which make it extremely promising for the development of next generation spintronic devices: (i) room temperature operation; (ii) a large modulation of spin accumulation; (iii) spin-transport lengths that can be pushed above 40 micrometers; and (iv) application of moderate control electric fields, which is a key point for low power consumption operation. Hence, our work demonstrates that electric fields can be exploited for guiding spins over macroscopic distances and for realizing fast room temperature modulation of spin accumulation.

3. Conclusions

We have demonstrated the capability of Ge as a platform for spintronic studies, thanks to the high efficiency in spin generation, the long and tunable spin-transport length, and the possibility to epitaxially grow high-SOC materials that can be employed as spin detectors. Moreover, Ge-based nonlocal architectures can be devised as prototypical devices able to modulate the spin transport between the spin generation and detection points. Our results, thus, pave the way to the realization of spintronic devices adding functionalities to common electronic technology without the employment of ferromagnetic materials.

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Molecular beam epitaxy growth of ferromagnetic Heusler alloy films on SiGe(111) grown by Al-Ge-paste-induced liquid phase epitaxy

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1. Introduction

SiGe-based spintronics devices are expected to enhance the functionality of present Si electronics [1]. For the spin injection and detection into Ge, a ferromagnetic Heusler alloy/SC heterostructure is one of the fascinating structures because some of ferromagnetic Heusler alloys have high Curie temperature and high spin polarization [2]. So far, we have developed the epitaxial growth technique of Co-based Heusler alloy on Si(111)[3], Ge(111)[4] and SiGe(111)[5] substrate using low temperature molecular beam epitaxy (MBE).

Recently, using the Co-based Heusler alloy/SiGe Schottky tunnel contacts, we experimentally revealed an enhancement in spin diffusion length of the strained SiGe(111) layers due to the energy splitting of the conduction valleys [6,7]. To promote the study of Si-Ge-based spin devices, the strain engineering platform on the SiGe(111) should be further developed.

As a simple, low-cost, and high-speed formation technique of a SiGe layer, the liquid phase epitaxy (LPE) of SiGe(100) induced by annealing the Al-Ge paste on the Si substrate has been reported [8,9]. In this study, we explore the combination of MBE-growth of Co-based Heusler alloy films and LPE-growth of the SiGe(111) layer on Si(111) for SiGe-based spintronics devices.

2. LPE-growth of SiGe(111) with Al-Ge mixed paste

The growth procedure of LPE-SiGe was presented in Fig. 1(a). Al-Ge mixed paste (Toyo Aluminium) was coated on Si(111) substrate by screen printing technique, where the Al:Ge ratio in the paste was 7:3, followed by the thermal annealing at 1000ºC. During the annealing, the ternary solution of Al-Ge-Si was formed between the paste and Si substrate. In the cooling process, the solution was supersaturated, resulting in growth of the SiGe layer on Si(111). Here the thermal annealing was performed in Ar atmosphere to prevent the formation of Al oxide film and to obtain the continuous SiGe layer [8]. To remove the residue on the grown SiGe layer, the surface was polished and planarized by chemical mechanical polishing (CMP). We characterized the surface of the SiGe layer after the CMP by atomic force microscopy (AFM). Root-mean-square roughness of the surface was determined to be 0.95 nm over an area 1 × 1 μm^2. In addition, the continuous SiGe layer on Si(111) was observed by cross-sectional scanning electron microscopy (SEM)

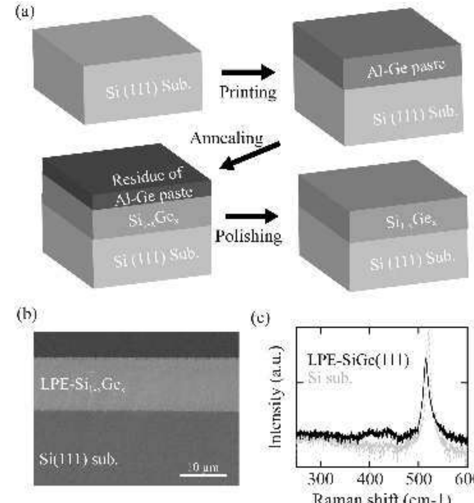

Fig. 1 (a)Schematic of sample preparation procedure of LPE-SiGe. (b) Cross-sectional SEM image of LPE-SiGe/Si(111). (c) Raman spectrum for the polished LPE-SiGe.

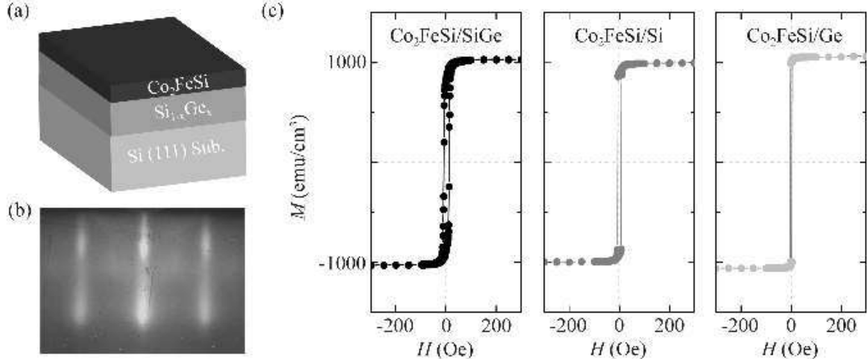

Fig. 2 (a) Schematic of the sample structure. (b) RHEED patterns of the surface for Co_2FeSi on LPE-SiGe. (c) *M-H* curves at 300 K for Co_2FeSi on LPE-SiGe(111), Si(111) [3], and Ge(111) [4] substrates.

combined with energy dispersive X-ray spectroscopy (EDX) [Fig. 1(b)]. To confirm the composition of the SiGe layer, Raman scattering spectroscopy was conducted. In Fig. 1(c), the peaks related to the SiGe film were observed at around 520 cm^{-1} (Si-Si mode) and 420 cm^{-1} (Si-Ge mode). The composition of the SiGe layer was estimated to be ~0.095 from the peak position of the Si-Si mode, where we assumed that the strain in the SiGe layer is fully relaxed because strain relaxation of SiGe layers on Si(100) substrate grown by the same method was confirmed by X-ray diffraction reciprocal space mapping in a previous report [9]. The value of composition is consistent with that measured by SEM-EDX. Therefore, the epitaxial growth of the $Si_{0.9}Ge_{0.1}$(111) layer was achieved by the annealing Al-Ge paste on Si(111).

3. MBE-growth of Co_2FeSi on LPE-SiGe(111)

Prior to the growth of a Co-based Heusler alloy, the surface of the LPE-SiGe(111) was chemically cleaned with HF solution to remove the native oxide and contamination. After the cleaning, the LPE-SiGe(111)/Si(111) was loaded into the MBE chamber (base pressure: ~1×10^{-9} Torr) followed by heat treatment in the chamber. On the SiGe(111) layer, a 25-nm-thick Co_2FeSi layer was grown below 80ºC by MBE [Fig. 2(a)], where the Co, Fe, and Si were coevaporated by effusion cell to precisely control the composition of Co_2FeSi Heusler alloy [2-4]. The surface of Co_2FeSi was confirmed by *in-situ* reflection high energy electron diffraction (RHEED). In Fig. 2(b), the streak RHEED patterns are observed, indicating the epitaxial growth of the Co_2FeSi layer on the SiGe layer. We examine magnetic properties by using vibrating sample magnetometry (VSM). Figure 2(c) shows the field dependent magnetization (*M-H*) curves measured at 300 K for the MBE-Co_2FeSi film on the LPE-SiGe(111), together with those on Si(111) and Ge(111) commercial substrates. The values of saturation magnetization and coercive field are ~1030 emu/cm^3 and ~11 Oe, respectively, and are consistent with those for the epitaxial Co_2FeSi layer on Si(111) and Ge(111) commercial substrates. The large saturation magnetization and sharp magnetization reversal mean that the Co_2FeSi film with a good film quality is grown even on the LPE-$Si_{0.9}Ge_{0.1}$(111) layer.

For the spin injection and detection in the SiGe layer, the surface roughness of the LPE-SiGe on Si(111) should be improved by optimizing polishing conditions because an atomically abrupt Co-based Heusler alloy/SiGe interface is required to achieve the highly efficient spin injection and detection [10].

4. Conclusions

We have explored the combination of MBE-growth of Co_2FeSi films and LPE-growth of the SiGe(111) layer on Si(111) for SiGe-based spintronics devices. Epitaxial Co_2FeSi films with good magnetic properties were obtained even on the LPE-$Si_{0.9}Ge_{0.1}$(111). This study will open a way for SiGe spintronic technologies with simple, low-cost, and high-speed formation processes.

Acknowledgements

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Electric Field Manipulation of Spin Currents in Silicon Platforms

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1. Introduction

The implementation of spin-based devices in bulk Si substrates represents a crucial goal for spintronics to improve the functionalities of CMOS-compatible circuits without transforming the electronics supply chain [1, 2]. In this context, spin injection and detection in silicon heterostructures have been developed in recent years, exploiting lateral spin valves in three and four terminal configurations with high injection and detection efficiencies in a vast range of doping concentrations and temperatures [1, 2]. Alternatively, optical spin injection has been demonstrated to be efficient for promoting spin-polarized electrons at the indirect gap in bulk and nanostructured silicon, by exploiting phonon-mediated transitions allowed by dipole selection rules [3]. However, the manipulation of the spin degree of freedom of carriers directly inside the semiconductor without employing power-consuming magnetic fields remains a more difficult task. This is mainly due to the low spin-orbit coupling that prevents spin precession at least in bulk Si [1]. Nevertheless, an advantage of the low spin-orbit interaction consists in the fact that spin currents can survive for long distances inside the semiconductor, with spin lifetimes around tens of nanoseconds at room temperature [1, 3]. For this reason, published studies have primarily concentrated on the large spin diffusion length that makes this material appealing for spin interconnects [3, 4]. Conversely, studies aimed to realize spin-based logic gates have been limited to high-Z or magnetic materials that should eventually be integrated onto the silicon platform [5]. In this work, we propose a non-local architecture where the electrical control of spin-dependent output signals can be directly realized in Si by manipulating the spin current rather than the spin itself, taking advantage of the semiconductor spin-transport properties.

The spin diffusion length L_s that we measure in our silicon platform is $L_\mathrm{s} \approx 12$ um, in accordance with the literature [3]. The latter can be enhanced (diminished) about a factor 3 by applying an in-plane electric field that fosters (hinders) the spin-polarized electrons diffusion. In a non-local geometry, this results in the switching of the spin-dependent output signal through a control potential voltage.

2. Methods

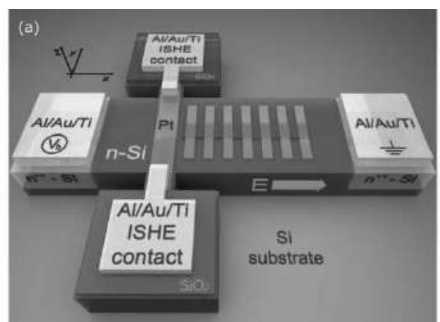
The non-local architecture for spin current injection, manipulation, and detection at room temperature in *n*-doped bulk Si ($N_\mathrm{d} \approx 1 \times 10^{15}\ \mathrm{cm}^{-3}$) is sketched in Fig. 1(a). The spin generation is obtained by optical orientation [6], illuminating with circularly polarized light at the indirect gap of bulk Si at the edges of a set of Pt stripes. In this way, we generate a spin-population at a highly-localized position in the sample [7]. The detection stage consists in a Pt pad grown onto the Si substrate where spin-to-charge conversion is obtained by means of the inverse spin hall effect (ISHE) [7, 8]. Referring to Fig. 1(a), the first left Pt pad is used as spin detector: two Al/Au/Ti contacts enable the measure of the voltage drop ΔV due to the ISHE. The Al/Au/Ti contacts are electrically isolated from the Si substrate by a SiO_2 interlayer. The Si substrate is firstly etched to realize a mesa over which a series of Pt pads is deposited that are used for promoting spin-polarized carriers below the pad edges. Spin carriers then undergo drift/diffusion, generating spin currents that are revealed when they reach the Pt detector. Because of the finite spin lifetime, spin-polarized carriers arrive at the detector in smaller or larger quantities depending on the direction of the applied electric field. The bias voltage is applied between two Al/Au/Ti ohmic contacts, deposited after using the spin-on-dopant (SOD) method to severely dope the area beneath the electrodes; in this way, the Schottky barrier at the Ti/Si interface has been suppressed [9]. We have investigated the device performances in both the spin drift regime with applied voltage V up to 7.5 V (electric field $E = 35\ \mathrm{V/cm}$) and the spin diffusion regime.

3. Results

The reflectivity R and the ISHE signal ΔV that we measure while locally illuminating the Pt stripes are shown in Fig. 1(b) and (c). The peaks of the profile are fitted to estimate L_s within a 1D spin diffusion model [7]:

$$\Delta V = \Delta V_0 e^{-\frac{x}{L_\mathrm{s}}} \qquad (1)$$

without applied electric field (see Fig. 1(d)). We show that electric fields antiparallel (parallel) to the electrons diffusion velocity can enhance (reduce) the *spin*



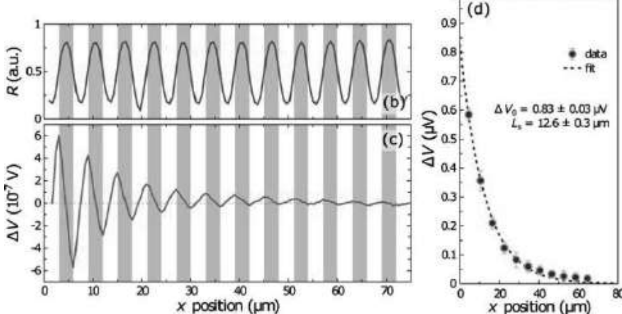
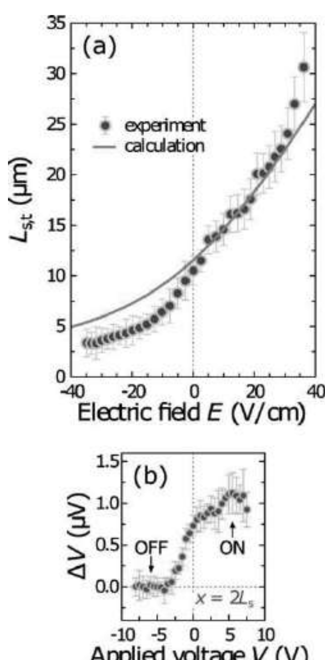


Figure 1. (a) Investigated sample structure (not in scale). Pt injectors are grown at various distances from the ISHE detector (the first Pt stripe on the left). Two Al/Au/Ti pads are used to electrically contact the detector and probe the voltage drop ΔV. At the end of the Si mesa, two Al/Au/Ti ohmic contacts are deposited to apply an electric field E along the sample's x axis. (b) Reflectivity R and (c) ISHE signal ΔV profiles measured while illuminating the Pt stripes along the x axis. (d) ISHE signal ΔV as a function of the distance from the Pt detector, evaluated at correspondence with the left edge of each Pt stripes. On the sample, the light spot is diffraction limited employing an objective with 0.7 NA and the light power results 7 uW.



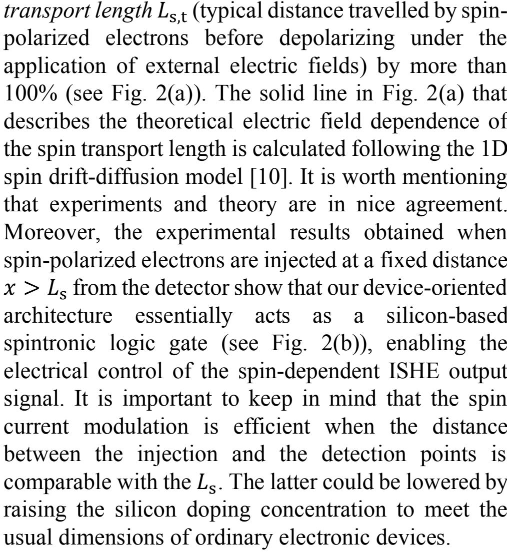


Figure 2. (a) Experiments (dots) and calculations (solid line) of the spin transport length $L_{s,t}$ dependence on the electric field E. (b) The ISHE output signal as a function of V for optical spin injection at a distance $2L_s$ from the Pt detector.

transport length $L_{s,t}$ (typical distance travelled by spin-polarized electrons before depolarizing under the application of external electric fields) by more than 100% (see Fig. 2(a)). The solid line in Fig. 2(a) that describes the theoretical electric field dependence of the spin transport length is calculated following the 1D spin drift-diffusion model [10]. It is worth mentioning that experiments and theory are in nice agreement. Moreover, the experimental results obtained when spin-polarized electrons are injected at a fixed distance $x > L_s$ from the detector show that our device-oriented architecture essentially acts as a silicon-based spintronic logic gate (see Fig. 2(b)), enabling the electrical control of the spin-dependent ISHE output signal. It is important to keep in mind that the spin current modulation is efficient when the distance between the injection and the detection points is comparable with the L_s. The latter could be lowered by raising the silicon doping concentration to meet the usual dimensions of ordinary electronic devices.

4. Conclusions

As a result, the output ISHE voltage drop of the non-local device can be electrically manipulated to be two logic levels by the action of an external bias voltage. This is achieved taking advantage of the fact that spin currents can be effectively controlled by applying an electric field along the direction of motion of the spin-polarized carriers. These outcomes push towards the design and engineering of a novel class of Si-based spintronic devices for spin-dependent logic operations.

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Enhancement in Spin Transport Length in Strained *n*-$Si_{0.1}Ge_{0.9}$(111)

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1. Introduction

One of the semiconductor spintronics devices, spin MOSFET, is expected for novel logic and memory architectures with low power consumption [1]. Group-IV semiconductors such as Si and Ge are good candidates for channel materials for the spin MOSFET because they are compatible with Si-CMOS technologies.

Thus far, electron spin relaxation in Si and Ge has been theoretically predicted to be governed by intervalley spin-flip scattering among the conduction-band valleys [2,3]. Recent experimental studies revealed that spin diffusion length (λ_s) and spin lifetime (τ_s) in *n*-type Si (*n*-Si) [4] and *n*-Ge [5-7] were clearly interpreted in these theories. To reduce the intervalley spin scattering and to enhance λ_s and τ_s, Tang *et al*. have theoretically proposed that lifting the degenerate valleys in the channel through a lattice strain is effective [2].

In this study, we experimentally find the significant effect of strain on spin transport in Ge-rich *n*-$Si_{0.1}Ge_{0.9}$, which exhibits Ge-like conduction bands, and demonstrate an enhancement in the spin transport length at room temperature by the strain-induced valley splitting [8,9].

2. Spin Transport in Strained *n*-$Si_{0.1}Ge_{0.9}$

We grew 70-nm-thick (111)-oriented *n*-$Si_{0.1}Ge_{0.9}$ and reference 140-nm-thick *n*-Ge spin transport layers on a Ge buffer layer/Si(111) by molecular beam epitaxy (MBE) [10]. For the *n*-$Si_{0.1}Ge_{0.9}$ layer, coherent growth and in-plane biaxial and tensile strain over 0.6% are confirmed by two-dimensional x-ray diffraction (XRD) reciprocal space map (RSM) [9]. Carrier concentrations (*n*) are determined to be ~1×10^{18} cm^{-3} by Hall effect measurements for both layers. Then, we fabricated lateral spin valve (LSV) devices with spin injection/detection contacts of Co-based Heusler alloys (Co_2MnSi or $Co_2FeAl_{0.5}Si_{0.5}$) with a δ-doping and an Fe atomic layer insertion [6,11],

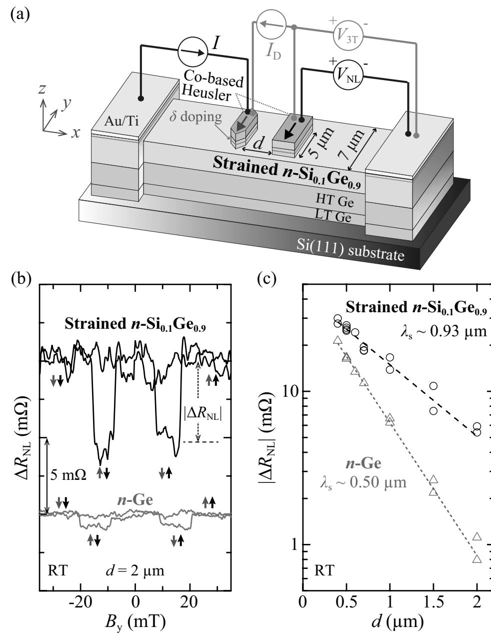

Fig. 1. (a) Schematic of the fabricated Co-based Heusler/*n*-$Si_{0.1}Ge_{0.9}$-based LSV device. (b) Nonlocal spin transport signals (ΔR_{NL}) with $d = 2$ μm and (c) *d* dependence of $|\Delta R_{NL}|$ for the strained *n*-$Si_{0.1}Ge_{0.9}$ and *n*-Ge channels at room temperature.

as shown in Fig. 1(a), where the edge-to-edge distance (*d*) between the spin injector and the detector was varied from 0.4 to 2 μm. The detailed fabrication process has been described in [8,9].

To estimate values of λ_s, nonlocal spin transport signals ($\Delta R_{NL} = \Delta V_{NL}/I$) are measured in four-terminal configuration in Fig. 1(a) by applying in-plane magnetic fields (B_y). For both LSV devices with the *n*-$Si_{0.1}Ge_{0.9}$ and *n*-Ge channels, hysteretic changes in ΔR_{NL} depending on magnetization switching between parallel and antiparallel states are clearly observed in Fig. 1(b). For both *n*-$Si_{0.1}Ge_{0.9}$ and *n*-Ge, $|\Delta R_{NL}|$ is found to decay exponentially with increasing *d*, as

shown in Fig. 1(c). Notably, the d dependence of $|\Delta R_{NL}|$ in n-$Si_{0.1}Ge_{0.9}$ is smaller than that in n-Ge. The values of λ_s in the strained n-$Si_{0.1}Ge_{0.9}$ and n-Ge are estimated to be ~0.93 μm and ~0.50 μm, respectively, by fitting to the exponential decay [$|\Delta R_{NL}| \propto \exp(-d/\lambda_s)$ [12]]. The two-fold increase in λ_s for the strained n-$Si_{0.1}Ge_{0.9}$ indicates suppression of spin relaxation by strain-induced L-valley splitting. Although the $Si_{0.1}Ge_{0.9}$ has Ge-like conduction-band structure, this value is comparable to that ($\lambda_s \sim 0.95$ μm [4]) in n-Si.

We elucidated the values of τ_s from the relation, $\lambda_s = \sqrt{D\tau_s}$, where D is the diffusion constant calculated from the n and mobility (μ). The estimated τ_s of ~0.27 ns in the strained n-$Si_{0.1}Ge_{0.9}$ is also larger than that ($\tau_s \sim 0.15$ ns) in the n-Ge. From the above, we conclude the enhancement in λ_s attributes not only to the enhancement in D but to the enhancement in τ_s [9].

3. Enhancement of Spin Transport Length

If an electric-field (E) is applied to the spin-transport semiconductor channels, the value of spin transport length (L_s) as a function of E can be represented using the following equation [13]:

$$L_s(E) = \left(\frac{eE}{2\varepsilon_d} + \sqrt{\left(\frac{eE}{2\varepsilon_d}\right)^2 + \left(\frac{1}{\lambda_s}\right)^2}\right)^{-1}, \quad (1)$$

where e is the elementary charge and ε_d ($= eD/\mu$) is an energy scale that controls the strength of the spin drift. On the basis of this, we investigate the spin-drift effect on L_s in the strained n-$Si_{0.1}Ge_{0.9}$ and n-Ge. Here the spin-drift-transport signals ($\Delta R_{3T} = \Delta V_{3T}/I_D$) are measured in three-terminal configuration in Fig. 1(a). The values of L_s are estimated from d dependence of ΔR_{3T} at various values of I_D ($\propto E$). Figure 2 shows the E dependence of L_s at room temperature, where λ_s is plotted at $E = 0$ and $E < 0$ means down-stream spin-drift transport. The estimated L_s for the strained n-$Si_{0.1}Ge_{0.9}$ is substantially enhanced with increasing $|E|$, reaching ~5 μm under the electric field of $E \sim -1.4\times10^3$ V/cm, while the n-Ge shows relatively small $L_s \sim 2$ μm under the same value of E. The calculated $L_s(E)$ using Eq. (1) is depicted as dashed curves in Fig. 2, where ε_d = 39 meV and $\lambda_s \sim 0.93$ μm for the strained n-$Si_{0.1}Ge_{0.9}$ and ε_d = 39 meV and $\lambda_s \sim 0.50$ μm for the n-Ge are used. The strain-induced enhancement in L_s is roughly reproduced using the enhancement in λ_s in Eq. (1).

The suppression of the intervalley spin scattering in the strained n-$Si_{0.1}Ge_{0.9}$ is induced by the energy difference (ΔE) between the Fermi level ($E_F \sim 23$ meV for $n \sim 1\times10^{18}$ cm^{-3}) in the one-fold lower-energy L valley along [111] and the valley energy splitting of ~55-90 meV [14,15], as depicted in the inset of Fig. 2. The observed strain-induced enhancement in λ_s and L_s attributes to sufficiently large ΔE compared to $k_BT \sim 26$ meV at room temperature.

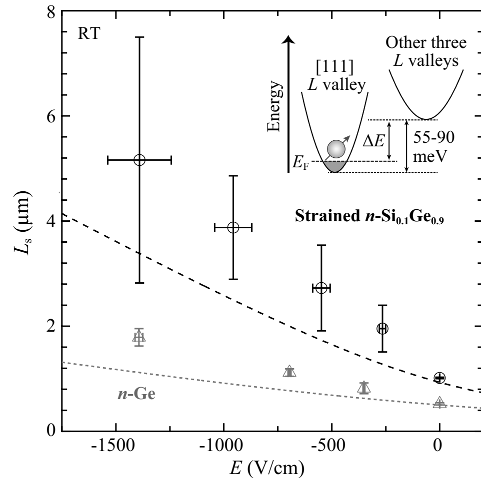

Fig. 2. L_s as a function of E for the strained n-$Si_{0.1}Ge_{0.9}$ and n-Ge at room temperature. The dashed curves are simulated data using Eq. (1). The inset shows a schematic of conduction-band L valleys in the strained n-$Si_{0.1}Ge_{0.9}$.

4. Conclusion

We experimentally studied the effect of strain on the spin transport. We found the λ_s for the nonlocal spin transport and L_s for the spin-drift transport in the strained n-$Si_{0.1}Ge_{0.9}$ are much larger than those in the n-Ge at room temperature. The enhancement in λ_s and L_s indicates the suppression of the intervalley spin scattering by the sufficient energy difference between the strain-induced valley-energy splitting and E_F. Therefore, the strain effect on the spin transport is useful for developing semiconductor spintronic applications.

Acknowledgements

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Optical Spin Injection and Coherent Control in GeSn Semiconductors

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1. Introduction

The quantum interference between two independent absorption pathways can be exploited to enable ballistic charge and spin current injection in semiconductors, in a process of coherent control. These injected currents, dependent on the polarization and relative phase of the beams, have stimulated interest in various research areas, such as the implementation of qubit-photon interfaces relevant to quantum communication [1], and generation of spintronic THz emission [2], among others. The initial coherent control studies have focused on GaAs, Si and Ge. The latter, with its stronger spin-orbit coupling and long spin lifetime, is of particular interest for optical injection at telecom wavelengths.

By reducing the direct gap, alloying Sn with Ge could enable optical spin injection and coherent control in the entire mid-infrared region, thus offering the prospect of quantum coherent manipulation in the molecular fingerprint region. $Ge_{1-x}Sn_x$ is an emerging alloy which properties remain to be explored [3], even though recent studies suggest a long spin lifetime and larger spin-orbit coupling, relevant to spintronics.

In this work, carrier, spin, current and spin current injection in bulk $Ge_{1-x}Sn_x$ with a Sn content up to 20% are theoretically investigated. The two-color ω and 2ω coherent control scheme is evaluated within a 30-band k·p model semiclassical framework.

2. Theoretical framework

A rigorous framework based on a full-zone 30-band k·p model is implemented to compute the carrier and spin injection processes in $Ge_{1-x}Sn_x$. The coverage of the entire Brillouin zone allows the study of the high-energy E_1 transition processes, located in the Γ-L direction. The band structure of Ge and $Ge_{0.86}Sn_{0.14}$, as computed with the 30-band k·p model, is shown in the panel (a) of Fig. 1. Alloying Sn with Ge lowers the split-off band and the first conduction band. In panel (b), the plot of the bandgap energy as a function of Sn content shows that the gap at Γ covers the full mid-infrared region (3μm-8μm).

A semiclassical framework, developed under the independent particle approximation, is employed to calculate various optical response tensors related to carrier and spin injection processes. The contribution from indirect transitions is neglected since direct processes are much stronger. Furthermore, the reciprocal space integration is realized with an improved linear tetrahedron method, and point-group symmetry properties of $Ge_{1-x}Sn_x$ are exploited to reduce the required computation time and memory.

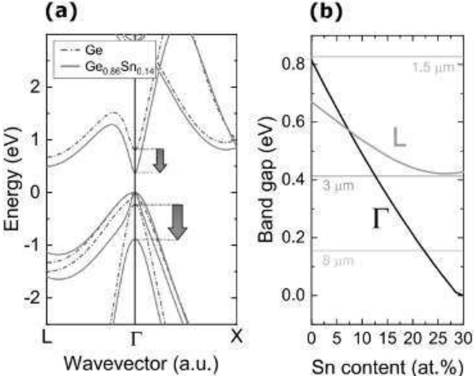

Fig. 1. (a) Band structure of Ge and $Ge_{0.86}Sn_{0.14}$. (b) Bandgap of $Ge_{1-x}Sn_x$ as a function of Sn content at the L and Γ valleys. Reprinted from [4].

3. Results and discussion

3.1. One and two-photon absorption

Under the studied scheme, electrons in the material can be excited to the conduction band by either one-photon absorption of a 2ω beam, or two-photon absorption of an ω beam. The theoretical framework is used to evaluate carrier and spin injection generated by these two processes in $Ge_{1-x}Sn_x$, at a few selected Sn compositions in the range of 0% to 20%. The degree of spin polarization (DSP) is then extracted by dividing the spin injection by the carrier injection, as shown in the following formula, valid in the case of one-photon absorption:

$$DSP^z = (2S^z_1) / (\hbar\, n_1), \qquad (1)$$

with the one-photon spin injection S^z_1 and one-photon carrier injection n_1.

The calculations showed that, in addition to the expected reduction of the direct bandgap, the incorporation of Sn into Ge leads to an increase of the DSP at the E_1 resonance. From a 20% one-photon

electron DSP in Ge at E_1, a 34% DSP is reached for $Ge_{0.83}Sn_{0.17}$. In the case of two-photon absorption, a similar formula to the one in (1) is used, and the results are presented in Fig. 2.

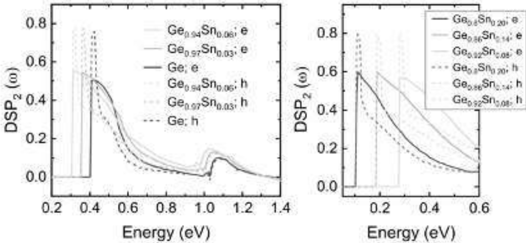

Fig. 2. The two-photon DSP of carriers injected in $Ge_{1-x}Sn_x$, for left-circularly polarized light at <001> incidence. The plain (dashed) curves show the electron (hole) spin. The sign of the hole DSP is reversed. Reprinted from [4].

At the band edge, when the Sn content increases, the two-photon electron DSP goes beyond the 53% value obtained in Ge, to reach a 60% maximum DSP for GeSn with a Sn content above 14%.

3.2. Coherent control

The quantum interference between the one-photon and two-photon absorption pathways induces charge and spin ballistic currents in the material. These coherently controlled currents are calculated with the theoretical framework for three different polarization configurations. In the case of colinear beams' polarizations, a relatively strong charge current is injected; the response tensor results are presented in Fig. 3.

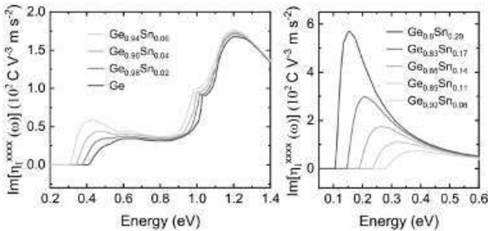

Fig. 3. The electron contribution to the component η_I^{xxxx} of the charge current injection tensor η_I in $Ge_{1-x}Sn_x$, as a function of photon energy $\hbar\omega$. Reprinted from [4].

As the $Ge_{1-x}Sn_x$ is enriched with Sn, an augmentation of charge current injection is observed at the band edge, which is almost exponential relatively to the Sn content. This sharp evolution is attributed to the reduction of carrier effective masses caused by the incorporation of Sn.

In the case of cross-linear beams' polarizations, a relatively strong spin current is optically injected by coherent control. The results are shown in Fig. 4.

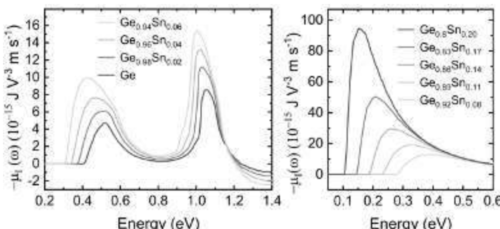

Fig. 4. The electron contribution to the component μ_I^{xyxxz} of the spin current injection pseudotensor μ_I in $Ge_{1-x}Sn_x$ as a function of photon energy $\hbar\omega$. Reprinted from [4].

Similarly to charge current injection, with the incorporation of Sn in Ge, there is a massive increase of spin current injection at the band edge, and also at the E_1 resonance.

4. Conclusions

The theoretical investigation of carrier, spin, current, and spin current optical injection in $Ge_{1-x}Sn_x$ has been performed. Focusing on a Sn content in the 0% to 20% range allowed a mapping of the entire mid-infrared region with the direct gap of these alloys. Coherent control was studied within the two-color scheme, with two beams of frequencies ω and 2ω. It was found that the incorporation of Sn in Ge significantly enhances the one-photon DSP at the E_1 resonance. Moreover, the band edge value of two-photon DSP increases up to 60% for alloys with more than 14% of Sn, which exceeds the 53% value in Ge. Another consequence of adding Sn is the exponential magnitude increase of charge and spin current injection close to the band edge. Overall, the results demonstrate that $Ge_{1-x}Sn_x$ has potential as a platform for tunable coherent control in the molecular fingerprint region, relevant to quantum sensing.

Acknowledgements

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Detection of magnetoresistance effect in all-epitaxial $Co_2MnSi/Ge/Co_2MnSi$ vertical spin-valve devices on Si(111)

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1. Introduction

For future semiconductor-based spintronic applications with low power consumption, spin-MOSFET with a group-IV semiconductor channel such as Si or Ge is one of the most attractive devices [1]. Vertical spin-valve (VSV) devices with ferromagnet (FM)/Ge/FM trilayer structure have some advantages for the spin-MOSFET because they are compatible with CMOS transistors and Si photonics [2] in addition to the compatibility of high integration. Recently, we have detected two-terminal magnetoresistance (MR) effect with over 1 % at room temperature for all-epitaxial VSV devices with a Ge intermediate layer and a bottom Co_2FeSi (CFS) [3], in which CFS is one of the Co-based Heusler alloys with high spin polarization [4].

Thus far, lots of Co-based Heusler alloys have been utilized for spintronics devices. In particular, Co_2MnSi (CMS) is a very famous Heusler alloy for magnetic tunnel junction (MTJ) devices [5,6]. However, CMS/Ge/CMS VSV structures have not been achieved because it has been difficult to crystalize CMS by a low-temperature growth method [7].

In this study, using the combination of solid phase epitaxy (SPE) and molecular beam epitaxy (MBE), we demonstrate VSV structures with an epitaxial CMS/Ge/CMS on a Si platform, as shown in Fig. 1(a). Even at room temperature, we observe MR effect meaning the spin-dependent transport via the Ge intermediate layer.

2. Growth and characterizations

We explain the growth procedure of CMS/Ge/CMS vertical structures on Si. First, a 240-nm-thick Ge layer was grown on a Si(111) substrate utilizing a two-step growth technique by MBE [8]. Next, a Fe_3Si layer was grown as a buffer layer [9] and a 5-nm-thick Co_2MnSi layer as a bottom electrode [7] was grown by MBE. The surface crystal structure was confirmed by *in-situ* reflection high energy electron diffraction (RHEED).

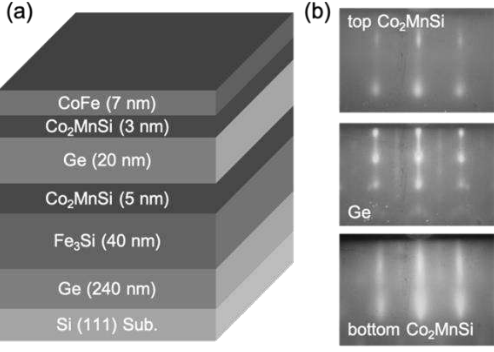

Fig. 1. (a) Schematic of the grown $Co_2MnSi/Ge/Co_2MnSi$ structure on $Fe_3Si/Ge/Si(111)$. (b) RHEED patterns of the surface for top Co_2MnSi, intermediate Ge, and bottom Co_2MnSi layers during the growth.

We clearly observe two-dimensional epitaxial growth of the bottom Co_2MnSi layer as shown in the bottom of Fig. 1(b). Then, the surface of the Co_2MnSi was terminated with a 0.3-nm-thick Si layer to epitaxially grow a Ge layer [10]. On top of the Si-terminated CMS(111), we grew a 20-nm-thick Ge layer by SPE and MBE to obtain the smooth surface even for low temperature growth [11]. A RHEED image of the surface during the Ge growth also maintains streaks [middle of Fig. 1(b)], indicating the epitaxial growth of the Ge layer on the bottom CMS. Furthermore, the surface of the Ge intermediate layer was terminated with 0.7-nm-thick Fe to induce the crystallization of a top CMS layer. On top of the Fe-terminated Ge layer, a 5-nm-thick CMS layer as a top electrode was grown below 80 °C [7]. Finally, we grew a 7-nm-thick CoFe layer to make the difference in coercivity between the top and bottom CMS layers. Although the RHEED images of the Ge intermediate layer and the top Co_2MnSi layer include slightly spotty patterns, we find all-epitaxial CMS/Ge/CMS structures on a Si platform.

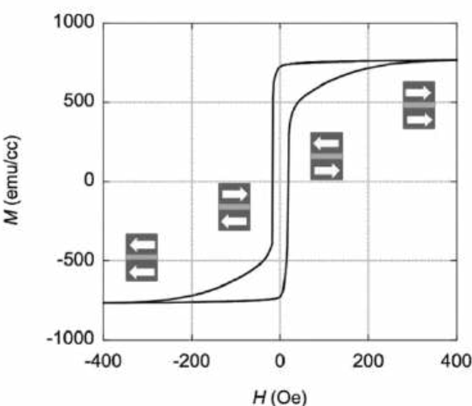

Fig. 2. Room-temperature *M-H* curve of an all-epitaxial CoFe/Co_2MnSi/Ge/Co_2MnSi/Fe_3Si structure. The insets mean the magnetization states between the top and bottom Co_2MnSi layers.

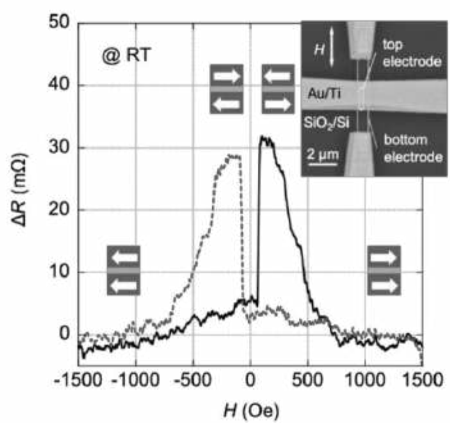

Fig. 3. Room-temperature MR curve for a VSV device with the Co_2MnSi/Ge/Co_2MnSi structure. The inset is an SEM image (top view) of a fabricated VSV device.

Figure 2 shows a magnetic field (*H*) dependence of magnetization (*M*) (*M-H* curve) at room temperature for an all-epitaxial CoFe/CMS/Ge/CMS/Fe_3Si structure on Ge/Si(111). We observe a difference between the two magnetization states between the top CoFe/CMS and the bottom CMS/Fe_3Si layers. Also, the value of the saturation magnetization is nearly consistent with the theoretical value. Therefore, we conclude that the grown CMS/Ge/CMS vertically stacked structure is successfully obtained.

3. Magnetoresistance measurements

To measure spin-dependent transport properties, we processed the all-epitaxial CoFe/CMS/Ge/CMS/Fe_3Si structure into VSV devices. A scanning electron micrograph image (top view) of a fabricated VSV device is shown in the inset of Fig. 3. To realize the antiparallel magnetization state between the top CoFe/CMS and bottom CMS/Fe_3Si electrodes for detecting spin-dependent transport properties, we formed the point-end-shaped CoFe/CMS top contact with a junction size of ~0.66 μm^2 and the wire-shaped CMS/Fe_3Si bottom one.

Using a four-terminal dc method, we electrically measure MR effect under applying in-plane *H* along the long axis of the wire-shaped electrodes. Figure 3 shows the *H*-dependent resistance change (ΔR) at room temperature. We obtain a clear hysteretic curve depending on parallel and anti-parallel magnetization states between the top CoFe/CMS and bottom CMS/Fe_3Si contacts. This means that MR effect is observed even in the CMS/Ge/CMS structure at room temperature. The MR value is still approximately 0.03 % because the intermediate Ge layer is *p*-type conduction having a small spin diffusion length of ~8.4 nm [12]. We should further enhance MR values in VSV devices with *n*-type Ge having a large spin diffusion length of ~400 nm [13] at room temperature. In future, the growth of P-doped Ge layers will also be explored on top of the bottom CMS layer.

4. Conclusion

We have achieved the vertically stacked and all-epitaxial CMS/Ge/CMS structure on a Si platform. We clearly detected MR effect at room temperature in the fabricated Ge-based VSV devices with CMS.

Acknowledgements

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Towards Si-based Topology by Design: The Emergence of Quantum Phases in GeSn Heterostructures

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1. Introduction

Topological phases of solid-state electron systems look poised to provide solutions that will revolutionize information technologies [1]. One of the most stringent hindrances to translate topologically enriched devices from research lab to scale-up production remains the recurrent use of environmentally-polluting or resource-critical materials. To overcome these limitations, we propose a practical silicon-based architecture that spontaneously sustains topological properties, while being compatible with the high-volume manufacturing capabilities of modern microelectronic foundries [2]. Here we show how $Ge_{1-x}Sn_x$ alloys, an emerging group IV semiconductor, can be engineered into junctions that demonstrate a broken gap (BG) alignment. We predict that such a basic building block undergoes a quantum phase transition that accommodates the existence of gate-controlled chiral edge states directly on Si. This will enable the design of integrated circuits hosting quantum spin hall (QSH) insulators, thus bringing topological functionalities a step closer to their deployment in consumer electronics.

2. Results and discussion

Our proposal relies on a heteroepitaxial stack grown on the so-called virtual substrate (VS), which accommodates the mismatch between the lattice parameters (being $a_{Sn}>a_{Ge}>a_{Si}$) and consists of a $Ge_{1-s}Sn_s$ layer deposited on a conventional Si wafer. The lattice constant of the top surface of the buffer is that of a relaxed $Ge_{1-s}Sn_s$ alloy, which can then be used as an epitaxial template for the repeated deposition of $Ge_{1-x}Sn_x/Ge_{1-y}Sn_y$ bilayers in a state of biaxial tension or compression, owning to the lattice mismatch with the selected VS. To disclose a rational design of QSH insulators on Si we begin by considering the band alignment established at a generic $Ge_{1-x}Sn_x/Ge_{1-y}Sn_y$ heterointerface. We assume the epitaxial films to be in full registry - or coherent - with the lattice constant of an underlying fully relaxed $Ge_{1-s}Sn_s$ buffer. To minimize the computational

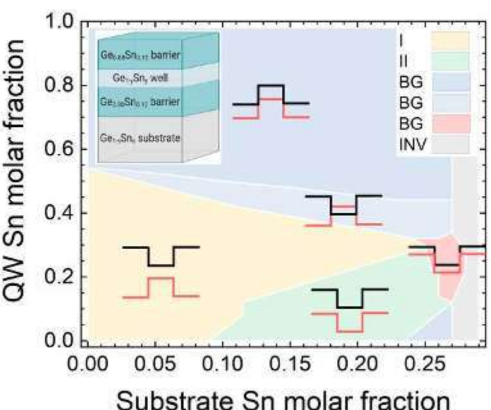

Fig. 1 Band-edge profiles of $Ge_{0.88}Sn_{0.12}$/ $Ge_{1-y}Sn_y/Ge_{0.88}Sn_{0.12}$ heterojunctions as a function of the Sn concentration of the relaxed substrate. The schematics of the band line-ups demonstrates a type I (yellow), type II (green), and broken gap (BG red, light and dark blue) alignments. The region where the band inversion occurs within the same layer is also shown (INV, grey).

burden and accelerate our investigation, we rely on the flexible approach offered by the well-established model-solid theory to compute band edges and interface line-ups by including strain effects [3].

Without loss of generality, we consider here a symmetric $Ge_{1-x}Sn_x/Ge_{1-y}Sn_y/Ge_{1-x}Sn_x$ heterostructure. The two external and identical $Ge_{1-x}Sn_x$ films will be dubbed barriers, whereas the intermediate $Ge_{1-y}Sn_y$ layer will be termed well. The band line-ups at the heterointerface have been obtained by varying the strain in the epitaxial stack through the modification of the Sn molar fraction of the $Ge_{1-s}Sn_s$ buffer.

Fig. 1 summarizes the results that were obtained for the specific case of $Ge_{0.88}Sn_{0.12}/Ge_{1-y}Sn_y/Ge_{0.88}Sn_{0.12}$ heterojunctions when opposite ends of the y range of the well are considered (more elaborate results can be found in Ref. [2]). Fig. 1 also reports a basic scheme of the offsets at the conduction band (black lines) and at the top of the valence band (red lines). It is interesting to notice the rich atlas of line-ups unleashed in the $Ge_{1-x}Sn_x$ system. Specifically, when

the Sn molar fraction of the substrate is high, a Sn bulk-like band structure can be systematically achieved within the films (INV, grey region in Fig. 1). However, when s<0.26, an inverted regime can be prominently observed also when the Sn content of the wells exceeds 50%. More specifically, a region exhibiting an inverted type-I feature opens below 60%, while a distinct BG develops well above 60%. In the low Sn content scenario (y<0.5), the strain imprinted by the substrate appears to restore the normal band sorting, featuring either a type-I (yellow area) or a staggered type-II (green area) alignment. In the latter case, charges are set apart at opposite sides of the heterointerface, where a well-defined insulating gap is retained. Surprisingly, however, in this diluted alloy regime there exists a region, albeit minute, in which our calculations predict the emergence of a unique BG. This occurs around 0.23<s<0.3 and 0<y<0.4 (marked in red in Fig. 1). Such a band has the advantage of having a direct gap in both the well and substrate and of being manifested in heterostructures that are easier to grow through epitaxial techniques.

As a proof-of-concept of the compelling emergence of a quantum phase on Si, we now focus on a model $Ge_{0.88}Sn_{0.12}/Ge_{0.78}Sn_{0.22}$ superlattice (SL) featuring a BG alignment. We utilize a nanoribbon geometry and solve numerically the full 8-band $k{\cdot}p$ Hamiltonian to address the emergence of gapless helical states [4]. Fig. 2 shows the edge energy spectrum where two linearly dispersing energy states (red) appear inside of the gapped bulk (black) and cross each other at the Γ point. A detailed analysis further showed a vanishing square amplitude in the bulk of the SL [2]. These findings eventually demonstrate the presence of Kramers's pair tightly localized at the opposite sides of the nanoribbon, thus providing strong evidence about the emergence of a QSH phase in group IV heterostructures.

3. Conclusions

We unveiled quantum phases of matter in silicon-compatible materials beyond conventional systems. The model-solid theory was applied to rapidly chart out the space of band line-ups in $Ge_{1-x}Sn_x$-based heterostructures. We were able to gather insights and identify, for the first time in group IV materials, a BG alignment suitable for a subband inversion and the final emergence of topologically protected edge states. Using $k{\cdot}p$ calculations we show $Ge_{1-x}Sn_x$ SLs that exhibit the QSH effect. Above all, the dipolar nature of these edge states at the heterointerface naturally permits the electric field control of the quantum phase [2]. Our concept of a $Ge_{1-x}Sn_x$-based QSH insulators is highly flexible and can have a longstanding impact, stimulating new research directions towards bandgap-engineered topology on Si. The future ability to integrate QSH phases onto ordinary Si wafers can be profoundly impactful by quickly and cost-effectively bring quantum technologies into present-day microchip architectures and ignite future progress towards large-scale Si-based topological computing and spintronics.

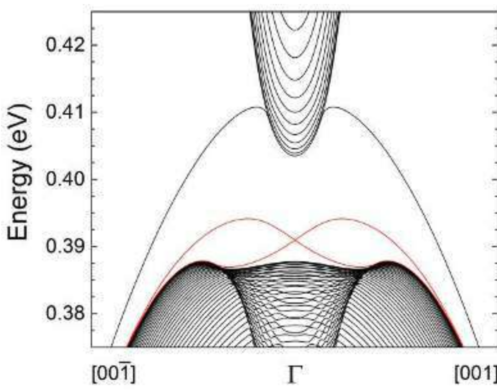

Fig. 2 Band structure calculated through $k{\cdot}p$ method in a 300 nm nanoribbon comprising a $Ge_{0.78}Sn_{0.22}$(25 nm)/$Ge_{0.88}Sn_{0.12}$(25 nm) infinite superlattice that is fully strained to a $Ge_{0.7}Sn_{0.3}$ substrate. The red lines highlight the topological edge states.

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Temperature dependence of Raman scattering in Ge and GeSn layers

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1. Introduction

Germanium (Ge) and GeSn epitaxial layers are excellent candidates for CMOS-compatible optoelectronics and photonics. The understanding of their optical and electrical transport property as well as full device simulations, including heat transport and carrier scattering mechanism, requires knowledge of their vibrational properties. Temperature dependence is especially relevant since the devices often operate at cryogenic temperature [1].

To this aim, Raman spectroscopy is a well-suited technique since it is a non-destructive method and can easily be used in combination with cryostats and be applied to spatial mapping. Its measurements of phonon energy provide detailed information about structural properties such as epitaxial strain and composition as well as anharmonicity of vibrations and heat transport in the material.

A full account of temperature dependence of the energy of Raman modes can therefore be very fruitful for fundamental investigations and to provide experimental parameters to be included in numerical studies. Additionally, it supports the calibration of methods to extract temperature-dependent properties such as strain in microdevices.

In this work, we use Raman spectroscopy to study epitaxial Ge and GeSn layers in the temperature range from 80 to 573 K and compare the result to a model comprising thermal expansion, multiphonon scattering and strain. Using X-ray diffraction (XRD) as a function of temperature, we obtain experimental values for the volume expansion and strain of the layer to be used in the analysis.

2. Methods

2.1. Sample preparation

Epitaxial layers were grown by Reduced Pressure Chemical Vapor Deposition (RPCVD). For Ge growth [2], we used Si substrates. GeSn was grown on Ge virtual substrates on Si [3].

2.2. Raman spectroscopy and XRD

For Raman spectroscopy, visible lasers (532 nm and 633 nm) were used for excitation. The scattered light was collected in backscattering geometry using a long working distance objective and dispersed using a grating with 1800 or 2400 line/mm grating. The main LO phonon of Ge and of Ge-Ge pairs in GeSn alloys was measured as a function of temperature using a liquid nitrogen cryostat.

The lattice parameters of the different samples were measured via high-resolution XRD reciprocal space mapping as a function of temperature using a liquid nitrogen cryostat. The (004) and (224) Bragg reflections were measured.

3. Model

The energy of the phonon mode measured by Raman spectroscopy derives its dependence on temperature through different mechanisms. In bulk, multiphonon anharmonic processes and thermal expansion must be considered. In epitaxial layers, an additional contribution of strain is present.

Phonon-phonon scattering is a manifestation of the anharmonicity of the interatomic potential. Its dependence on temperature arises from the occupation of phonon states according to the Bose-Einstein statistics and results in both shift and broadening of Raman peaks [4]. Multi-phonon scattering can be considered. Here, we limit to the 3-phonon case (one phonon decays into two). It is assumed that the coupling constant A is independent of temperature and is a free parameter in the model.

Thermal expansion affects the vibrational modes through the thermodynamic properties of the phonon gas [5]. This term is controlled by the coefficient of thermal expansion (CTE) α and the Grüneisen parameter γ. For an epitaxial layer, thermal expansion of both substrate and epilayer must be considered, resulting in an effective linear CTE α_{eff} that may differ from that of a bulk material. In this work, we have used temperature-dependent XRD to measure the

lattice parameters and the volume of the epitaxial layer unit cell, to obtain α_{eff}.

The thermal expansion affects also the amount of strain in the epitaxial layer. In turn, this shifts the vibrational mode in a different way with respect to the volumetric expansion described above. The temperature dependence of strain and that of the coupling constant *b* [6] should then be considered. Therefore, we used XRD data for the strain values. Additionally, since the temperature dependence of *b* is typically very weak, we take it as constant.

Using typical values for the free parameters, we found that the dominant contribution is the anharmonic scattering, while thermal expansion and strain dependence are less relevant. In Fig. 1, the results of the fit for a Ge sample is reported.

Furthermore, numerical analysis shows that the variation of Grüneisen parameter γ and the coefficient *b* have much smaller effect than the anharmonic coupling *A* on the quality of the fit. Thus, we can assume γ to be fixed to the value established for Ge. In this way, since we use the XRD data for thermal expansion and strain, and assume some of the parameter to be constant, the model is reduced to have only two free parameters, the coupling *A* and the energy of the mode in the low temperature limit ω_0.

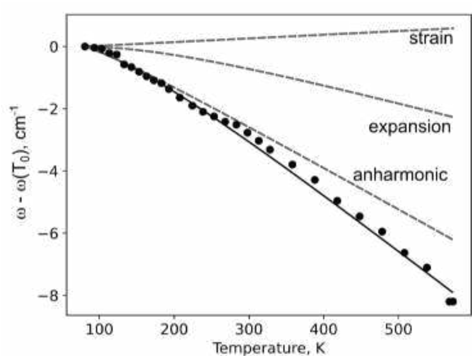

Fig. 1. Energy variation (data, symbols, and fit, solid line) with respect to 80 K vs temperature for the main peak of a Ge sample. The contribution of thermal expansion, anharmonic coupling and strain are also reported (dashed lines) relative to their value at 80 K.

4. Experimental results

We have compared our model to different samples of thin films of Ge and GeSn that were measured by XRD and Raman spectroscopy. The model as described above reproduce well the temperature dependence of the main peak (see an example in Fig.1). We selected Ge samples with different treading dislocation density (TDD), down to $7{\cdot}10^6$ cm^{-2} [2]. The anharmonic coupling, of the order of 1 cm^{-1}, increases by ~10% raising the TDD by a factor 50. A control sample of polycrystalline Ge has an anharmonic coupling ~15% larger with respect to the sample with lowest TDD.

In the thin, compressively strained GeSn alloy layers, with Sn concentration in the range of 5%-14%, the anharmonicity does not have clear correlation with the Sn content and is in the range 1-1.5 cm^{-1}. This result is comparable with the values of Ge.

5. Conclusions

In conclusion, we have applied a model for the temperature dependence of the Raman modes in epitaxial Ge and GeSn, using complementary XRD data. We find that the dominant mechanism is anharmonic scattering. The comparison of several samples indicates that scattering has comparable strength in Ge and GeSn with little dependence on defect density and alloy composition.

These insights can be beneficial in predicting phonon transport properties, which are important for heat management of optoelectronic devices and for efficient thermoelectric materials and devices.
Conversely, the calibration of the Raman spectroscopy as a function of temperature can be exploited, for example, in the measurement of strain in microstructures, where XRD can be not of straightforward application.

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Low-temperature Thermoelectric Properties of GeSn Alloys Films

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1. Introduction

One of the recent hot topics in the group-IV field is the realization of a direct transition semiconductor in $Ge_{1-x}Sn_x$ alloys with a sufficient Sn content, resulting in the demonstration of the optically pumped [1-3] and electrically injected lasers [4]. The ceaseless efforts by many researchers since the first demonstration of the material synthesizing is opening up the feasibility of on-chip and chip-to-chip optical communications using only group-IV alloys.

Apart from the photonic applications, the $Ge_{1-x}Sn_x$ is expected to be used in thermoelectric (TE) material. Theoretically, $Ge_{1-x}Sn_x$ alloys possess lower thermal conductivities κ than Ge, owing to the mass-difference scattering of phonons that occurred by the heavier element of Sn [5]. Experimentally, the κ reduction by introducing Sn was reported for the poly- [6,7] and single- [8,9] crystalline $Ge_{1-x}Sn_x$ layers. The low κ achieves a high TE performance and may help to ensure temperature differences within small TE devices integrated on Si chips, as in the Si nanowire TE generators [10]. However, a lack of data on the electrical conductivity σ and the Seebeck coefficient S was challenging to discuss $Ge_{1-x}Sn_x$ alloys' potential.

Recently, we reported relatively high power factors ($PF = S^2\sigma$) for $Ge_{1-x}Sn_x$ layers epitaxially grown on semi-insulating GaAs(001) substrates [9,11]; specifically, ~10 and ~30 $\mu Wcm^{-1}K^{-2}$ at room temperature (RT) for the p- and n-type layers, respectively. Note that the PF value for the n-type $Ge_{1-x}Sn_x$ layers is comparable with the counterparts of BiTe-based n-type layers (~25 $\mu Wcm^{-1}K^{-2}$ at RT [12]). This paper presents the low-temperature TE properties less than RT, which showed a significant S enhancement by phonon drag effects.

2. Experimental Procedure

A semi-insulating GaAs(001) wafer with a high resistivity exceeding 10^7 Ωcm was used for the growth of $Ge_{1-x}Sn_x$ layers to isolate electrically from the substrates. First, the substrates were cleaned in sequential deionized water, HCl solution, and deionized water. Next, the substrates were heat-treated at 500 °C in an ultra-high vacuum chamber with a base pressure of 10^{-7}–10^{-8} Pa. Before $Ge_{1-x}Sn_x$ deposition, the substrate was cooled down to 150 °C. A 150-nm-thick $Ge_{0.97}Sn_{0.03}$ layer with an antimony (Sb) dopant was grown on the substrates using a molecular beam epitaxy with Knudsen cells. X-ray diffraction analyses (XRD; Fig. 1) revealed that the in-plane reciprocal lattice of the $Ge_{1-x}Sn_x$ layer corresponds to that in the GaAs substrate, indicating a pseudomorphic growth. The crystallographic and TE characterizations samples were cut into a square shape of about 1×1 cm^2.

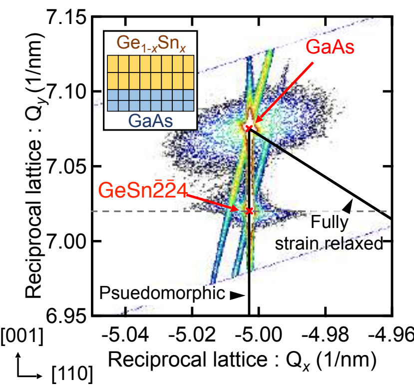

Fig. 1. XRD two-dimensional reciprocal space mapping of an Sb-doped $Ge_{1-x}Sn_x$ layer with the target Sn content of 3%. The Hall electron concentration was 4.0×10^{19} cm^{-3}.

3. Results and Discussion

We analyzed the surface morphology using atomic force microscopy (Fig. 2(a)). Figure 2(b) shows the Sb concentration dependence of the root-mean-square (RMS) roughness of the $Ge_{0.97}Sn_{0.03}$ layers. The RMS roughness gradually decreases with increasing the Sb concentration, although the microscopic domain structure with a small size of ~50 nm remains. The smooth surface is due to the surfactant effect of Sb during the growth, as is the case of MBE of $Ge_{1-x}Sn_x$ on Ge(001) substrates [13].

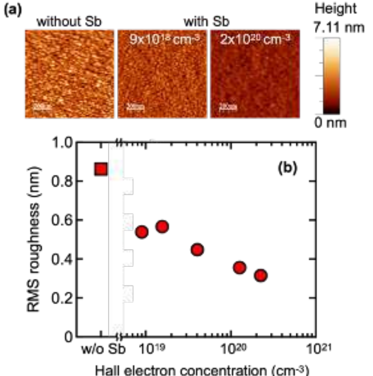

Fig. 2. (a) AFM images and (b) the RMS values of the $Ge_{1-x}Sn_x$ layers with different Sb concentrations.

The σ, S, and PF are summarized in Figs. 3(a)-3(c), respectively, as a function of measurement temperature T. The σ gradually increases with decreasing T from 300 to 30 K and then saturated. On the other hand, $|S|$ gradually decreases with decreasing the T from 300 to 100 K. As lowered the T more, the $|S|$ significantly begins to increase and then decrease. As a result, a maximum value of $|S|$ was observed at ~20 K for all samples. Specifically, 1.59 mVK^{-1} was obtained for the sample with the Sb concentration of 9×10^{18} cm^{-3}. The maximum $|S|$ values decreased with increasing the electron concentration, but the peak was observed even for a high Sb concentration of 2×10^{20} cm^{-3}.

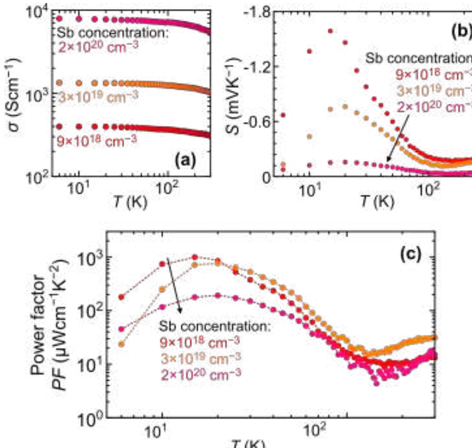

Fig. 3. The temperature dependence of (a) σ, (b) S, and (c) PF (= $S^2\sigma$) of the $Ge_{1-x}Sn_x$ layers with different Sb concentrations.

In the previous study on S in single-crystalline Ge bulks [14], the $|S|$ enhancement at a low temperature of less than 100 K was reported, and they claimed that this is due to a phonon-drag effect. Unfortunately, the phonon drag was absent in the heavily doped bulks required for σ enhancement, specifically above the electrical concentrations of 2.3×10^{18} cm^{-3}. In contrast, our $Ge_{0.97}Sn_{0.03}$ films showed a phonon-drag related $|S|$ peak around 20 K, even for a higher Sb concentration over an order of 10^{18} cm^{-3}. As a result, an excellent PF was obtained at a low T; specifically, ~10^3 $\mu Wcm^{-1}K^{-2}$ for the sample with the Sb concentration of 9×10^{18} cm^{-3} (Fig. 3(c)).

3. Conclusions

We have systematically investigated carrier transport properties in heavily Sb-doped $Ge_{1-x}Sn_x$ layers with different doping concentrations pseudomorphically grown on GaAs(001) substrates. From analyses of the Hall effect and Seebeck effect, we obtained an enhancement of the $|S|$ by the phonon-drag impact on the temperature range of less than 100 K without reducing the σ, resulting in a high PF (~10^3 $\mu Wcm^{-1}K^{-2}$ at 20 K). This finding is a good guide for achieving high-performance TE devices operated at low temperatures.

Acknowledgements

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Polarized-resolved Raman scattering of epitaxially grown GeSn layers with various Sn content

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1. Introduction

Due to its potential use in photonics, optoelectronics, microelectronics, and thermoelectrics, germanium-tin ($Ge_{1-x}Sn_x$) alloys are gaining interest, since they could be integrated into the complementary metal–oxide semiconductor (CMOS) technology. The band-gap structure of GeSn may be largely engineered into a direct band gap group IV semiconductor by selecting the appropriate strain and composition of the epitaxial layer [1-4].

Raman spectroscopy is a powerful tool for the characterization of this material and other semiconductors, as it permits rapid and accessible measurements of a number of important characteristics, such as the strain and composition of the layers and their crystalline properties. Raman spectroscopy provides a more general understanding of vibrational modes, including their energy, symmetry, and lifetime. The Raman spectra of semiconductor alloys exhibit strong first-order peaks associated with the vibrations (optical phonons) of each possible pair of component atoms [5-6].

Polarization-resolved Raman measurements reveal the symmetry of the vibrational modes. When coupled with numerical simulations of the vibrational modes under various disorder configurations, this method is particularly effective. DFT simulations provide insight into the movement of ions in a supercell of an alloy, hence directing the interpretation of experimental Raman spectra. We use the polarization-resolved Raman spectroscopy on GeSn layers to study the nature of individual modes. In this way, we obtain in-depth understanding on the role of alloy disorder in producing multiple spectral features.

2. Results and discussion

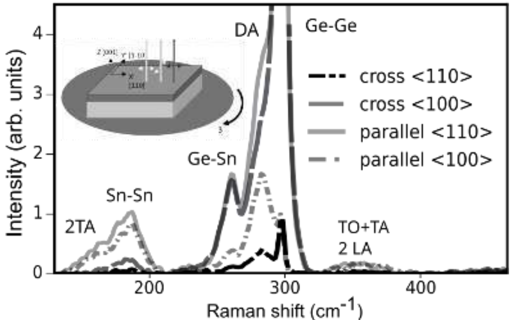
2.1. Experimental details

We have investigated $Ge_{1-x}Sn_x$ epitaxial layers with thickness in the range 90-770 nm, composition $0.045 \leq x \leq 0.14$ and compressive strain values from -0.13% to -1.51%. $Ge_{1-x}Sn_x$ alloys were epitaxially grown on 1-μm-thick Ge buffers on 200 mm Si(100) wafers in an industry chemical vapor deposition (CVD) reactor. To determine the characteristics of individual Raman modes and to separate the independent components based on the symmetry of the vibrational mode, we aligned the crystal axes to the setup polarization. The direction of incidence and scattering is [001] (z). Raman spectra were obtained in the four polarization configurations z(x'x')z, z(y'x')z, z(yy)z and z(xy)z in Porto notation, where x, x', y, y' correspond respectively to [100], [110], [010], [110] crystal directions.

As a reference, we employ the Raman active representations of the O_h point group to analyze the polarization angle dependence of the modes in GeSn. We examine the polarization dependence of the various spectral features and compare them with all the Raman-active representations of the O_h point group, namely T_{2g}, non-degenerate A_{1g}, and 2-fold degenerate E_g[7].

2.2. Polarization dependence

Figure 1 Raman spectra in four different configurations for



samples with 6at.% of Sn and strain of -0.32%. The inset shows the measurement setup.

The analysis of polarization dependence of spectra allowed us to separate unambiguously the different contributions to the Raman spectra, i.e. the main LO Ge-Ge, Ge-Sn, and Sn-Sn-like modes, as well as disorder-activated (DA) secondary multiphonons Ge-

Ge modes [4]. To better assess the symmetry of the different modes, we measured sample with 14at.% Sn content by rotating the wafer from β=0° to 90° in 5° clockwise steps for parallel and cross-polarization.

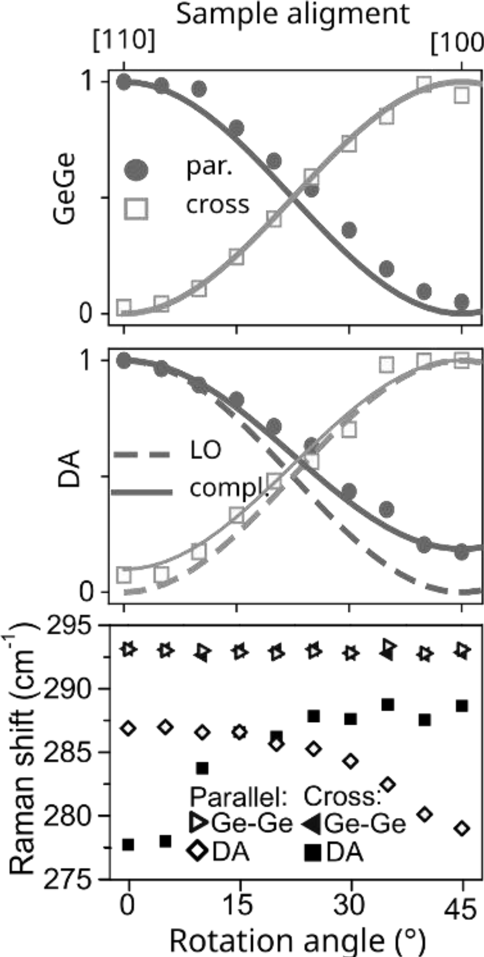


Figure 2 Angular dependence of peak intensity of Ge-Ge and DA peaks in the cross (full points) and parallel (empty points) polarization normalized to the maximum. The lines represent the fitting with an LO- only angular dependence (dashed) and complete (all symmetries, solid line). Angular dependence of the peak position of same peaks, in cross (full symbols) and parallel (empty symbols) polarization.

The angular-dependent intensity was fitted with a model composed of the sum of all active components T_{2g} (LO), A_{1g}, and E_g (represented by a solid line) and compared to the tendency of a pure T_{2g} (LO) mode (represented by a dashed line). After evaluating the evolution of the multiple components of the vibrational modes with Sn content, we concentrate on the spectral characteristics associated with the lattice disorder (disorder assisted, DA). The composite nature of the DA peak is revealed by analyzing its position as a function of the rotation angle. Figure 2 shows the angular dependence of the peak positions of Ge-Ge and DA in the cross (full symbols) and parallel (empty symbols) polarization. The Ge-Ge mode position is independent of the angle and the polarization configuration. Instead, the DA peak is characterized by a significant variation of about 10 cm^{-1}, with a clear correlation with the angular dependency of the peak intensity. This suggests that the DA peak is a convolution of multiple modes whose center of mass shifts with the angle because they have different symmetry. For better understanding of the nature of the DA peak, we use the two numerically simulated cases of GeSn. In the case of clustered Sn, a single main Ge-Ge peak (without shoulders) is present, corresponding to Ge-Ge pairs whose vibration is weakly affected by the Sn atoms. In the case of the short range ordered (SRO) alloy, we can observe a main peak and an evident shoulder on the low energy side; the shoulder corresponds to the clustered case. We associated the shoulder to the DA component with LO symmetry.

In addition, the so-called Sn-Sn peak is confirmed by simulations to result from an effective combination of Ge and Sn atomic motion.

3. Conclusions

Using polarized Raman spectroscopy and numerical simulations, we have provided a picture of the role of Sn incorporation on vibrational properties of $Ge_{1-x}Sn_x$ epitaxial layers. By comparing the results of polarization-dependent Raman and DFT simulations, we can determine the nature of the DA structure, which is a combination of a mode related to vibration of Ge atoms unaffected by Sn neighbors and one due to the activation of modes caused by the presence of disorder.

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Determining the Superiority of Cavity-Free Thermoelectric Generators Composed of GeSn and Si Wires

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1. Introduction

This work demonstrates the thermoelectric (TE) performance of cavity-free thermoelectric generators (TEGs) using GeSn and Si wires. In the Cavity-free structure, one side of the TEG is heated, and the back of the substrate is cooled. Thus, the heat energy flows mainly in the vertical direction but also exudes horizontally. This horizontal heat flow forms a steep temperature gradient in the wires, which is ranged from hundreds of nm.

The efficiency of a given material to produce a thermoelectric power is governed by its figure of merit (ZT), which is proportional to the Seebeck coefficient (S), electrical conductivity (σ), and absolute temperature (T) but inversely proportional to thermal conductivity (κ) [1]. The typical conversion efficiency of a TE material remains below 10%; therefore, research is ongoing to develop new TE materials for power generation by improving ZT [2,3]. Si and GeSn have drawn significant attention in recent years as prominent TE materials due to their low thermal conductivity and high power-factor [4].

In this work, with the identical patterning design, the TE performance of the cavity-free TEG using GeSn and Si wires was investigated. The obtained TE performance was conducted to compare GeSn wires with Si wires in the cavity-free planar structure, focusing on scalability.

2. Experimental

Two distinguished TEGs with the same pattern were fabricated by the GeSn and Si wires on the Gallium arsenide (GaAs) and silicon-on-insulator (SOI) substrates, respectively. The thicknesses of the Si substrate, the buried oxide (BOX) SiO_2 layer and the top SOI layers were 750 µm,145 nm, and 55 nm, respectively. The Antimony (Sb) doped GeSn (Sn: 2.5%) was grown on a semi-insulating 650 µm thickness of GaAs substrate by molecular beam epitaxy. The thickness of GeSn layer was 250 nm. The SOI and GeSn layers were turned into wires and pads by photolithography and reactive ion etching. The cross-sectional views of the fabricated TEGs are shown in Fig. 1.

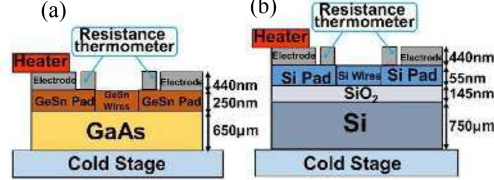

Fig. 1. Schematic views of TEGs. (a) GeSn (b) Si.

The active impurity concentration of Sb for GeSn is 5×10^{19} cm^{-3} and that of Phosphorus for Si is 1.1×10^{20} cm^{-3}. The wire lengths (L_{wire}) are varied as 3000, 1000, 500, 100, and 5 µm. Metal films (Ti: 10 nm, TiN: 30 nm, Al: 400 nm) were deposited by sputtering to form electrodes and resistance thermometers at both ends of the wires. The temperature differences between both ends of the wires (ΔT_{wire}) were measured by the resistance thermometers. The heater was attached to the hot side electrode of the TEG. The temperature of the stage was kept constant at 20°C, and the heater was set at 25 °C.

3. Results and Discussion

The effective Seebeck coefficient (S), which is defined as the open-circuit output voltage (V_{oc}) divided by the ΔT_{wire}, of the GeSn and Si-TEGs were evaluated as approximately -277 and -100 µV/K respectively, by using the resistance thermometers (Fig. 2). The low thermal conductivity of the GeSn-TEG increases ΔT_{wire} compared to the Si-TEG which produces high V_{oc} of the GeSn-TEG. Therefore, the S of the GeSn-TEG is higher than the Si-TEG.

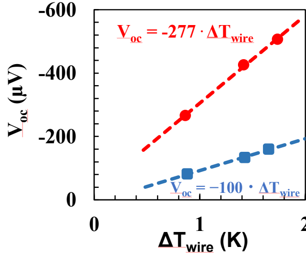

Fig. 2. Seebeck coefficient of 3000 µm device

The electrical resistances both in GeSn and Si-TEGs (R_{TEG}) increased with the increase of the L_{wire}. The electrical resistivity (ρ) of the GeSn and Si-TEGs were estimated as 2493 and 694 μΩ·cm. The power factor (S^2/ρ) of GeSn-TEG is 2.5 times larger than Si-TEG. Higher Seebeck coefficient leads to the higher power-factor of the GeSn-TEG than the Si-TEG.

The maximum power (P_{max}) was calculated as $V_{oc}^2/(4 \cdot R_{TEG})$. The P_{max} was increased by increasing the L_{wire} (Fig. 3a). The maximum TE power of the GeSn-TEG shows higher values than the Si-TEG. Since the V_{oc} of the GeSn-TEG is much higher than the Si-TEG and the resistances of the GeSn-TEG are lower than the Si-TEG. Therefore, the GeSn-TEG shows greater TE power than the Si-TEG. The same phenomenon has happened in our other work also [5].

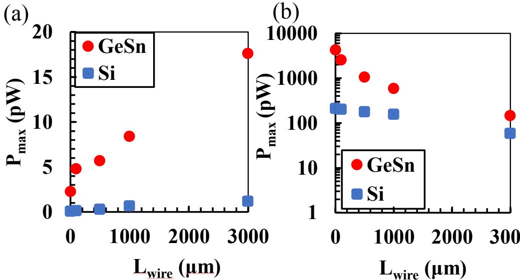

Fig. 3. TE power (a) experiment, (b) simulation

To evaluate the experimental result, the TE performance of the fabricated devices was numerically analyzed by COMSOL Multiphysics. The simulated TE power shows the opposite trend to the experiment, where TE power increases with the shortening of the wire as shown in Fig. 3b.

The contact thermal resistance between the stage and the device may be a factor for this discrepancy in the experiment. However, to ensure this, the simulated model was modified by adding a high thermal resistance layer beneath the substrate, as shown in Fig. 4a. The modified model's TE power (Fig. 4b) agrees with the experimental TE power, which suggests that the performance could be further improved by suppressing contact thermal resistance between the stage and substrate in the experiment, which was not conducted in our previous work.

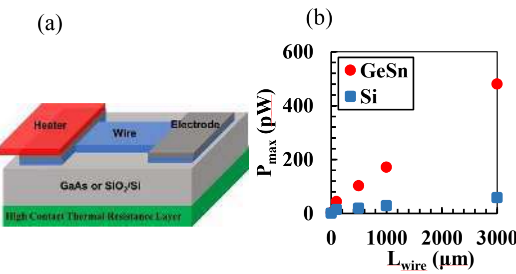

Fig. 4. (a) Modified model, (b) new simulated TE power

To obtain a large power from a large-scale integrated TEG, realizing high power density is important. The TE power density was calculated by dividing the P_{max} by the total footprint of the GeSn and Si wire bundle, excluding the pad areas. The TEG with shorter wires demonstrated a greater power density (Fig. 5) both in GeSn and Si-TEGs, which is similar to our previous study [1].

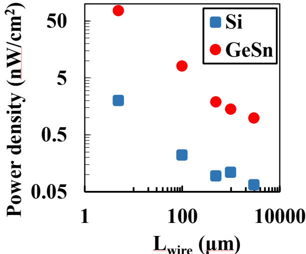

Fig. 5. Power density dependences on the lengths

The maximum TE power density of the GeSn-TEG is approximately 28 times larger than the Si-TEG for the length of 5 μm. Considering that the thickness of GeSn wire is 4.5 times thicker than the Si wire, we can conclude that the TE power of GeSn-TEG is intrinsically higher than that of the Si-TEG by about 6 times.

4. Conclusion

We demonstrated GeSn and Si-TEGs in the cavity-free structure. The Seebeck coefficient and TE power of GeSn-TEG show higher values than Si-TEG due to the high power-factor of GeSn-TEG. The maximum power density of GeSn-TEG is approximately 6 times higher than Si-TEG in considering wire thickness difference, indicating the superiority of the GeSn-TEG over the Si-TEG. The experimental TE performance could be further improved by suppressing contact thermal resistance between the stage and substrate.

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Record-High Electron Mobility in Polycrystalline GeSn Thin Films on Insulators

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Abstract

The low-temperature solid-phase crystallization was applied to n-type impurity doped amorphous GeSn thin films on insulators. Optimizing the amounts of P and Sn in Ge and preparing an Al_2O_3 underlayer, the resulting GeSn layer exhibited an electron mobility 450 $cm^2\ V^{-1}s^{-1}$ despite the low-temperature process (375 °C). This is the world's highest value among n-type polycrystalline Ge based layers directly formed on insulators below the melting point of Ge (937 °C).

1. Introduction

Ge is again expected as a channel material for next-generation thin-film transistors. We have successfully fabricated p-type polycrystalline Ge layers with high hole mobility (690 $cm^2\ V^{-1}\ s^{-1}$) at low temperatures (< 500 °C) using an advanced solid-phase growth method [1,2]. In addition, we fabricatd n-type polycrystalline Ge layers by doping n-type impurities (P, As, and Sb) [3]. Here, we investigate the effects of Sn addition and interfacial layer insertion on P-doped Ge to improve the electron mobility μ_n, which has been effective for p-type Ge [2,4]. As a result, the highest μ_n among low-temperature n-type polycrystalline Ge layers is demonstrated.

2. Experimental Procedures

P-, As-, or Sb-doped amorphous Ge(Sn) layers were deposited on SiO_2 glass substrates using the Knudsen cell of a molecular beam deposition system. The samples were then loaded into a conventional tube furnace under a N_2 (99.9%) atmosphere and annealed at a growth temperature (T_g) of 375 °C for 150 h or 400 °C for 10 h to induce crystallization. The dopant concentrations in Ge were determined by secondary ion mass spectrometry (SIMS), which were constant regardless of before and after annealing. To control the interfacial nucleation, Al_2O_3 or GeO_2 (10 nm thickness each) underlayers (ULs) were sputtered on the substrate before Ge deposition. The samples were analyzed using optical microscope, electron backscattering diffraction (EBSD), transmission electron microscopy (TEM), and Hall effect measurement (van der Pauw method).

3. Results and Discussion

According to the EBSD analyses, Ge grain size after growth strongly depended on the dopant type and concentration, reaching a maximum with P addition in the 10^{20} cm^{-3} range (Fig. 1(a)). The electron density n peaked with the dopant concentration (Fig. 1(b)), while the dopant activation rate decreased with increasing dopant concentration (Fig. 1(c)). The trend of the activation rate is consistent with the solid solution limit of various dopants [4]. μ_n generally reflects the grain size, reaching 390 $cm^2\ V^{-1}\ s^{-1}$ for the P-doped sample (Fig. 1(d)).

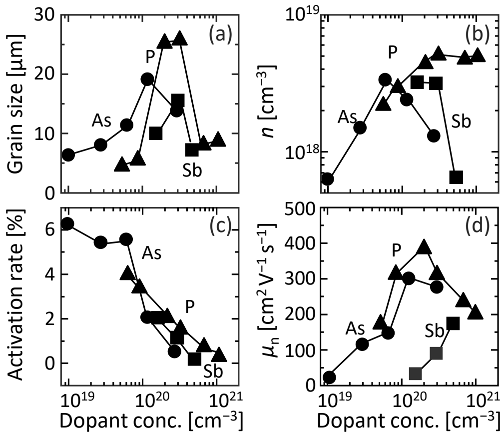

Fig. 1. Characteristics of the P-, As-, and Sb-doped Ge samples. (a) Average grain size determined by the EBSD analyses, (b) n, (c) activation rate, and (d) μ_n as a function of the dopant concentration.

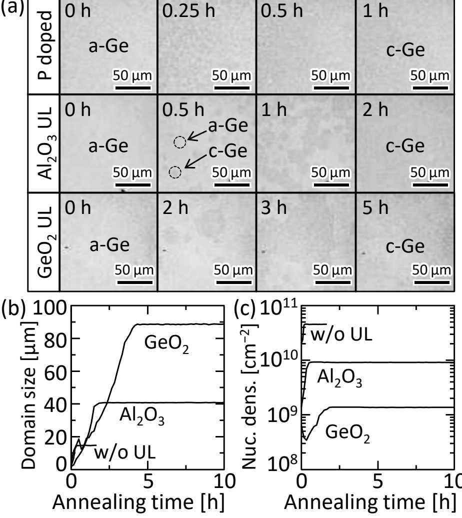

Fig. 2. Characteristics of the crystallization rate of undoped and P-doped Ge (w/ and w/o UL), where T_g = 400 °C. (a) In situ optical microscopy observation. Annealing time dependence of the (b) domain size and (c) nucleus density.

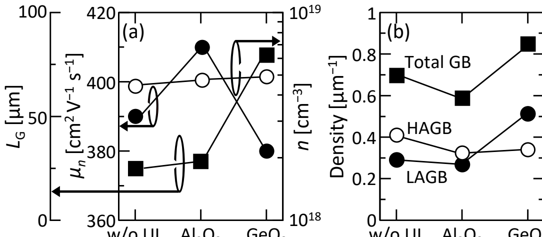

Fig. 3. Characterization of the P-doped Ge samples with Al_2O_3 and GeO_2 ULs. (a) Grain size L_G, μ_n, and n. (b) Grain boundary density.

Hereafter, we focused on P as n-type dopant, which showed the best properties. We investigated the effects of the Al_2O_3 and GeO_2 ULs for P-doped Ge. Figure 2(a) shows typical optical microscope images, indicating the crystallization process of the amorphous Ge layer. With an increase in the annealing time, the Ge crystals nucleated, grew laterally, and covered the entire substrate. The domain size and the nucleus density were subsequently analyzed using machine learning with our algorithm (Fig. 2(b), (c)) [6]. With the insertion of the ULs, the domain size increased while the nucleus density decreased. The difference in the growth behavior due to the insertion of UL can be attributed to the change in the interfacial energy. Grain size and electrical properties were then investigated. n was constant regardless of UL type (Fig. 3(a)). μ_n was the largest for Al_2O_3 while the smallest for GeO_2, which did not match the grain size behavior. EBSD analysis of the density of low-angle grain boundaries (LAGB) and high-angle grain boundaries (HAGB) indicated that the GeO_2 sample had many LAGB within the grains as the grain size increased (Fig. 3(b)), which was suggested to be the cause of the mobility decrease.

For p-type Ge, hole mobility enhancement by Sn addition is well known [5,7,8]. Therefore, we added small amount of Sn (< 1%) in the P-doped Ge on Al_2O_3 UL. Cross-sectional TEM evaluation of the GeSn thin film with Al_2O_3 shows that there are no stacking faults or dislocations (Fig. 4(a)). Cross-sectional EDX evaluation shows that neither P, and Sn segregation nor Al_2O_3 diffusion occurs in Ge (Fig. 4(b)). The lattice image focusing on the interface between Ge and Al_2O_3 shows that high crystallinity is maintained near the interface (Fig. 4(c)). The selected area electron diffraction (SAED) pattern (Fig. 4(d)) indicates that the GeSn layer is single crystalline in this area. This sample exhibited μ_n of 450 cm^2 V^{-1} s^{-1}, which is the highest among the n-type polycrystalline Ge-based thin films (Fig. 5) [9–11]. It is also attractive because it surpasses that of a single-crystal Si wafer [12], whereas the process temperature of GeSn is 375 °C.

4. Conclusions

We investigated the solid-phase crystallization of impurity-doped amorphous Ge layers on insulators. The type and concentration of impurity significantly influenced the crystal quality and electrical properties in the resulting n-type Ge. The P-doped Ge was superior to the As- and Sb-doped Ge.

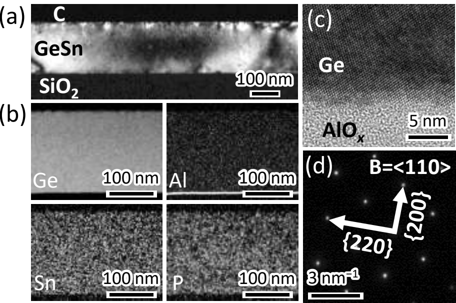

Fig. 4. Characterization of the cross-section of the GeSn on Al_2O_3 UL. (a) Dark-field TEM image. (b) EDX mapping of Ge, Al, Sn, and P. (c) High-resolution lattice images showing the Ge/Al_2O_3 interface. (d) SAED pattern obtained from region including GeSn layers with selected area of diameter 200 nm.

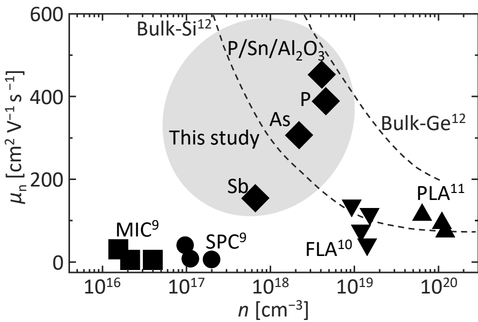

Fig. 5. Comparison of μ_n and n of polycrystalline Ge(Sn) on insulators. The data for bulk Si and Ge is shown by the dotted lines.

By adding Sn and employing Al_2O_3 UL to P-doped Ge, the μ_n of 450 cm^2 V^{-1} s^{-1} was achieved at a process temperature of 375 °C. This is the highest value among that of n-type polycrystalline Ge-based layers directly grown on insulators at low temperatures. The low-temperature synthesis of high-mobility Ge on insulators will provide a pathway for the monolithic integration of high-performance Ge- CMOS onto Si-LSIs and flat-panel displays. In the presentation, we will also report the results of development on flexible plastic substrates.

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GeSn Mid-Infrared Thermophotovoltaic Cells for Power Beaming and Heat Conversion

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1. Introduction

Narrow bandgap thermo-photovoltaic (TPV) cells have been the subject of extensive investigations motivated by their strategic importance in harvesting infrared radiations for heat waste conversion, portable devices, power beaming, and space applications [1], [2]. Recently, tremendous efforts have been expended to develop mid-infrared TPV cells to leverage their several technological advantages such as the potential to exploit the atmospheric transparency windows for eye-safer energy beaming and the ability to generate energy from the staggering amount of heat wasted by major industries. In fact, vital manufacturing sectors such as iron, steel, cement, glass, and metallurgy suffer large energy footprints exacerbated by heat losses at temperatures below $2000\,\mathrm{K}$. An efficient absorption and conversion of black-body radiations emitted in this range requires semiconductors with a bandgap energy (E_g) smaller than $\sim 0.7\,\mathrm{eV}$.
Compound semiconductors have been explored to implement both far-field and near-field sub-$2000\,\mathrm{K}$ TPV cells reporting a measured efficiency in the 1-11% range, while theory hints to higher values reaching 24% [2]–[4]. Notwithstanding the progress achieved so far in developing narrow bandgap TPV cells, the substrates needed to grow these cells are costly and suffer large dark currents. To mitigate the latter, narrow bandgap interband cascade photovoltaic cells (ICPV) based on InAs/GaSb multiple quantum wells have been recently proposed [5], [6]. These devices alleviate the limiting factors of bulk narrow bandgap TPV (high saturation dark current density, relatively low absorption coefficient, short diffusion length, material quality, etc.) thanks to the type II broken-gap alignment at the InAs/GaSb interface, which mainly enables carrier collection through tunneling. Under standard black-body radiation illumination [5], [6], the ICPV devices operating at $80\,\mathrm{K}$ exhibit relatively high V_{OC} ($\sim 1.1\,\mathrm{V} > E_g/e$) demonstrating that the multiple stage absorbers operate in series. However, at 300 K the ICPV devices perform poorly with V_{OC} around $5.7\,\mathrm{mV}$ and an output power density below $0.002\,\mathrm{mW/cm^2}$. The deterioration is attributed to the saturation current density being significantly higher than the photo-current density generated by the radiation from the black-body source.
A cost-effective and scalable alternative to compound semiconductor mid-infrared TPV materials would be the silicon-compatible narrow bandgap $\mathrm{Ge}_{1-y}\mathrm{Sn}_y$ semiconductors [7]. These group IV alloys are grown on large-diameter silicon wafers and can cover the entire mid-infrared range by increasing the Sn content. Indeed, the recent progress in their epitaxial growth led to the demonstration of a variety of monolithic mid-infrared emitters and detectors . Building on these achievements, herein we introduce $\mathrm{Ge}_{1-y}\mathrm{Sn}_y$ alloys to design silicon-integrated mid-infrared TPV cells and discuss their performance and its evolution as a function of the basic material properties.

2. Device structure and theoretical Framework

The proposed all-group IV mid-infrared TPV cells consist of a fully relaxed $\mathrm{Ge}_{1-y}\mathrm{Sn}_y$ p-i-n homojunction grown on a silicon wafer using a germanium interlayer - commonly known as virtual substrate. Fig. 1 exhibits a schematic illustration of the device structure. Note that the front electrode shadowing and the parasitic resistances are neglected in evaluating the device performance. Moreover, the one-dimensional treatment is justified since the device dimensions are significantly larger than the device thickness. Thus, the performance and the electrical properties of the TPV cell are estimated by solving self-consistently the steady-state coupled Poisson drift-diffusion equations. In the simulations of the optical behavior and related calculations of the generation rate $G(x)$ and the absorbance $\mathcal{A}(\lambda)$, the complete stack of layers is considered to describe both the front-side and back-side illumination. In our work, the optical transfer matrix method (OTMM) is employed to simulate light propagation through the different layers of the $\mathrm{Ge}_{1-y}\mathrm{Sn}_y$ TPV cells. To account for the incoherency of light in the structure (induced by the $500\,\mathrm{\mu m}$ thick Si substrate), $\mathcal{A}(\lambda)$ was computed using the generalized transfer matrix method (GTMM) [8]. Once the optical simulations are done and both $G(x)$ and $\mathcal{A}(\lambda)$ are obtained, as a first approximation,

the simulations are restricted to the set of active layers, namely the p-i-n junction (Fig. 1).

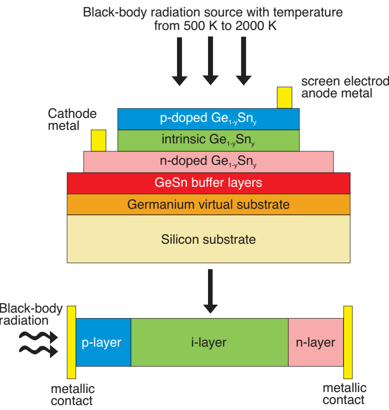

Figure 1. (a) Schematic illustration of the $Ge_{1-y}Sn_y$ TPV cell. (c) Impact of the source temperature T_{bb} upon the power conversion efficiency of the $Ge_{0.83}Sn_{0.17}$ p-i-n TPV.

In Si solar cells, the impact of the intrinsic recombination mechanisms (Auger and radiative recombination) on the conversion efficiency was shown to be negligible [9]. However for narow-bandgap $Ge_{1-y}Sn_y$ materials, depending on the material quality, these processes could be the most dominant. For that reason, the established formalism takes into account Auger, Shockley-Read-Hall (SRH), and radiative recombination mechanisms. The net non-radiative recombination rates are computed following the process described in [10]. As for the radiative recombination, rather than using a constant bimolecular recombination coefficient B, mostly accurate for non-degenerately doped semiconductor in weak-injection conditions, to estimate the net rate, the parabolic band approximation (PBA) combined with the Fermi's golden rule are used to derive a new expression of $B(n, p)$.

3. Results and discussion

The simulations are focused on $Ge_{0.83}Sn_{0.17}$ heterostructures corresponding to a bandgap energy of 0.291 eV. The $Ge_{0.83}Sn_{0.17}$-based TPV cells, operating at 300 K, are illuminated by standard black-body radiation sources whose temperature T_{bb} is within the 500 K to 1500 K range. In this range, the incident power density P_{in} varies from 0.16 to $27\,\text{W/cm}^2$, spanning both the low and high injection regimes. Assuming ideal ohmic contacts, the evolution of the TPV electrical parameters with the radiation temperature is studied, for both front-side and back-side illuminations. To account for the non-ideal experimental parameters (the geometrical view factor, the emissivity of the emitter etc.), the theoretical P_{in} can be scaled down to a specific value of interest. This approach is particularly useful for comparing our GeSn-based TPV to narow-bandgap III-V based TPV

TABLE 1. Performance parameters of current narrow bandgap TPV cells.

Parameters	GaInAsSbP p-n-n	InAs p-i-n	InAs p-i-n	GeSn p-i-n	GeSn p-i-n	GeSn p-i-n
E_g(eV)	0.35	0.35	0.35	0.291	0.291	0.291
T_{bb}(K)	1200	$\sim$ 1000	$\sim$ 1200	1200	1500	1500
P_{in}(W/cm^2)	0.5	0.72	0.32	0.3	0.7	26.96
J_{SC}(A/cm^2)	0.29	0.89	0.21	0.203	0.485	18.68
V_{OC}(V)	0.028	0.06	0.018	0.075	0.097	0.195
FF(%)	33	37	28.09	42.82	47.81	62.47
η(%)	0.53	3	0.33	2.16	3.22	8.45
P_{out}(mW/cm^2)	2.66	21.6	1.05	6.48	22.54	2.28×10^3
Ref	[11]	[12]	[3]	This work	This work	This work

cells for which the incident power densities are in the mW/cm^2 range for $T_{bb} \sim 1000 - 1500\,\text{K}$, as presented in table 1. These results show that TPV cells based on GeSn with relatively good material quality could performed better compared to III-V based cells.

4. Conclusion

In this work, we investigated the performance of TPV cells based on narrow bandgap GeSn materials. From these analyses, power conversion efficiency up to 9% was obtained for devices under black-body radiation of temperature within the 500 K to 1500 K range. With these results, silicon-integrated mid-infrared TPV cells are presented as cost-effective and scalable alternative to compound semiconductor mid-infrared TPV materials for harvesting the infrared radiation emitted through the heat wasted by major industries.

Acknowledgment

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Piezo Resistivity of Epitaxial SiGe

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1. Introduction

Recently, strain sensors are highly demanded in social and industrial fields such as health care sensing via heartbeat, pulse, and breathing, industrial robots to handle soft materials and to recognize the state of grabbed objects with precise and high-resolution [1,2]. Small dimension devices are a powerful candidate for these applications because of their small occupying area for high density array, and relatively large physical change for high sensitivity. However, by downsizing, fluctuations of the device properties, due to variation of polycrystalline grain size, become more pronounced, which prevents the sensing reliability of the devices. This fluctuation could be improved by switching from polycrystalline to single crystal material. In last three decades, Si has been an effective material for highly sensitive strain sensors. In this study, we evaluate piezo resistivity of epitaxial SiGe to assess the potential and feasibility for strain sensor applications.

2. Experimental

The piezo resistivity of epitaxial SiGe on a Si (001) substrate is investigated based on gauge factor (GF). 50 and 100 nm-thick, B and P-doped pseudomorphic SiGe is deposited by reduced pressure CVD on n- and p-type Si, respectively. The compositions of Ge are 10, 20 and 30% and B and P concentration are targeted to $\sim 1\times10^{19}$ cm^{-3}. The deposited SiGe is patterned by photolithography and dry etching to form a 16 µm wide and 300 µm long line as schematically shown in Fig. 1 (a). Afterwards the SiGe is passivated by 200 nm thick SiO_2 and windows for metal contact pads are opened. On the contact pads, 50 nm thick p+ and n+ differential epitaxial Si are deposited by using CVD on the B and P-doped SiGe, respectively, and polycrystalline part on SiO_2 is removed by dry etching. Then Ni sputtering followed by annealing is performed to form Ni silicide. On the Ni silicide, Al is deposited by sputtering. Finally, the contact pads are structured by photolithography. A schematic cross section of the Al contact pad is shown in Fig.1 (b). Then, the substrate is thinned down to 200 µm and diced to 2 cm × 2 cm.

In order to measure the piezo resistivity, the resistance is measured using four-terminal measurement with bending the sample by four-point bending method as shown in Fig. 2 [3]. The GF is estimated by slope of relative resistivity as function of induced strain.

3. Results and Discussion

In Fig. 3 (a, b), the relative resistance of B and P-doped SiGe as function of the induced strain is summarized. In the case of B-doped SiGe, the resistance of the SiGe decreases linearly with increasing induced strain for SiGe composition. The slope of the induced strain is slightly higher with increased Ge concentration. By introducing the compressive strain in SiGe, the enhancement of hole mobility is reported [4]. One of the possible reasons of the resistance reduction could be due to the hole mobility enhancement. On the other hand, in the case of P-doped SiGe, no clear dependency of the resistance by the induced strain is observed. In the case of n-type SiGe influence of the compressive strain on electron mobility is low [4].

GFs of B and P-doped SiGe as function of Ge content is summarized in Fig. 4 (a, b). With increasing the Ge concentration from 10% to 30%, the GF of B-doped SiGe is decreased from ~ -70 to -85, indicating improved strain sensitivity. It seems the effect/influence of thickness on GF is weaker when Ge content increases However, further investigation is required due to high error bar of the GF measurement. In the case of P-doped SiGe, almost no influence of Ge concentration on GF is observed. These results might be related to enhancement of hole mobility in SiGe and lower sensitivtiy of electron mobility by induced compressive strain in SiGe [4].

4. Conclusion

The piezo resistivity of epitaxial B and P-doped SiGe is investigated to assess the potential of thin-film epitaxial SiGe strain sensors. The piezo resistivity of B-doped SiGe is detected and increased strain sensitivity is observed for the SiGe with higher Ge content.

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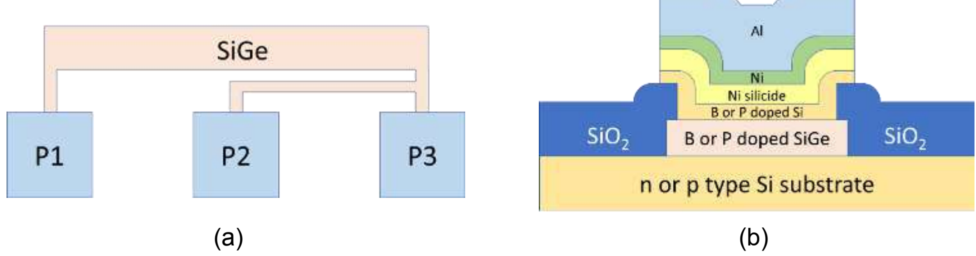

Fig. 1. (a) Schematic top-view diagram of piezo resistivity measurement structure and (b) cross sectional diagram of Al contact pads area. The SiGe structure is covered by CVD SiO_2. Al with Ni silicide is used for contact pads at P1, P2 and P3. Length and width of SiGe layer is 300 µm and 16 µm, respectively.

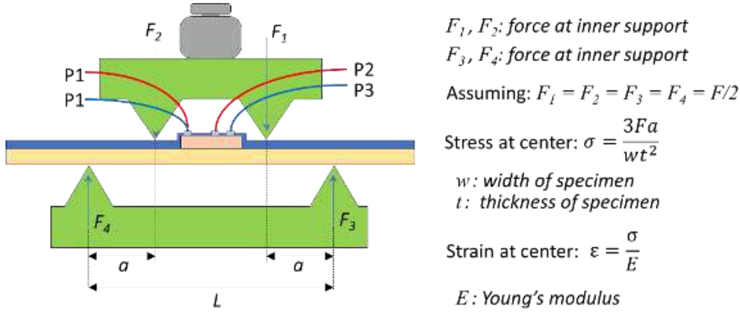

Fig. 2. Schematic diagram of tool to apply compressive strain into SiGe layer on Si substrate for piezo resistivity measurement. Current is supplied between P1 and P2 (also shown in Fig. 1(a)) and voltage between P1 and P3 is measured for resistance measurement.

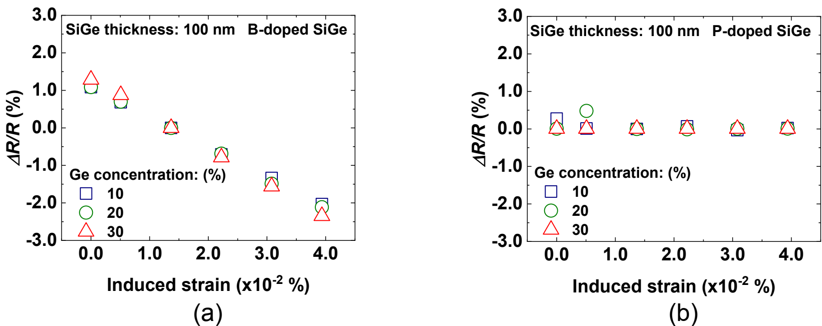

Fig. 3. Relative resistance of (a) B-doped SiGe and (b) P-doped SiGe with 10 - 30 % Ge content. B and P concentrations are targeted to ~1×10^{19} cm^{-3}. SiGe thickness is 100 nm. SiGe are psudomorphically grown on Si.

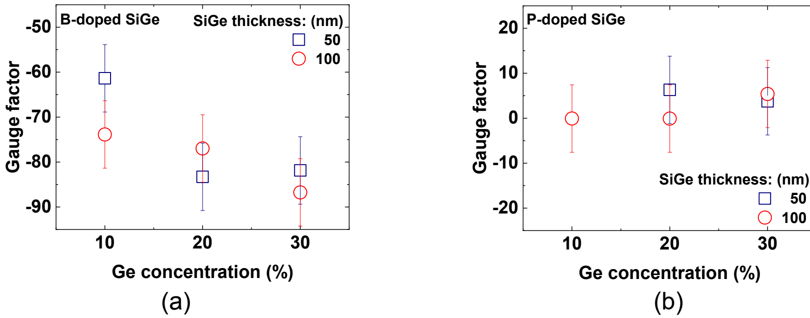

Fig. 4. GFs of (a) B-doped and (b) P-doped SiGe with 10 - 30 % Ge content. B and P concentrations are targeted to ~1×10^{19} cm^{-3}. SiGe thicknesses are 50 and100 nm. SiGe are psudomorphically grown on Si.

Silicon Germanium integrated modulator and photodetector in the mid-IR wavelength range.

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1. Introduction

Optical spectroscopy in the mid-infrared (mid-IR) range is an unambiguous way to detect environmental and toxic analytes. Therefore, mid-IR photonics has a great importance for many applications in sensing, imaging or even telecommunication. A challenging task is to make mid-IR spectroscopy accessible in remote areas, driving the development of compact and cost-effective solutions. The development of mid-IR photonics circuits has thus witnessed a burst of research activity in the recent years. Among the different materials investigated to develop mid-IR photonic circuits, germanium (Ge) based circuits benefit from both the compatibility with large scale and high-performance fabrication tools and a wide transparency window, extending up to 15 µm wavelength. Ge-on-silicon (Si) or graded silicon-germanium (SiGe) waveguides have already been successfully developed within the mid-IR spectrum. However new challenges arise to develop efficient on-chip electro-optical devices such as high speed electro-optical modulators and photodetectors, that could open a wide range of applications, from on-chip synchronous detection to frequency comb generation and detection.

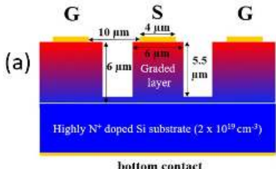
In this work, we report integrated electro-optical device that operate in a wide spectral range in the mid-IR, from 5 to 9 µm wavelength. They both rely on Ge-rich graded index SiGe photonics circuits that allow low loss propagation in a wide spectral range in the mid-IR [1]. First, a Schottly diode is embedded in the waveguide, in order to be able to tune the carrier concentration in the waveguide, and to achieve absorption modulation by free carrier concentration variation. Electro-optical modulation up to 1 GHz radio-frequency has been reported [2]. Interestingly it has been shown that this device can also be used for photodetection at room temperature [3]. Defect mediated sub-bandgap level is expected to be the mechanism at the origin of the photocurrent. Responsivity reaching up to 0.1 mA/W has been obtained at 5 µm wavelength.

2. High speed electro-optical modulator

The schematic view of the cross-section of the integrated modulator is depicted in Fig. 1.

It is based on a 6-µm-thick graded SiGe layer grown on a highly n-doped (Si) substrate with doping concentration of 2 x 10^{19} cm^{-3}. The graded SiGe layer is grown by linearly increasing the concentration of germanium (Ge) from 0 to 100 %, inducing a linear increase of the refractive index in the waveguide. The graded epitaxial layer has a residual n-doped concentration estimated to be in the order of 10^{15}-10^{16} cm^{-3}. At the top of the waveguide, a grounded coplanar waveguide electrodes based on a 300-nm-thick gold layer is deposited. The top contact on the lightly n-doped Ge layer presents a Schottky behaviour, while the bottom contact on highly n-doped Si is ohmic.

(a)



(b)

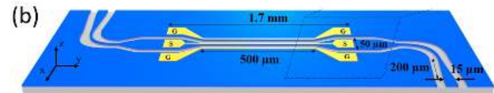


Fig. 1. : (a) Schematic cross-section view of the active region of the SiGe mid-IR integrated EOM, (b) Schematic view of the waveguide integrated modulator

When applying a negative voltage on the Signal electrical pad, the depth of the depleted region below the Schottky contact increases. The overlap between the optical mode and the free carriers region responsible for free carrier absorption decreases and so the absorption coefficient of the guided mode decreases, which corresponds to a modulation of the optical transmission of the guided mode.

The schematic view of the waveguide-integrated device is reported in Fig. 1.b. The core of the integrated modulator is 500 µm long, while the total distance between the GSG pads is 1.7 mm. The modulation efficiency has been characterized first in DC operation. The relative optical transmission (normalized with the optical transmission at zero bias)

is reported in Fig. 2(a) as a function of the reverse bias voltage and for wavelengths from 5.5 to 9 µm. As expected, the optical transmission increases when the amplitude of the reverse voltage increases. It can be noticed that the modulation efficiency increases for higher wavelengths, which is in good agreement with the FCPD effect. An extinction ratio higher than 1dB is obtained at the wavelength of 9 µm with -8V applied to the device.

High-speed characterizations have also been performed. An RF electrical signal is added to the reverse DC bias using a bias tee. The electrical signal is applied to the modulator by the external probes. The light coming out of the device is sent to a fast mid-IR detector and an electrical spectrum analyzer is used to acquire the corresponding beat notes. The peak amplitudes are recorded to characterize the evolution of the modulated optical power as a function of the applied RF frequency as reported in Fig 2b. The measured signal coming from the EOM is also compared with the noise level measured in the same configuration, by turning off the input laser. As measurements between 500 MHz and 700 MHz are limited by the high noise level of the detector at this frequency range. Nevertheless, a slow decrease of the modulated optical signal is observed as a function of the RF frequency. The time constant of the photodetector itself (specified to be below 25 ns) is expected to explain, at least partially, this evolution. Interestingly, optical modulation is measured up to 1 GHz where a signal to noise ratio larger than 10 dB is still obtained.

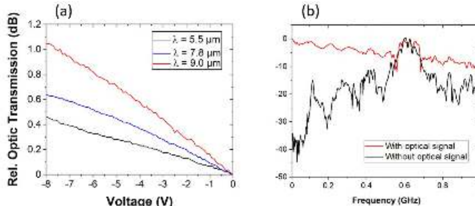


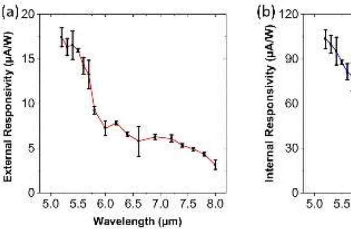
Fig. 2. (a) DC characterization of the EOM, (b) RF characterization of the EOM

2. Room-temperature integrated photodetector

Interestingly, the extensive characterization of the device allows to demonstrate that it can also be useful as an integrated photodetector operating at room temperature. Indeed, a clear photocurrent has been seen above the dark current level, when mid-IR laser is coupled in the photonics circuits, which was not expected as the photon energy is well below the bandgap energy of the SiGe alloy. A linear relation between the photocourant and the coupled power is obtained which excludes any non-linear effect such as two/three/four photon absorption. The photodetector sensitivity has been quantified by estimating the external (resp. internal) responsivity, by the ratio between the measured photocourant and the optical input power measured using a power meter at the output of the QCL source (resp. considering the fraction of the light coupled in the photonic circuit).

Both the external and internal responsivities are reported in Fig. 3. Interestingly, a clear photoresponse is obtained from 5 to 8 µm at the bias voltage of -8V. When considering the light effectively coupled in the photodector, an internal responsivity up to 0.1 mA/W is obtained at 5.2 µm.

Defect-mediated sub-bandgap absorption due to dislocations within the graded region is supposed to the mechanism at the origin of the photocurrent, but further studies are required to optimize this effect.



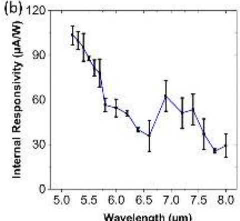


Fig 3: External (a) and internal (b) responsivity of the photodetector as a function of the mid-IR wavelength with -8 V applied to the device.

3. Conclusion

In this work integrated optoelectronic devices operating in a wide spectral range in the mid-IR have been reported. Electro optical modulation is seen from 5.5 to 9 µm wavelength with an extinction ratio reaching 1dB. High speed operation is demonstrated up to 1 GHz, limited by the available experimental set-up. In terms of photodetection, room temperature operation is obtained from 5 to 8 µm wavelength, with internal responsivity up to 0.1 mA/W at 5 µm. While there is still room of improvement in terms of efficient, it is believed that these results pave the way for the integration of advanced optical functions in the mid-IR wavelength range.

Acknowledgements

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Influence of thickness in Ge-based plasmonic antennas for the detection of human serum albumin

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1. Introduction

The plasmonic properties of highly n-type doped Germanium (Ge) allow the use of localized surface plasmon resonances (LSPR) in bow-tie antennas to amplify the spectroscopic signal in the Terahertz (THz) spectral range. This feature enables the detection of biomolecules at very low concentrations [1, 2]. In particular, this capability was demonstrated qualitatively on lipoic acid [3] and quantitatively using various concentrations of bovine serum albumin (BSA) as bioanalytes [4, 5]. For the detection we monitored the analyte-induced shift of well-defined LSPR transmission resonance in the spectral range of 0.5–1.5 THz [2–4].

In this paper, we report on the protein detection capability of Ge/Si bow-tie antenna arrays fabricated using standard lithographic complementary metal-oxide-semiconductor (CMOS) processes in a 130 nm-SiGe pilot line. As a target analyte, we used human serum albumin (HSA), the most abundant protein in plasma, which was incubated and immobilized on antennas at various concentrations (0.3125–5 mg/mL). Using an optimized Ge-antenna thickness, we found resonant spectral shifts up to 5–6 GHz in response to HSA layers by concentration as low as 0.625 mg/mL.

2. Methods and experiments

2.1. Epitaxial growth of highly-doped Ge on Si

Layers of different n-doped Ge thickness were heteroepitaxial deposited on 200 mm Si (001) wafers and on 220 nm Si/2 µm SiO_2/Si (001) SOI substrates by means of reduced pressure chemical vapor deposition at 350°C. The Ge/Si layer was then capped by a 30 nm-thick Si_3N_4 layer and flash annealed at 700°C to improve the material quality. Bow-tie antennas formed a THz resonant structure with two trapezoidal arms and a subwavelength gap in between, as shown in Fig. 1a. Subsequently, a second 30 nm-thick Si_3N_4 layer was deposited to encapsulate the antennas. Two thickness, 1.3 µm (see Fig.1b) and 1.5 µm (see Fig.1c), were targeted to study the influence of the antenna height on the LSPR.

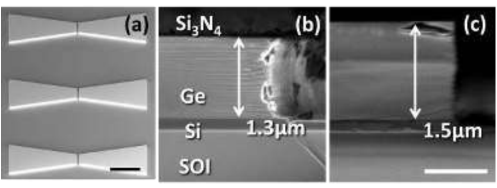

Fig. 1. SEM image of the Ge-based plasmonic antennas (Scale bar 20 µm) (a), SEM cross-sections of the analyzed antennas with 1.3 µm (b) and 1.5 µm (c) Ge thicknesses. (Scale bar 1µm).

2.2. THz Time-Domain Spectroscopy (TDS)

The spectral response of the Ge antennas, contained in a 6 mm x 6 mm chip, was studied by Terahertz time-domain spectroscopy (THz-TDS) in transmission mode using a TERASMART tool from Menlo GmbH in the frequency range *f*=0.2–5 THz with a resolution of 1.2 GHz, using a linearly polarized source [3, 4].

2.3. BSA and HSA incubation

In this study, HSA was used with the concentrations ranging from 0.3125 –5 mg/mL for comparison with BSA results from previous study [4]. In addition, Ge-antennas with different thickness were used and observed the sensitivity of structure, i.e. change of resonance frequency, to different HSA concentrations was monitored. The immobilization method was the same reported in the previous study [4]. After each step, the THz spectra of each sample at their respective concentration were measured by THz-TDS techniques.

3. Results

3.1. Height influence of the Ge epilayer

SEM cross sections of antennas with a Ge thicknesses of 1.3 µm and 1.5 µm can be seen in Fig. 1b and 1c, respectively. Also visible are the Si_3N_4 cap, the 220 nm Si growth layer and the SiO_2 box. Even if antennas with larger thickness could potentially have a larger field enhancement in the gap, we limit ourselves to Ge thickness compatible with subsequent back end of line (BEOL) steps. According to simulation, the field enhancement in 1.3 µm-thick Ge antennas is ~9% less than that of 1.5 µm antennas. The effect of the antenna thickness in the THz resonance of as-fabricated antennas is shown in Fig. 2. We can observe a decrease of 0.04 in the transmission corresponds to ~8% difference in the intensity for the thinner antennas.

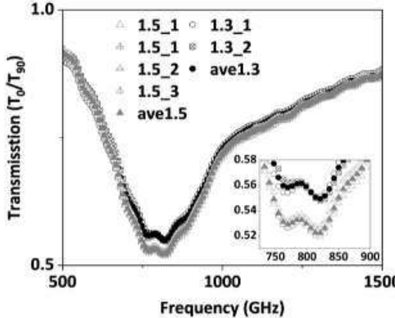

Fig. 2. Influence of Ge-thickness on the THz transmission at the antennas resonance obtained by TDS measurements.

3.2. Comparison of the resonance shift using HSA and BSA

To study the resonance shift due to the presence of a biolayer in direct contact with the plasmonic antennas, either BSA or HSA layers were incubated on 1.5 µm-thick antennas.

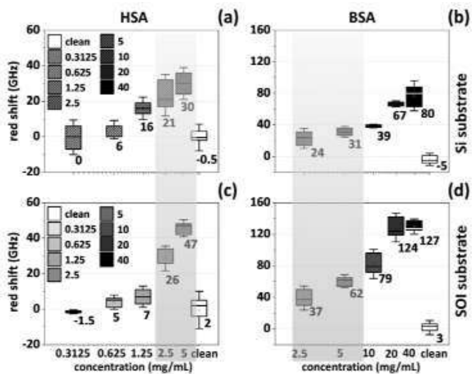

Fig. 3. Resonance shift due to the presence of either (a) HSA or (b) BSA. For different concentrations were tested (labelling each experimental point).

In Fig.3 we show the extracted data as a box plot diagram for the same antenna design and density on Si and SOI substrates as a function of the HSA and BSA concentrations.

We can observe a trend of resonant redshifts as the concentration increases up to a saturation concentration of 20 mg/mL (see Fig.3b and 3d). We notice also that the SOI-based samples (see Fig.3c and 3d) present the larger shifts compared to the Si-based samples (see Fig.3a and 3b) for concentrations from 2.5 to 40 mg/mL.

The box plot analysis also shows a perfect agreement of sensitivity at the 2.5 and 5 mg/mL concentrations for both BSA and HSA detection on Si and SOI substrate.

The HSA concentration of 0.625 mg/mL is the smallest concentration, which we can be reliably detected with the 6 and 5 GHz red shift for Si and SOI substrate, respectively.

4. Conclusions

In summary, we presented a THz biochip sensing platform consisting of highly n-doped Ge plasmonic THz microstructures with different Ge thickness based on Si/SOI substrates, entirely realized in an industry-standard CMOS foundry pilot line.
Furthermore, the lowest HSA detection limit for different thicknesses of Ge antennas was evaluated. Finally, the influence of the thickness of the highly doped antennas has been quantitatively determined.

Acknowledgements

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Ge-on-Si mid-infrared plasmonics

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1. Introduction

Silicon photonics is an ever-expanding market with an increasing number of applications. Plasmonics has not yet made its way to the microelectronic industry, mostly because of the lack of compatibility of typical plasmonic materials with foundry processes. In this context, we have undertaken the development of heavily-doped Ge films as novel plasmonic materials, grown on Si wafers with CMOS-compatible processes [1]. We will review the plasmonic applications developed in the framework and with the foreground of the project GEMINI ('Germanium mid-infrared plasmonics for sensing'), including antenna arrays for sensing [2], optically-activated antennas [3], and nanoantennas for nonlinear frequency conversion [4].

2. Fabrication and applications of Ge antennas

Plasmonic nanoantennas have been realized by electron-beam lithography and reactive ion etching techniques, starting from heavily-doped Ge films (electron density 10^{19}-10^{20} cm^{-3}) grown by low-energy plasma-enhanced chemical vapor deposition [1]. Post-growth annealing strategies represent a crucial optimization step to achieve uniform and full activation of the P dopants in the Ge matrix [5] and allowed us to demonstrate plasma frequencies covering the whole mid-infrared range up to about 3500 cm^{-1} (about 3 μm wavelength).

Compared to standard plasmonic metals such as Au, besides the crucial issue of the foundry compatibility, our analysis highlights that mid-infrared surface plasmons on heavily-doped Ge possess higher losses (and therefore shorter propagation lengths) due to the deeper penetration of the electromagnetic field inside the material but also a higher degree of field confinement [6], as also demonstrated by a theoretical analysis of the two respective figures of merit (see Figure 1).

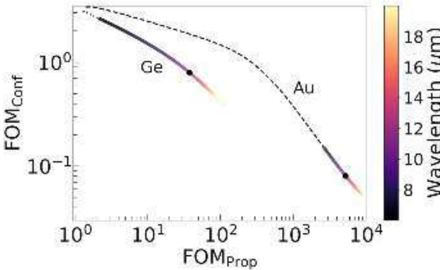

Fig. 1. Figures of merit for the field confinement (FOM_{Conf}) and the propagation length (FOM_{Prop}) in the mid infrared, calculated for Au and Ge following Ref. 7 [6].

The main investigated antenna structures are represented by single- or double-rod geometries [2-4, 8]. Other designs have also been explored, such as suspended Ge membranes with narrow slits, acting as slot antennas in the mid infrared [6], see Figure 2.

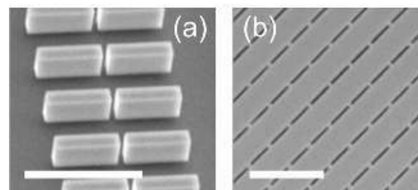

Fig. 2. Representative SEM images of (a) plasmonic Ge gap antennas on a Si substrate and (b) slot antennas on a suspended Ge membrane. Scale bars are 5 μm.

As a benchmark application, we target the sensing of thin molecular/polymeric layers in the fingerprint region. Figure 3 demonstrates the spectroscopic characterization of the main resonances supported by the rod geometry (panel a) and a representative sensing experiment in which the Si–C stretching modes of PDMS around 800 cm^{-1} are detected with single- and double-rod geometries, demonstrating an enhancement of about 2 orders of magnitude for the

material in the gap of the double-rod antenna [2].

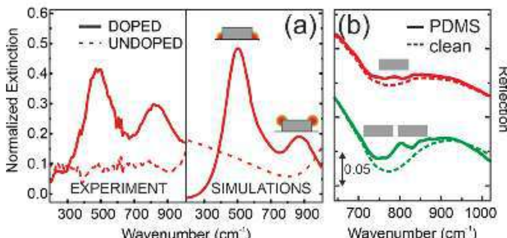

Fig. 3. (a) Extinction spectroscopy (optical experiments and finite-difference time-domain simulations) of Ge plasmonic rod antennas, highlighting their two main dipolar resonances. (b) A benchmark sensing experiment addressing a thin PDMS layer with single- and double-rod Ge antennas [2].

We also exploit ultrafast laser technologies to demonstrate plasmon-enhanced third harmonic generation in the mid infrared, the ultrafast optical activation of mid-infrared plasmonic resonances in undoped antennas, and the time-domain experimental analysis of the plasmonic antenna response.

Third-harmonic generation is excited in the plasmonic Ge antennas with 300-fs narrowband mid-infrared laser pulses obtained by difference frequency generation. By exciting individual antennas with varying arm length, we are able to tune the antenna resonance to the excitation wavelength and demonstrate the plasmonic enhancement in the efficiency of the nonlinear optical conversion (see Figure 4) [4].

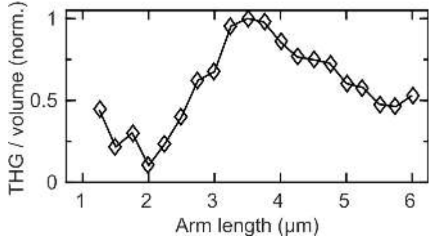

Fig. 4. Third-harmonic emission from individual Ge antennas with different arm lengths, after excitation with laser pulses centered at a wavelength of 12 μm, demonstrating plasmon-enhanced generation when the antenna is resonant with the excitation wavelength (arm length around 3.5 μm) [4].

The ultrafast activation of undoped Ge antennas is achieved via optical doping exploiting sub-20 fs pulses with energies up to 15 μJ at a central wavelength of 1050 nm, leading to a high concentration of free carriers that support a plasmonic behavior up to approximately 2000 cm^{-1}. The antenna resonances are probed by mid-infrared pulses generated via difference frequency generation [3]. Finally, we successfully exploited time-domain electro-optic sampling to demonstrate time- and field-resolved detection of the response of a single plasmonic antenna in the mid infrared with sub-optical-cycle precision [8].

3. Conclusions

Our results represent a benchmark for group-IV mid-IR plasmonics and confirm that CMOS sensing platforms could benefit from plasmonic enhancements provided by integrated Ge-based devices. They also pave the road for the exploitation of mid-infrared semiconductor technologies in the field of ultrafast nano-optics and nonlinear optical conversion at the nanoscale.

Acknowledgements

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SiGe parabolic quantum wells for strong light-matter coupling at THz frequencies

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1. Introduction

In an optical cavity, the strong-coupling regime of light matter-interaction can be observed by measuring the interaction between an electronic transition (matter) and the resonant photonic cavity mode. Typically, the strong coupling regime is achieved when the a-priori degeneracy between the energies of electronic and photonic modes is lifted, and two polariton states are created with mixed light and matter character. The energy separation between the two polariton modes (called Rabi splitting) can be observed spectroscopically [1].

Recently, intersubband (ISB) transitions in semiconductor quantum wells have become an ideal model system for strong-coupling studies due to the relatively low value of the electromagnetic frequency in the mid-infrared and terahertz ranges where ISB transitions are observed (the mode frequency is at the denominator of the strong-coupling parameter), and the possibility to modulate the Rabi splitting by controlling the charge density in the quantum wells (at the numerator in the strong-coupling parameter).

Foreseen applications include the development of novel quantum devices such as emitters, photodetectors and optical modulators with increased efficiency. So far, all studies about ISB polaritons have been conducted in III-V semiconductor quantum wells. In particular, parabolic quantum wells (PQWs) have been identified as an optimal system to achieve the strong coupling regime in the THz as the energy separation of the subbands is constant (the system behaves as a quantum mechanical harmonic oscillator) and the ISB spectral features are theoretically independent from electron sheet density and temperature, making accessible the strong coupling regime also at room temperature [2].

In this work, we aim at demonstrating the existence of ISB polaritons in the silicon-foundry-compatible group IV SiGe material system, employing $Si_{1-x}Ge_x$ PQWs grown by ultra high vacuum chemical vapor deposition (UHV-CVD) on silicon wafers. The foreseen operation frequency is in the range 2 to 5 THz. In order to obtain very high oscillator strength and single-frequency matter resonance spectra in this range, parabolic quantum wells have been designed, grown, and characterized structurally and optically. The parabolicity of the $Si_{(1-x)}Ge_x$ profile has been evaluated by X-ray diffraction (XRD) and Secondary Ion Mass Spectrometry (SIMS). Fourier Transform infrared (FTIR) spectroscopy has been carried out to measure the ISB absorption resonances.

The fabrication process of microcavity arrays is under development and it includes heavily doped semiconductor layers used as cavity mirrors, a choice that eliminates the typical post-processing steps of double-metal photonic cavities and makes the final devices compatible with scalable foundry technology. Electromagnetic design, simulations and preliminary spectroscopy data taken on arrays of microcavities filled with $Si_{1-x}Ge_x$ parabolic quantum wells will be presented.

2.Results and discussion

The compositional graded $Si_{1-x}Ge_x$ PQW samples have been grown by UHV-CVD on a reverse graded SiGe virtual substrate deposited on Si(001). The parabolic compositional profile is obtained by keeping the GeH_4 gas flow constant and varying the SiH_4 flux. The module, composed by the parabolic well and a $Si_{0.20}Ge_{0.80}$ barrier, has been repeated 20 times. The samples investigated were n-doped by phosphine co-deposition in the center of the $Si_{0.20}Ge_{0.80}$ barriers, leaving an undoped $Si_{0.20}Ge_{0.80}$ layer between the dopants and the well to reduce ionized impurity scattering.

Two samples with a different parabolic profile width W have been deposited, in order to change the ISB transition energy that can be estimated as $E_0 = \hbar\omega_0 = \hbar(8\Delta_0 / W^2 m_z^*)^{1/2}$, where Δ_0=120 meV is the maximum barrier height (band offset) and m* = 0.13 is the electron effective mass in the z-direction [2]. Sample A has W_A=46 nm and sample B W_B=70 nm.

Their expected ISB transition energies are therefore about 17 and 11 meV, respectively.

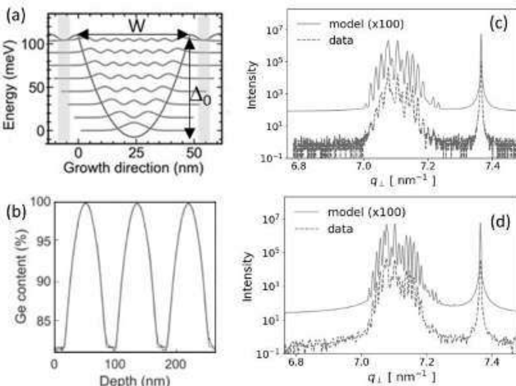

Fig. 1: (a) Calculated electron energies and squared wavefunctions in PQWs of sample A. (b) SIMS composition profile and parabolic fit of sample B; (c), (d) XRD (004) $\theta/2\theta$ curves of the samples A and B, respectively.

The parabolicity of the $Si_{1-x}Ge_x$ compositional profile of the PQWs has been accurately assessed by SIMS, as shown in Fig. 1(b) where the SIMS profile of sample B, is reported and compared to the parabolic fit. A similar result has been obtained on sample A [3]. Figure 1(c) and (d) show the XRD (004) $\theta/2\theta$ curves of sample A and B respectively, together with the result of the dynamical diffraction model simulations made assuming a parabolic profile. The high quality-factor of the superlattice interference fringes evidences the sharp periodicity of the multiple PQW structure. Moreover, the good agreement between XRD data and simulations confirms the parabolic shape of the compositional profile.

The two samples were coated with Ti/Au, cut into prism waveguides, and mounted in an FTIR spectrometer with an optical cryostat. In Fig. 2 (a) and (b) the ISB absorption spectra of sample A and B are reported. A single strong absorption peak which is the signature of the ISB transition is present in both cases. The peak maxima are at 19 meV (sample A) and 11 meV (sample B), in good agreement with the estimation based on the well profiles of the two samples. The sheet carrier concentration estimated from the spectra is about $3.5x10^{11}$ cm^{-2} in sample A and $1.5x10^{11}$ cm^{-2} in sample B. Such difference can explain the narrower FWHM of sample B (3 meV) with respect to that of sample A (6 meV), in agreement with previous reports for square QWs with similar doping profiles [4]. Interestingly, the dichroic transmission spectra of sample A acquired at different temperatures in the range between 10 and 300K and shown in Fig 2(a) do not change with temperature, as expected in parabolic-shaped QWs.

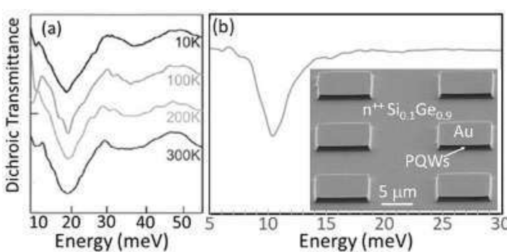

Fig. 2: (a) Temperature dependence of the dichroic transmittance of sample A (b) Dichroic transmittance of sample B (T=100K). The inset in panel (b) shows the SEM micrograph (65° tilted view) of an array of square mesas etched by ICP in a $Si_{0.10}Ge_{0.90}$ sample. The array has been designed to match the cavity resonance with the ISB absorption energy of sample B. On the SEM image the components of the complete device for ISB polaritons investigation are reported.

These achievements indicate that the improvements made in the epitaxy of Ge-rich SiGe heterostructures make this material platform competitive with respect to the III-V semiconductor one [3,5] and thus promising for strong-coupling applications. In this perspective, we developed the fabrication process of microcavity arrays on SiGe heteroepitaxial wafers made of square patch resonators with the Metal-Insulator-Metal structure [6]. An array of square etched mesas on a $Si_{0.10}Ge_{0.90}$ dummy sample is shown in the inset of Fig. 2. As sketched, the complete microcavity array includes an Au layer on top of the mesas and an n^{++} $Si_{0.10}Ge_{0.90}$ back mirror, with the PQWs in between. The array period is twice the square size *s*, so that *s* is the only parameter that governs the cavity mode. The cavity mode detuning from the ISB resonance can be varied by changing *s* to demonstrate the ISB polaritons development. The development of arrays of microcavities filled with $Si_{1-x}Ge_x$ parabolic quantum wells and their THz spectroscopy characterization for the investigation of ISB polaritons are in progress.

Acknowledgements

This work has been supported by Regione Lazio, program POR FESR 2014-2020, project n. A0375-2020-36579 “Teralaser” and by the European Union’s Horizon 2020 research and innovation program under Grant Agreement No. 766719 (FLASH).

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Mid-infrared nonlinear optics with Ge quantum wells

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1. Introduction

Photonic integrated circuits (PICs) working in the Mid- infrared (MIR) have received in the last years a great attention due to the variety of potential applications in medical diagnostics, analytical chemistry, environmental monitoring, and sensing for safety and security. In this framework second-order nonlinear phenomena are key to achieve high-speed optical modulation via the Pockels effect, f-2f frequency-comb self-referencing, and also direct frequency-comb generation by cascaded second-order effects that mimic third-order nonlinear effects, but with higher efficiency. Many research efforts have been dedicated to achieve second-order nonlinearities in silicon PICs. To this aim, the SiGe material system represents a natural choice, thanks to its prompt integrability with the CMOS standard. Indeed bulk Si and Ge are compatible with PIC foundry processes, but unfortunately both feature vanishing second-order susceptibility $\chi^{(2)}$ due to their centrosymmetric unit cell. A promising way to circumvent this limitation is to resort to "artificial" non-linearities in asymmetric semiconductor quantum wells (QW). In fact, such heterostructures can be specifically tailored to realize resonant intersubband transitions which, thanks to their large oscillator strength, guarantee an unmatched enhancement of the second order nonlinear susceptibility $\chi^{(2)}$ with values typically falling in the 10^4-10^5 pm/V range. In this work we present our recent experimental results about second harmonic generation in the MIR using Ge/SiGe asymmetric QWs, as well as a theoretical investigation of their potential performances in waveguide-integrated photonic devices.

2. **Demonstration of MIR SHG.**

The demonstration relies on an asymmetric coupled QWs architecture that has been designed by means of an advanced semi-empirical first-neighbor $sp^3d^5s^*$ tight-binding Hamiltonian model which includes also the spin-orbit interaction [1]. This multi-orbital description ensures that all the relevant effects related to the subband non-parabolicity and to the momentum-dependence of the dipole matrix elements, which for p-type structures operating at room temperature (RT) are expected to play a relevant role, are properly taken into account. The model has been used to calculate the absorption spectrum and the $\chi^{(2)}$. The sample, whose epitaxial scheme is reported in figure 1a, has been grown by low-energy plasma enhanced chemical vapor deposition.

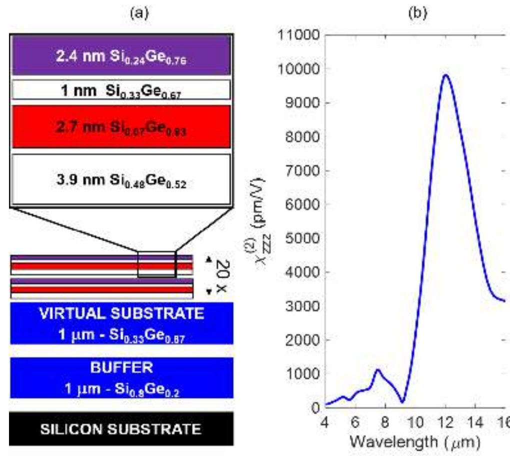

Figure 1: Epitaxial scheme (a). Calculated $\chi^{(2)}_{zzz}$ (b).

A low-temperature growth procedure has been specifically developed for this sample in order to minimize the inter-diffusion.

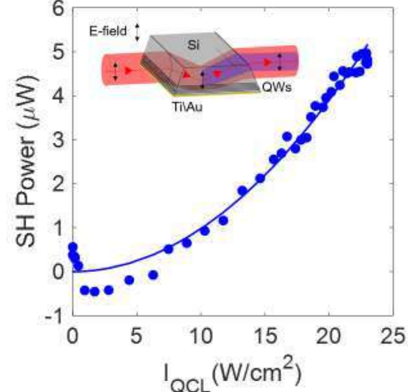

Figure 2: SH power as a function of the pump intensity.

The sample has been then cut into a prism waveguide

in order to characterize it in TM polarization (Fig 2, inset). A strong second harmonic generation [2] has been measured by pumping the sample with a continuous wave quantum cascade laser emitting at λ = 10 µm (fig. 2).

3. Study of waveguide integration

In order to fully exploit the potential of artificial nonlinearities, we have theoretically investigated possible waveguide integration schemes and the expected performances in terms of conversion efficiency.

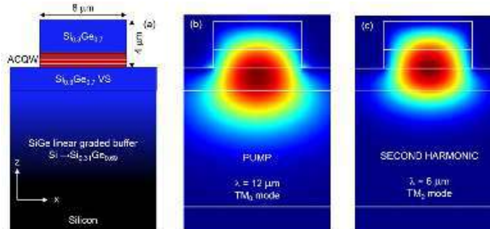

Figure 3: Rib waveguide scheme (a). Electric field distribution in the zx plane, for the TM_0 mode at the pump (b) and second harmonic (c) wavelengths.

In order to integrate the ACQWs, we choose a rib waveguide featuring a SiGe forward graded buffer, which serves as an high quality virtual substrate for the ACQW stack, as well as a waveguiding layer, by taking advantage of the higher refractive index of Ge with respect to Si. The waveguide geometry has been designed by the Lumerical software package, and as can be seen in figure 2 (b) and (c) it ensures single mode operation both at the pump and at the second harmonic wavelength in TM polarization. The second harmonic conversion efficiency has been calculated by numerical integration of the nonlinear coupled mode equations [3] as a function of the propagation distance and by considering different thicknesses of the ACQW stack. The results, assuming perfect phase matching and considering the phase mismatch are reported in Figure 4 (a) and (b) respectively. In phase matching condition, the second harmonic emission increases as the propagation length increases due to the strong conversion efficiency provided by the ACQWs. Then it reaches a maximum and decays for the combined effect of pump depletion and second harmonic re-absorbtion. Strikingly η increases for decreasing N, with a maximum efficiency of η = 0.63 %/W with N = 1 ACQW. If the phase mismatch is taken into account, the conversion efficiency shows a periodic trend, with multiple peaks, whose amplitude is progressively damped by the absorption. The SH conversion efficiency clearly increases by increasing the number of ACQW, reaching a maximum η of 0.4%/W for N = 100, with a propagation length of only 100 µm. Interestingly one can notice that the maximum efficiencies achievable in PM and not-PM are almost the same for large N. This is due to the rather high optical absorption coefficients at the pump and second harmonic wavelengths which, for large N, fully damps the second harmonic field well before it reaches a propagation distance comparable to the coherence length, which is of ~ 600 µm for N = 200.

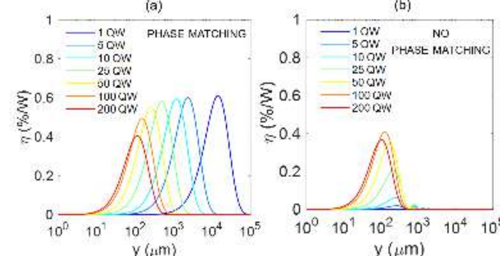

Figure 4: Second harmonic generation efficiency as a function of the propagation length, for different values of N, in phase-matching (a) and non phase-matching (b) conditions.

4. Conclusions

Second harmonic generation at mid-infrared frequencies, relying on artificial nonlinearities engineered in Ge/SiGe ACQWs has been experimentally demonstrated.

The nonlinear conversion efficiencies achievable in waveguide integrated ACQWs at room temperature have been theoretically investigated. A particular attention has been devoted to understand the role played by the number of ACQWs in phase matching and phase mismatched conditions. The results show that Ge/SiGe ACQWs is an interesting and promising material platform to exploit second order nonlinear effects in PICs at mid-infrared frequencies.

Acknowledgements

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Photonic Properties of Self-Assembled Semiconductor Microstructures

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1. Introduction

The ever-expanding photonics industry is constantly developing advanced and reliable ways to generate, manipulate, and detect light. The understanding and control of light-matter interaction is paramount for the development of efficient photonic devices to be applied in a wide range of technologies, e.g., from sensing to quantum computing.

Group-IV semiconductors, besides having advantageous optical properties, are interesting because of their compatibility with microelectronic fabrication techniques and could be readily implemented into industrial processes. Research is currently attempting to find ways to overcome some of the limitations of group-IV elements, such as the mediocre light emission efficiency caused by the indirect bandgap, or the lattice mismatch that restricts heteroepitaxy. Some of these issues can be tackled through the out-of-equilibrium growth of semiconductors on patterned Si seeds, that has been shown to yield vertically aligned epitaxial microcrystals whose morphology can be precisely controlled by changing the fabrication parameters. This process results in heterostructures with numerous degrees of freedom to be tuned to obtain a system with the desired characteristics. [1,2]

Such self-assembled microcrystals stand out for their exceptional optical properties: the growth on a patterned substrate prevents the formation of cracks and elastically relaxes stress, even reducing the density of dislocations by aspect-ratio trapping. Moreover, the epitaxial nature of the synthesis generates high-quality crystallographic facets with few scattering and nonradiative recombination centers. [3] The vertically aligned microcrystals show great promise for their application in photonics, but until very recently, little work has been done to understand their interaction with light.

In this work, we present some results on the analysis of light-matter interaction and of the photonic properties of homo- and heteroepitaxial group-IV semiconductor microcrystals.

2. Discussion

2.1. Antireflection

The microcrystals are composed of semiconductors with a high refractive index (e.g., $n_{Si}>3.5$, $n_{Ge}>4$), generating photonic effects. Among such properties, antireflection has a key role in the development of high efficiency detectors, particularly for low-intensity operation. The reflectivity of a model system composed of homoepitaxial Si microcrystals on Si seeds presents a strong, 40% decrease with respect to a flat continuous layer. Finite-difference time-domain simulations show that this reflectivity decrease is determined by a ~2-fold increase in the absorption efficiency of the Si microcrystal. Moreover, the simulation of the absorption profile demonstrates that the faceted top surface redirects light towards the center of the microcrystal, where a device can be selectively located during design, thus maximizing its final performances. [4]

2.2. Photonic bandgap

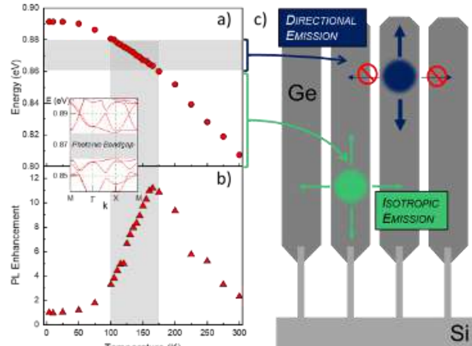

Fig. 1: a) Temperature shift of the Ge PL. The grey area is the energy of the PBG. b) PL increase with respect to a flat Ge film. Inset: photonic bandstructure calculated via FEM simulations. c) Scheme of the light routing concept.

Epitaxial microcrystals grown on patterned substrates can be considered as two-dimensional (2D) photonic crystals (PCs), which are usually fabricated by lithography and etching. Such process can be slow, and the etched surfaces can be irregular and unpassivated, possessing numerous nonradiative recombination centers. The epitaxial nature of the vertically aligned microcrystals can possibly

overcome these issues.

Finite elements method (FEM) simulations predict the appearance of a high-energy photonic bandgap (PBG) in a PC composed of heteroepitaxial Ge-on-Si microcrystals (inset in Fig. 1), whose presence can be investigated with the help of photoluminescence (PL). When the PL of the Ge microcrystal is off resonance with respect to the PBG, the emission is isotropic. However, by changing the energy of the Ge PL through the lattice temperature, it is possible to bring the emission in resonance with the PBG (Fig. 1a). In this configuration, light cannot propagate in the periodicity plane and is re-routed towards the vertical direction, increasing the collected signal (Fig. 1c). At the temperature at which the PL resonates with the PBG, the detected PL intensity demonstrates a ~10-fold increases with respect to a continuous Ge-on-Si reference film (Fig. 1b), proving experimentally the presence of the PBG in the Ge-on-Si microcrystal system. [5]

2.3. Topological properties

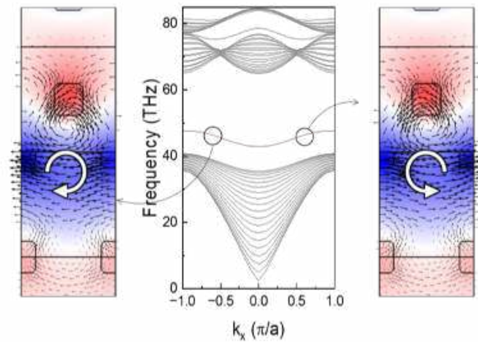

Fig. 2: Simulated bandstructure of an interface between trivial (top) and topological (bottom) photonic crystals. The electric field maps highlight the propagation direction of the localized interfacial mode.

Topological insulators are systems that possess an insulating bulk but conductive surface states. PCs are at the frontier of research on topological properties of matter because of their fabrication flexibility, that allows to explore the emergence of topological effects in a controllable and reproducible way on synthetic structures. The transition from a trivial to a topologically nontrivial structure occurs through the breaking of the symmetry of the unit cell of the PC, which determines an inversion of one of the degrees of freedom that describes the system (e.g., the band character of the high- and low-energy bands around the PBG). [6]

The 2D epitaxial microcrystal lattice can be described as the repetition of two distinct unit cells shifted by half a lattice constant. The first has a microcrystal in the center (*compressed* structure); the second has four quarters of a microcrystal in the corners of the cell (*expanded* structure). The two structures can be considered as the extreme case of a 2-dimensional Su-Schrieffer-Heeger lattice, a typical configuration for a topological PC.

FEM simulations demonstrate that the two distinct unit cells have the same bandstructure, with a key difference: in the X-point of the *expanded* structure the parity of the electric field is inverted, hence a topological transition has occurred.

A straightforward evidence for the presence of a topological transition is the emergence of spatially confined guided modes at the boundary between two regions with different band topology. The simulation of the interface between expanded and compressed unit cells shows that a localized mode appears at the interface between the insulating bulks. The localized mode is chiral, which means that light travels in opposite directions, depending on its helicity. Moreover, such a mode is topologically protected, therefore (thanks to symmetry constraints) it does not experience scattering, making propagation extremely efficient. Using this concept, it is possible to fabricate complex photonic structures, such as polarization-dependent waveguides, resonators, filters, and cavities. The possibility of including complex heterostructures in the vertically grown microcrystals could allow for the development of efficient group-IV photonic components working in a large spectral range, from the near-IR to the THz.

3. Conclusions

Vertical heteroepitaxial microcrystals promise to be extremely powerful for photonic devices. The high quality of such materials and the flexible synthesis allow for their application to both light detection and emission. Of particular interest is the possibility to design a 2D heteroepitaxial topological photonic crystal that could be applied to several photonic components of technological relevance.

Acknowledgements

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Exploitation of the natural instability in SiGe-based thin solid films for sensing and photonic applications

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1. Introduction

Silicon-based nanocrystals represent a promising resource both for next generation electronic devices and for nano-photonics applications. Their exploitation, however, requires precise size, shape and position control [1,2]. Owing to their large surface-area-to-volume ratio, thin semiconductor solid films are often unstable upon annealing. As such, under the action of surface diffusion, the film breaks eventually forming isolated islands when heated at temperature well-below the melting temperature of the bulk material. This phenomenon, known as solid-state dewetting, is one of the main factors impeding the use of ultra-thin silicon films on insulators (UT-SOI) for the further miniaturization of electronic components.

Here, we demonstrate the ultimate control of Si and SiGe-based thin films dewetting for the precise formation of complex nano-architectures, and their exploitation as dielectric nano-antennas and field-effect transistors wire. These nanostructures can feature extremely reduced fluctuations of size, shape and position (a few %) over hundreds of repetitions and on large scales [3,4]. The dielectric antennas are realized exploiting the natural mechanical instability of thin solid films to form regular patterns of monocrystalline atomically smooth silicon and germanium nanostructures that cannot be realized with conventional methods. Solid state dewetting (SSD) indeed is a natural shape instability occurring in thin solid films when heated at high temperature: it transforms a flat layer in isolated islands in a timeframe independent from the sample size. However, its potential for applications based on complex pattern formation is still unexplored in spite of the manifold advantages it offers: a) it forms monocrystalline and facetted (atomically smooth) structures (size from ~nm up to ~10 µm), free from defects and from the typical roughness produced by conventional etching methods; b) the islands are directly formed on an insulating substrate (SiO_2); c) spontaneous dewetting can produce over arbitrary scales patterns that cannot be designed numerically. Therefore, SSD can be efficiently exploited in all these fields to form perfectly ordered and complex nano-architectures over large scales, as well as randomly organized, isolated islands. The solid state dewetting initiated at the edges of the patterns controllably creates the ordering of nanocrystals with *ad hoc* placement and periodicity. The size of the dewetted material is tuned by varying the nominal thickness of the semiconductor thin film while their position results from the association of film retraction from the edges of the layout and Rayleigh-like instability.

By a properly combining e-beam lithographic and reactive ion etching processes, we can realize dewetted nanostructures that can play as Mie resonators. One of the main key features of high-refractive-index dielectric Mie resonators is that their optical spectra display strong multipolar electric and magnetic resonances. As a building material for such resonators Si or SiGe particles are very promising, since their absorption losses are very weak at visible and near-infrared frequency. Furthermore, differently from metallic particles used in plasmonic (e.g., gold, silver, aluminum), they are compatible with silicon-based nanofabrication technologies being, therefore,

more appealing for low-cost production and integration in electronic devices.

2 Results

In order to understand the optical behavior of a single dewetted structure, we exploit a fabrication process in which arrays of islands are obtained through solid state dewetting of Si or SiGe squares patterned by a combination of e-beam lithography and reactive ion etching. Specifically, the resonator fabrication process starts from a silicon-germanium-on-insulator (SGOI) with SiGe layers of 26 nm with a Ge content both of 20% and 30% on 7 nm Si layer itself on a 25 nm of SiO_2 box. The Ge content variation does not significantly modify the refractive index of the material, but it changes the dewetting dynamics. E-beam lithography is performed on negative resist at 30 KeV and the pattern exposed is transferred onto the substrate by reactive ion etching with CF_4. The layout obtained is reported in Figure 1.

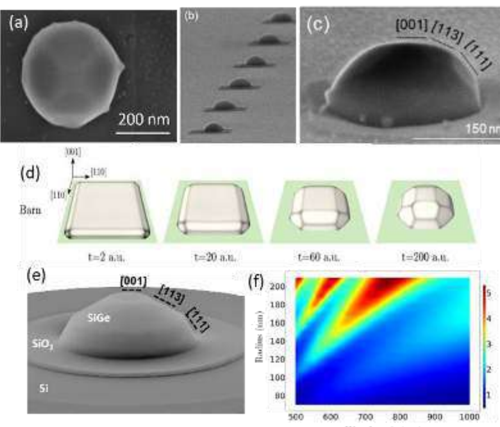

Fig. 1. (a) SEM top view image of a single dewetted Si0.7Ge0.3 island. (b) SEM image of islands acquired with a tilt angle of 45 degrees with respect the sample normal to highlight the faceting of each scatterer. (c) SEM image of of a single island, where the faceting planes {001}, {113} and {111} are labelled. (d) Phase field simulation of solid-state dewetting of patches with morphologies and contact angle compatible with a cupola shape. (e) 3D sketch of the SiGe resonator on the SiO2 pedestal used for FEM simulation. The crystallographic planes are labelled. (f) FEM scattering cross section in function of the radius size and for a fixed aspect ratio of 0.6

It consists of an array of square patterns with lateral sizes varying from 200 nm to 700 nm and a periodicity of 3 µm. These samples are then annealed in a dedicated machine at temperature of 800°C for 15 min at 10-10 torr, inducing the dewetting process [Figure1 (b,c)], forming 3D shape islands due to surface energy minimization [5,6]. Predictive phase-field simulations of the mass transport mechanism, assess the dominant role of surface diffusion providing a tool for further engineering this hybrid top-down/bottom-up self-assembly method [Figure 1(d)]. In contrast with more conventional top-down fabrication approaches where only cylinders can be obtained, this method enables a true 3D shaping of the nanoislands. The optical response of the nanoislands has been also evaluated by means of a commercial 3D finite element solver (Comsol Multiphysics). The simulations revealed thatnanoislands support multiple resonances whose spectral position undergoes a significant red shiftas the radius of the nanoparticle increases [Figures (e), (f)]. The results of the dark field spectroscopy show a good agreement between the simulation and the experimental data: the position of the peaks is perfectly reproduced, while the mismatching with respect to the intensity can be ascribed to the asymmetry of the resonator shape respect to the simulated one.

3. Conclusions

We showed that solid-state dewetting is extremely well promising for fabricating sub-micrometric ordered dielectric nano-antennas. We experimentally demonstrate that the nanoislands effectively behave as resonant nanoantennas, whose resonance frequency is governed by size, shape and composition and thus constitutes a precise probe of the dewetted material's homogeneity. The dewetted Si1-xGex islands provide an excellent platform for light manipulation at the nanoscale and for heterogeneous integration of photonic devices in the Si microelectronic platform

Acknowledgements

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Suitability of highly Doped Groupe IV semiconductor for spectral narrow plasmonic MIR detection devices

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1. Introduction

Plasmonic antennas can be used to enhance light-matter interaction with possible applications in improving optoelectronic device performance. For example, plasmonic antennas offer the possibility for boosting hot carrier photodetection for selected wavelengths [1]. While for the visible and NIR wavelength region metals are well studied and suited for this task, in the MIR wavelength region metals exhibit large ohmic losses and long plasmon confinement lengths. In contrast, heavily doped semiconductors with their, compared to metals, low electron density are promising candidates to replace metals and enable plasmonics in the MIR region [2, 3] . In particular, group-IV semiconductors such as SiGe, Ge and GeSn have the additional advantage of a non-polar lattice, free of infrared-active phonons. It was shown that and a plasma wavelength of $\lambda_p = 2.6$ µm could be achieved in n-type doped Ge with high carrier concentrations up to $N_D = 2.6 \times 10^{20}$ cm^{-3} [4].

Nevertheless, to build fully functioning plasmonic hot-electron photodetectors there are stronger requirements that need to be met: not only the lowering of the plasma wavelength but also the increase of the crystal quality and therefore of the carrier mobility. A short relaxation time is crucial to achieve good device performance. Besides the material requirements, the design of the sensor needs to enable electrical contact, for which standard dipole nano-antennas are not suitable. Also, plasmonic modes that are typically used for hot carrier excitation e. g. localized surface plasmon resonances (LSPR) in general are rather broadband, which makes them less ideal for detectors with narrow spectral resolution. Coupling LSPR with a diffractive mode, e. g. a Rayleigh anomaly, leads to the formation of surface lattice resonance (SLR) with concomitant narrow extinction peaks of plasmonic nano-antennas, this may be crucial to achieve detector performance improvement in the MIR region.

Here we present different material growth approaches, as well as post-growth processing, to optimize the material parameters as well as a possible device design that allows to electrically contact the plasmonic antennas and to optimize the excitation of SLR. By simulative optimization (carried out using the software Lumerical [5]) of the SLR, narrow extinctions peaks with high extinction values are predicted and could also been shown in fabricated comb-like antennas.

2. Device Geometry

To spatially remove the electrical metal contact from the optical active part the antennas were designed as a comb-like antennas, where an array of long rib antennas is connected at one end, forming a comb and allowing the rib antennas themselves to be out of range of the contact metal. By tuning the width and the pitch of these antennas the spectral position of the LSPR and the RA can be tuned and optimized to achieve narrow and high extinction peaks (Fig. 1).

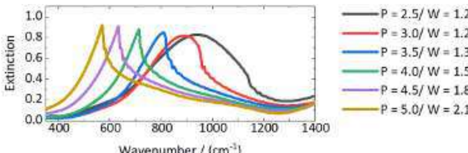

Fig. 1. Simulated extinction spectra with narrow spectral features.

3. Material Growth and parameter Measurements

To optimize the material parameters, different growth strategies, and additional post-growth pulsed laser melting (PLM) were used [6]. The samples discussed here were grown via molecular beam epitaxy (MBE) and by chemical vapor deposition (CVD). The PLM was performed using two different energy densities (0.3,0.5 J·cm^{-2}). Material permittivities are well described by a Drude model, whose parameters were obtained via absolute reflection measurements performed with a Fourier Transform IR (FTIR) spectrometer and fitted with the software RefFit [7].

For the MBE samples the active dopant concentration of the antenna layer was obtained from Hall effect measurements in a temperature range from 300 K to 10 K. The layer stack consists of 100 nm Ge-VS followed by 500 nm of a $Ge_{1-x}Sn_x$ buffer in which the Sn concentration was ramped up from 0.1 % to the final Sn concentration. Afterwards a 200 nm thick p-type doped $Ge_{1-x}Sn_x$ layer with a dopant concentration of $N_A = 1x10^{17}$ cm^{-3} was grown to form a PN junction. At last, the 500nm (group A), 400nm (group B) $Ge_{1-x}Sn_x$ n-type doped antenna layer with a nominal dopant concentration of $N_D = 1x10^{20}$ cm^{-3} or $N_D = 3x10^{20}$ cm^{-3} respectively was deposited. The nominal Sn concentrations were chosen to be $c_{Sn,nom} = (0, 2.5, 5, 7.5)$. PLM treatment was only performed on the samples of group B, to activate more of the dopants and increase crystal quality.

For the CVD layer the active dopant concentration was obtained from the optical data. The stack consists of a 2.8 µm thick Ge-VS followed by a 1.1 µm thick undoped $Si_{0.09}Ge_{0.91}$ buffer layer, and the 1 µm thick n-type doped $Si_{0.09}Ge_{0.91}$ antenna layer with a nominal dopant concentration of $N_D = 2x10^{19}$ cm^{-3}.

Introducing Sn into the Ge matrix lowers the plasma wavelength without decreasing the relaxation time by a large amount (Table 1). By using PLM the active dopant concentration as well as the crystal quality can be increased, allowing to lower the plasma wavelength down to 3.6 µm and making this material suitable for even lower wavelengths than MIR. The plasma wavelength is much longer in the present CVD material due to the lower dopant concentration and therefore it can only be used in the longer wavelength region towards the THz range. However, the relaxation time exceeds that of the untreated MBE samples although the CVD material contains 9% Si, making this a promising material for sharp SLR peaks.

Table I. Drude parameters obtained by optical measurements.

Sample ID	Sn/Si con. (%)	PLM (Jcm^{-2})	N_D (10^{20} cm^{-3})	λp (µm)	τ (fs)
MBE A.1	0/0	-	0.457	6.9	20.9
MBE A.2	2.5/0	-	1.31	6.1	14.1
MBE A.3	5/0	-	1.08	6.5	12.7
MBE A.4	7.5/0	-	0.97	6.6	11.1
MBE B.1	0/0	0.3	0.98	8.9	29
		0.5	1.35	4.6	41
MBE B.2	2.5/0	0.3	2.32	5.0	8.2
		0.5	3.20	3.6	8.7
MBE B.3	5/0	0.3	1.81	4.4	53
		0.5	2.08	3.8	15
MBE B.4	7.5/0	0.3	3.41	4.7	5
		0.5	4.03	3.9	10
CVD	0/9	-	0.14	12.5	23.9

4. Device fabrication and optical extinction spectra

Out of the MBE samples comb-like antennas were fabricated using optical lithography and ICP-RIE etching techniques. Extinction spectra were obtained from FTIR transmission spectra of the device T_D and the substrate T_{BG} as follows:

$$E_x = 1 - T_D/T_{BG}. \quad (1)$$

Figure 2 shows the measured extinction of a comb-like antenna. While the main peak is broadened compared to simulation it is nonetheless well defined. We discuss possible applications in hot-electron photodetection.

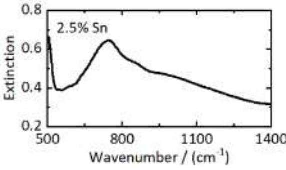

Fig. 2. Extinction spectra for a comb-like antenna made from GeSn (A.2) with 3.5 µm pitch and a width of 1.3 µm.

5. Conclusions

Controlling the material quality while tuning the active dopant concentration in SiGe, Ge and GeSn alloys is crucial for enabling plasmonic devices based on doped Group IV semiconductors. Using CVD the high crystal quality increases the relaxation time whereas the high possible doping via MBE and PLM treatment allows to lower the plasma wavelength. We demonstrate that comb-like antennas with sharp and high extinction peaks can be realized, showing that Groupe IV semiconductors are suitable for plasmonic devices with narrow spectral features in the MIR.

Acknowledgements

We would like to express sincere thanks to the 4th Physical Institute of the University of Stuttgart for the access to their FTIR Setup.

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How Ge Affects the Valley Splitting in Si Quantum Wells

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1. Introduction

Spin qubits, formed by electrostatically confining electrons in a SiGe/Si/SiGe quantum well, experience a two-fold valley degeneracy that can compete with the spin degree of freedom in defining the qubits. This is a serious problem for scaling up to large numbers of qubits. In principle, the problem can be solved by increasing the valley energy splitting. However, the valley splitting is very poorly controlled in these devices, with significant variability in quantum dots formed on the same chip. In fact, the standard deviation of the valley splitting is typically as large as its mean value, and in many cases, the valley splitting is too small to form well-defined qubits.

In this talk, I will show that the main reason for the valley splitting variability arises from the random nature of the SiGe alloy. Small layer-by-layer fluctuations of the Ge concentration within a dot lead to random valley couplings that tend to overwhelm engineering schemes for enhancing the valley splitting. I will also discuss two promising strategies for addressing this challenge [1,2], both of which rely on introducing Ge directly into the quantum well.

2. Theory

To understand the origin of valley splitting variability associated with random alloy disorder, we consider the following expression for the valley splitting, obtained from effective mass theory [3]:

$$E_v = 2\left|\int d^3r\, e^{-i2k_0 z} U_{\mathrm{qw}}(\vec{r}) \psi_{\mathrm{env}}{}^2(\vec{r})\right|, \quad (1)$$

where U_{qw} is the quantum well confinement potential, ψ_{env} is the wavefunction envelope, and $2k_0$ is the reciprocal lattice vector connecting the two z valleys within the first Brillouin zone. Equation (1) has the form of a Fourier transform of the overlap between the electron and the Ge concentration profile (proportional to U_{qw}), evaluated at the reciprocal lattice vector $2k_0$. As shown in Fig. 1(a), layer-by-layer fluctuations of the Ge concentration naturally have a wavevector component at $2k_0$, due to the small size of the quantum dot wavefunction, and the finite number of Ge atoms it is exposed to. In the talk, I will present tight-binding solutions of the valley splitting in a 3D crystal lattice, which incorporate SiGe random alloy disorder. The results show excellent qualitative and quantitative agreement with experimental measurements, and they confirm the role of alloy disorder in causing the observed variability of the valley splitting.

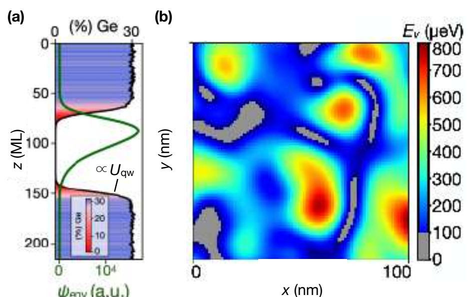

Fig. 1. Effect of SiGe random alloy on valley splitting. (a) Typical Ge concentration profile in a quantum well, averaged laterally over a quantum dot (black curve, ML stands for monolayers), and its corresponding envelope function (green curve). (b) Valley splitting results from tight-binding simulations, for a quantum well containing a nominally uniform 5% concentration of Ge. Variability arises from the alloy disorder.

3. Proposed Solution Strategies

To address the detrimental effects of alloy disorder, I will propose two strategies to ensure that valley splittings in quantum dots are consistently large enough for qubit applications.

3.1. Deterministic Strategy: The Wiggle Well

The complex phase term appearing in Eq. (1) is responsible for suppressing the valley splitting when the electron-Ge overlap is smooth. In this case, the integral expression quickly averages to zero. To overcome this problem, we propose to introduce Ge concentration oscillations into the quantum well, of the form $n_{\mathrm{Ge}} \sim \sin(2k_0 z)$, which has the effect of cancelling out the fast oscillations of the complex phase. Such an oscillating Ge concentration is referred to as a “Wiggle Well,” and has recently been explored theoretically and experimentally [1].

3.2. Disorder-Based Strategy: Uniform Ge in the QW

A second strategy for improving the valley splitting involves intentionally introducing a uniform concentration of Ge into the quantum well [2]. Figure

1(b) shows the results of tight-binding simulations of valley splitting, as a function of the quantum dot location, for a quantum well containing 5% Ge. In this case, the large electron-Ge overlap causes a significant enhancement of the mean valley splitting, as well as enhancing its variability. Here, the dangerously low values of the valley splitting ($E_v < 100$ μeV) are identified by gray color. To make use of the variability, we note that quantum dots can be repositioned laterally, by 20 nm or more in realistic devices [4]. By allowing such maneuverability, in Fig. 1(b), we see that it should always be possible to overcome the deleterious effects of alloy disorder.

Acknowledgements

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Reducing charge noise in quantum dots by using thin silicon quantum wells

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1. Introduction

Spin-qubits in silicon quantum dots are a promising platform for building a scalable quantum processor thanks to their small footprint, long coherence times, and compatibility with the advanced semiconductor manufacturing. However, electrical fluctuations due to charges and imperfections in the material stack can decrease gate fidelities. Therefore, reducing charge noise independently of the device location is pivotal to achieving the ubiquitous high-fidelity of quantum operations, within and across qubit tiles, necessary to execute more complex quantum algorithms and demonstrate larger quantum processors.

In this work, we demonstrate thin quantum wells in ^{28}Si/SiGe heterostructures with low and uniform charge noise, measured over several gate-defined quantum dot devices. By linking charge noise measurements to the scattering properties of the two-dimensional electron gas, we show that a quiet environment for quantum dots is obtained by improving the semiconductor/dielectric interface and the crystalline quality of the quantum well.

2. ^{28}Si/SiGe heterostructure

Figure 1a shows a bright field (BF) scanning transmission electron microscopy (STEM) image of the topmost layers of a ^{28}Si/SiGe heterostructure and the dielectric gate stack. We compare three different ^{28}Si/SiGe heterostructures (A, B, C) to improve, in sequence, the semiconductor/dielectric interface (from A to B) and the crystalline quality of the quantum well (from B to C).

Heterostructure A features a thin sacrificial Si cap grown at 675C. In Heterostructure B, we reduce the temperature to 500C, below the desorption temperature of chlorine from the surface, and expose the surface under the same conditions of DCS flow and pressure [1]. Fig. 1 b,c shows electron energy loss spectroscopy (EELS) semi-quantitative profiles across the semiconductor/ dielectric interface comparing the two processes. The growth of a sacrificial Si cap leaves residuals of unoxidized Si which are substituted in the low temperature process by a minor pile up of Ge at the semiconductor/dielectric interface.

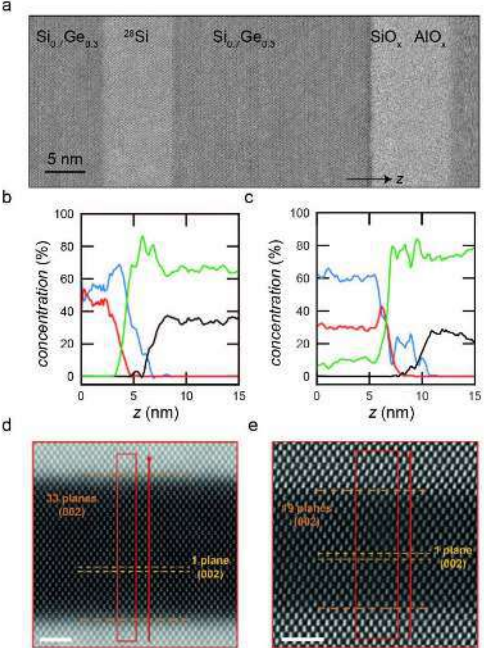

Fig. 1. **Structural characterization of the Si/SiGe heterostructure**. a, BF- STEM image of the active layers of a ^{28}Si/SiGe heterostructure field effect transistor showing, from left to right, the $Si_{0.7}Ge_{0.3}$ strained-relaxed buffer layer, the tensile strained ^{28}Si quantum well, the $Si_{0.7}Ge_{0.3}$ barrier, followed by the SiO_x/AlO_x dielectric stack. b - c, EELS semi-quantitative profiles across the semiconductor/ dielectric interface for Si (blue), Ge (red), O (green), and Al (black), taken on heterostructure A and B, respectively. d – e High resolution STEM images of the ^{28}Si quantum well of heterostructure B and C, respectively. We estimate the thickness of the quantum well by counting the (002) horizontal planes. The white scale corresponds to 2 nm.

In heterostructure C, we conserve the same amorphous Si-rich termination as in heterostructure B, and use a thinner ^{28}Si quantum well of ≃ 5 nm. This is nominally half of the thickness of the quantum well featured by heterostructures A and B (≃ 9 nm) and much thinner than the Matthews-Blakeslee critical thickness (≃ 10 nm). Figure 1 d,e shows high resolution STEM images of the two quantum wells. We estimate the thickness of the quantum well by

counting the (002) horizontal planes which are 5.3 ± 0.5 nm for heterostructure C and 9.0 ± 0.5 nm for heterostructure A and B.

3. Electrical and quantum dot performances

We evaluate the scattering properties measuring Hall-bar shaped field effect transistors (H-FETs) and charge noise in single layer quantum dot devices operated in accumulation mode. Figure 2 shows the distributions of multiple metrics resulting from the statistical characterization of multiple devices on the heterostructure A (red), B (blue), and C (green).

We use mobility at high density (μ) and percolation density (n_p) to benchmark the transport properties of the 2-Dimensional electron gas (2DEG). The results are shown in Fig 2 a,b. We see a steady increase in average mobility and a reduction in percolation density going from heterostructure A to B and C. Moreover, we demonstrate a decrease of almost a factor of ten in the spread of such metrics indicating a significant increase in uniformity on a wafer-scale.

In single layer quantum dot devices, we measure charge noise on a flank of a single electron transistor tuned in the Coulomb Blockade regime [2]. We use the power law frequency exponent α, the screening parameter β, and the minimum charge noise $S_\varepsilon^{1/2}{}_{min}$ to compare the different heterostructures.

We understand the charge noise trends in Figs. 3c–e by relating them to the evolution of the disorder landscape moving from heterostructures A to B and C. The narrow distribution of α in heterostructure A points to charge noise from many two-level-fluctuators (TLFs) possibly located at the low quality semiconductor/dielectric interface and above. Instead, the larger spread in α in heterostructures B and C implies that deviations from 1/f behavior become more frequent, possibly originating from a spatially non-uniform distribution of TLF. The decreasing trend in |β| indicates that heterostructures B and C are less sensitive to noise screening due to the addition of charges to the sensor, i.e., there is less noise to screen in the cleaner heterostructure. This assumption is confirmed directly by $S_\varepsilon^{1/2}{}_{min}$ in Fig. 2e, where we demonstrate a reduction of almost an order of magnitude of mean $S_\varepsilon^{1/2}{}_{min}$ going from A to C.

3. Conclusions

In summary, we have measured electron transport and charge noise in 28Si/SiGe heterostructures where we improve the semiconductor/dielectric interface, by adopting an amorphous Si-rich passivation, and the structural quality of the quantum well, by reducing the quantum thickness significantly below the Matthew-Blakeslee critical thickness for strain relaxation. We relate disorder in 2D to charge noise in quantum dots by following a statistical approach to measurements and quantify the reduction of remote impurities and dislocations nearby the quantum well.

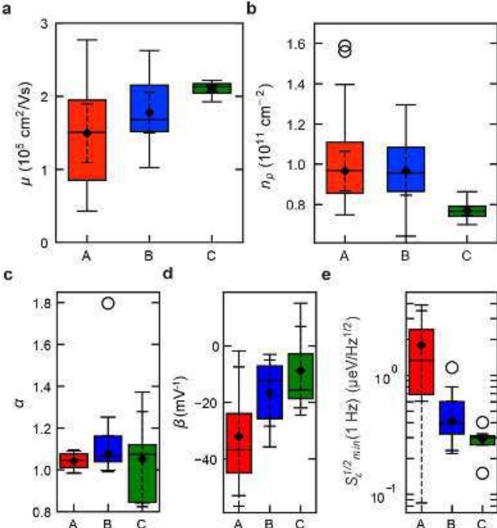

Fig. 2. **Distribution of transport properties and charge noise**. a - b Distributions of mobility (μ) measured at $n = 6 \times 10^{11}$ cm−2 and percolation density (n_P) for heterostructure A (red, 20 H-FETs measured), B (blue, 16 H-FETs measured), and C (green, 22 H-FETs measured). c - e Distributions of noise spectrum power law exponent α, coefficient β indicating the change in noise spectrum with increasing V_P, and minimum charge noise $S^{1/2}{}_{\epsilon,min}$ within the range of V_P investigated for heterostructure A (red, 4 devices measured), B (blue, 7 devices measured), and C (green, 5 devices measured). Quartile box plots, mode (horizontal line), means (diamonds), 99% confidence intervals of the mean (dashed whiskers), and outliers (circles) are shown.

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Epitaxy of group-IV semiconductors for quantum electronics

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1. Introduction

Epitaxy of group-IV semiconductors is a key enabler for quantum devices. Low temperature epitaxy can be used to deposit Si:B layers with boron concentrations so high that they are superconductive [1]. Tensily strained Si layers sandwiched between relaxed $Si_{0.7}Ge_{0.3}$ layers behave as quantum wells for electrons, enabling electron spin quantum bit (qubit) fabrication. Purified ^{28}Si without deleterious ^{29}Si isotopes (with a nuclear spin) are ideal as the core of fully-depleted, multiple gate transistors for qubits. Compressively-strained Ge layers sandwiched between relaxed $Si_{0.2}Ge_{0.8}$ layers can confine a two-dimensional hole gas (2DHG) offering an emerging pathway to hole-spin qubits. In the following, we will focus on the latter two subjects.

2. Results

2.1. epitaxy of ^{28}Si layers

We succeeded in growing ^{28}Si layers with the following concentrations: ^{28}Si isotopes > 99,992%, ^{29}Si isotopes < 0.006% and ^{30}Si isotopes < 0.002% [2]. Such values can instructively be compared to those in natural Si: ^{28}Si: 92.223%, ^{29}Si: 4.678% and ^{30}Si: 3.092% (**Fig. 1(a)**). The availability and cost of isotopically enriched $^{28}SiH_4$ is a major difficulty, however. We thus quantified the impact of growth temperature and HCl mass-flow on the Si growth rate (**Fig. 1(b)**). At high temperature, above 850°C, we reached a silane supply limited regime with a good decomposition efficiency, high growth rates (> 100 nm min.$^{-1}$ for the SiH_4 mass-flow selected) and almost no impact of the HCl flow. There was otherwise, below 850°C, a H- and Cl-surface desorption limited regime, with a lesser decomposition efficiency and Si growth rates which dropped as the temperature decreased and/or the HCl mass-flow increased. Thick ^{28}Si layers should be grown at high temperature (for instance for the production of ^{28}SOI substrates with a SmartCut™ approach). Meanwhile, low temperature epitaxy should be limited to the deposition of thin ^{28}Si layers on top of SiGe sacrificial layers (^{28}SOI fabrication with a bonding-etch back approach) or the thickening of SOI substrates (to avoid elastic or plastic relaxation/dewetting).

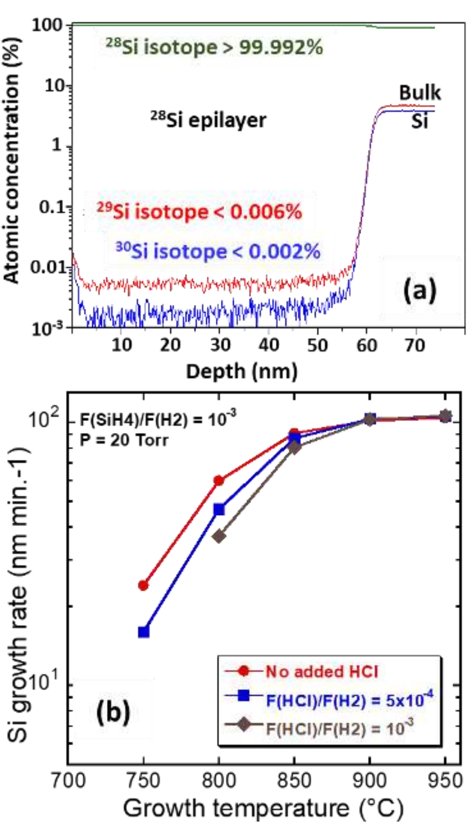

Figure 1 : (a) SIMS depth profiles of Si isotopes in a ^{28}Si epilayer; (b) Si growth rate function of the growth temperature and HCl flow for a given SiH_4 flow

2.2. c-Ge/SiGe heterostructures for hole spin qubits

We otherwise fabricated c-Ge/SiGe heterostructures for hole spin qubits. We first grew at 850°C, 20 Torr and with a SiH_2Cl_2 + GeH_4 chemistry, SiGe virtual substrates (VS), with a gradual ramping-up of the Ge concentration (to confine misfit dislocations) and a capping with 3 µm thick constant composition layers [3]. Reciprocal Space Maps around the (004) and (224) X-Ray Diffraction (XRD) orders gave us the Ge concentration in those SiGe caps (73.8% and 78.7%) and their macroscopic degrees of strain relaxation (102.0 and 102.5%). The surface cross-hatch, e.g. the regular array of undulations with a 1-2 µm spatial wavelength because

of a periodic strain field in VS, was suppressed using Chemical Mechanical Polishing (CMP). We then grew on top of the polished SiGe VS, at 500°C, 20 Torr and with a SiH_2Cl_2 + GeH_4 chemistry, {100 nm thick SiGe 74% or 79% / 16 nm thick compressively-strained Ge / variable thickness SiGe 74% or 79% overlayer / Si 2nm cap} stacks. The parameter that changed was the SiGe overlayer, with 22, 33, 44 or 55 nm thicknesses probed (**Fig. 2**).

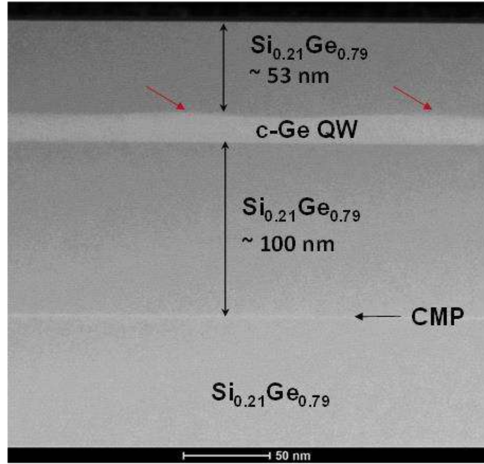

Figure 2 : SiGe/c-Ge/SiGe/Si cap stack grown at 500°C on a polished $Si_{0.21}Ge_{0.79}$ virtual substrate.

Compared to polished surfaces, a slight surface roughening was observed for the SiGe stacks, larger for the SiGe 74%/c-Ge than for 79%/c-Ge stacks. Thicker SiGe overlayers yielded smoother surfaces. We ascribed these surface undulations, with a ~ 100 nm wavelength, to a slight elastic relaxation of the compressive strain in the c-Ge layers. XRD showed that those stacks were pseudomorphic, with the same in-plane lattice parameter for the c-Ge layers than that of the SiGe VS underneath. Energy Dispersive X-ray spectroscopy (EDX) mapping of the whole structure showed that the Ge grading was rather linear with, as intended, a 10% Ge/µm grading (**Fig. 3(a)**). Cross-sectional Transmission Electron Microscopy (TEM) showed the presence of numerous misfit dislocations in the graded layer and none in the thick $Si_{0.21}Ge_{0.79}$ / c-Ge stack on top. A slight Ge concentration increase, by a few %, was measured by EDX at the CMP location, with a perfect crystallinity in the stack grown on top. The 16 nm thick c-Ge layer itself was perfectly monocrystalline, with a 1-2 bi-atomic layer roughness at c-Ge/SiGe interfaces, no in-plane deformation compared to the surrounding SiGe and an out-of-plane deformation of 1.5% from Precession Electron Diffraction (**Fig. 3(b)**).

Magnetotransport measurements in Hall-bar devices were performed at 4.2 K to assess the electrical properties of the 2DHG in the grown SiGe/c-Ge heterostructures. At low magnetic field, a hole mobility of 1.2 x 10^5 cm^2 V^{-1} s^{-1} was obtained for a hole density of n_{2DHG} = 3.7x10^{11} cm^{-2} in the c-Ge/SiGe 79% 55nm sample (**Fig. 4**), whereas quantum Hall effect plateaus and Shubnikov-De-Haas oscillations were observed at higher fields.

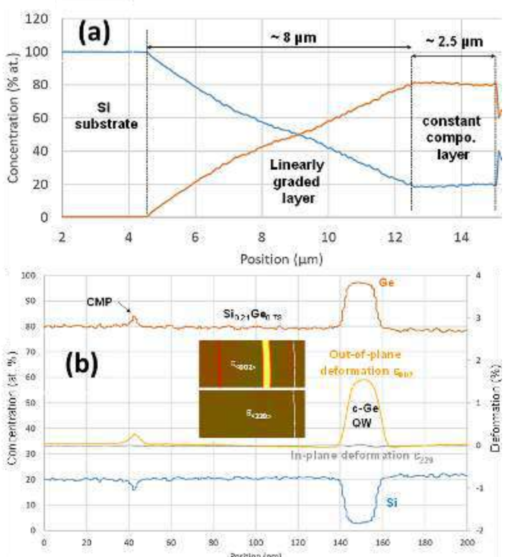

Figure 3 : (a) EDX profiles of the Ge and Si concentration in a $Si_{0.21}Ge_{0.79}$ VS; (b) Ge and Si concentration & deformation depth profiles in the 2DHG heterostructure grown on top.

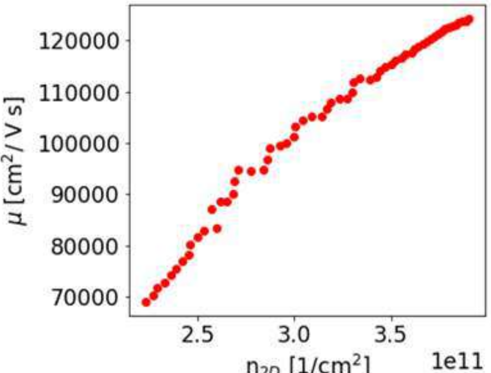

Figure 4 : hole mobility @ 4.2K function of the 2DHG sheet density.

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Growth and characterization of $Ge/Si_{1-x}Ge_x$ planar heterostructures for spin qubits applications

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1. Introduction

A great deal of interest is directed nowadays towards the development of innovative technologies in the field of quantum information and quantum computing, with emphasis in obtaining reliable qubits as the building blocks. The realization of highly stable, controllable and accessible hole spin qubits is strongly dependent on the quality of the materials hosting them. Ultra-clean germanium/silicon-germanium (Ge/SiGe) heterostructures in quantum wells (QWs) have been predicted and proven to be the perfect candidates and due to their large scalability potential, they are opening the door towards the development of realistic and reliable solid state, all-electric quantum computers.
The heteroepitaxial growth of SiGe layers having a high Ge content over Si wafers is challenging because of the large lattice mismatch between Si and Ge (~ 4.2%), which leads to the formation of misfit (MDs) and threading dislocations (TDs) [1]. Therefore, the heterostructure has to be engineered and optimized to reduce the defect density.
The use of chemical vapor deposition (CVD) allows the epitaxial growth of thin films with high structural quality and at elevated rates, compared to other techniques (e.g. molecular beam epitaxy, sputtering). The CVD growth conditions (temperature, pressure, flows, plasma power and growth time) influence dramatically the deposition rate and properties (mobility, crystallinity, interfaces quality) of the deposited layers. While this allows for a highly controllable process, the wide range of degrees of freedom makes it challenging and calls for a thoroughly optimization study.

2. Experimental

This work shows the results relative to the growth of epitaxial $Ge/Si_{1-x}Ge_x$ heterostructures for QW-based qubits, using a reverse grading approach. The CVD deposition kinetics and crystalline quality of the materials were investigated.

2.1. Growth kinetics

All the layers within this study were grown by CVD using a PlasmaPro 100 Nanofab and GeH_4 and SiH_4 as gaseous precursors. Fig. 1 shows the schematics of a complete $Ge/Si_{1-x}Ge_x$ QW heterostructure. A 2 µm virtual substrate (VS) consisting of a Ge thin film and a reverse graded alloy is deposited on a Si (100) wafer. The Ge film is grown using a two - temperatures step, for which a few nanometers layer deposited at low temperature (~ 400°C) is followed by a thicker high temperature (~ 550°C) one. For the graded $Si_{1-x}Ge_x$ alloy, the Ge molar fraction x is linearly decreased from 1 to 0.8 - 0.95 and the grading rate is kept below 10%/µm to avoid the generation of new dislocations. The QW stack, deposited over the VS, consists of two SiGe alloys having fixed Ge and Si molar fractions, in a range 0.8 - 0.95 Ge and 0.2 - 0.05 Si, enclosing a Ge QW. The thickness of the bottom SiGe barrier is ~ 300 nm, while the Ge QW and the top SiGe barrier are in a range 5 - 15 nm and 5 - 65 nm respectively. A thin Si protective cap completes the heterostructure. The control of the thickness of pure Ge layers and of the composition of $Si_{1-x}Ge_x$ alloys is crucial for the QW stack and the virtual substrate layers, allowing to obtain clean and dislocation-free heterostructures, with the possibility to tune the strain in the QW influencing the hole mobility and the spin-orbit splitting. Fig. 2 shows the dependence of the Ge thin films growth rate on temperature and partial pressure of the precursor gas. The growth rate increases with increasing temperature and pressure, which is explained by the thermal activation of the dissociative adsorption of

Fig. 1. Schematics of a planar Ge/SiGe heterostructure.

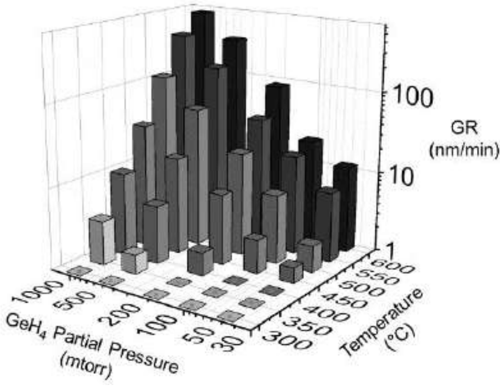

Fig. 2. Growth rate of epitaxial germanium layers.

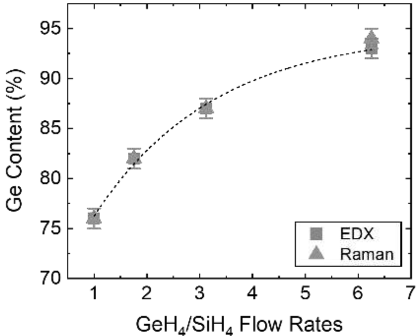

Fig. 3. Composition vs precursor flow rate in SiGe alloys.

GeH_4 and the larger imping rate at higher pressures according to Graham's law. The influence of different dilution gases is being investigated. The dependence of the Si and Ge molar ratios on the precursor gases flow rates is shown in Fig. 3. EDX analysis and Raman spectroscopy were used to calibrate the growth conditions of the alloy.

2.2. Ge/Si$_{1-x}$Ge$_x$ heterostructures

Heterostructures with 5-15 nm Ge QWs, 5-65 nm SiGe top barriers and SiGe alloys with 80-95% Ge content were grown and characterized to assess their morphological and crystalline quality. Fig. 4(a)-(b) show a Scanning Transmission Electron Microscopy (STEM) cross-section image of a heterostructure with 300 nm and 55 nm $Si_{0.2}Ge_{0.8}$ bottom and top barriers, respectively, and 14 nm Ge QW. Dislocations are confined within the Ge VS and the first tens of nanometers of the graded SiGe alloy, away from the QW region. Through a selective chemical etching, an upper limit for the TD density is found to be 8.1×10^8 cm^{-2}. Figure 4(c)-(d) show a High Resolution – Transmission Electron Microscopy (HR-TEM) image of the QW region and a Selected Area Electron

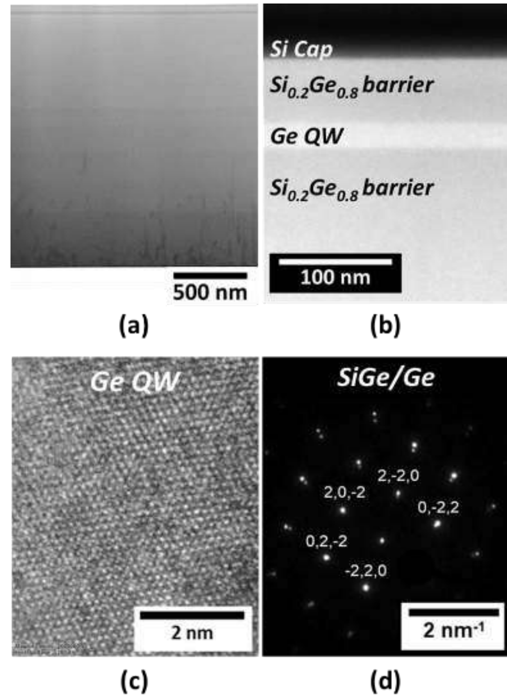

Fig. 4. (a) - (b) STEM of the whole heterostructure and zoom on the QW region. (c) HR-TEM of the Ge QW. (d) SAED at the interface between SiGe barrier and Ge QW.

Diffraction (SAED) pattern taken at the interface between the bottom SiGe barrier and the Ge QW. Both characterizations confirm the crystallinity of the grown films. From SAED, it was possible to extract the in-plane residual strain for the QW, $\varepsilon_{\parallel} = 0.3\%$.

3. Conclusions

The growth kinetics of Ge and SiGe thin films was investigated to successfully achieve the growth of planar and epitaxial Ge/Si$_{1-x}$ Ge$_x$ heterostructures. The morphological and crystalline quality of the material were assessed and the degrees of freedom of the layout were explored to obtain the best configuration for spin qubits applications. Future efforts will be devoted to further improve the quality of the material and to develop new structural layouts.

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Optical Fingerprint of Subnanometer Interfacial Broadening in SiGe/Si Superlattices

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1. Introduction

Interfaces are ubiquitous in semiconductor low-dimensional systems used in electronics, photonics, and quantum computing. Based on a recent method to map in $3D$ and the atomic level the roughness and uniformity of buried epitaxial interfaces in SiGe/Si superlattices (SLs) with a layer thickness in the 1.5-$7.5\,\mathrm{nm}$ range, we address the optical properties of these SLs using room temperature spectroscopic ellipsometry.

SiGe/Si superlattices (SL) can indeed be used as the core of multi channel field effect transistors with superior $I_{\mathrm{on}}/I_{\mathrm{off}}$ tradeoffs thanks to the stacking of channels one upon the other [1]. This recent progress generates a great deal of interest in ultrathin group IV SLs as building blocks for future CMOS technologies. Moreover, the artificial periodicity in these low-dimensional systems provides an additional degree of freedom to engineer their band structure and thus improve their electronic and optical properties.

Understanding their atomic-level properties has thus been crucial to controlling the basic behavior of heterostructures and optimizing the device performance. Herein, systematic studies revealed a new SL-related optical transition between 2.1 and 2.5 eV. we demonstrate that subnanometer interfacial broadening in heterostructures induces localized energy states. This phenomenon is predicted within a theory incorporating atomic-level interfacial details obtained by atom probe tomography (APT). The experimental validation is achieved using heteroepitaxial $(\mathrm{Si}_{1-x}\mathrm{Ge}_x)_m/(\mathrm{Si})_m$ SLs as a model system demonstrating the existence of additional paths for holeelectron recombination. These predicted interfacial electronic transitions and the associated absorptive effects are evaluated at variable superlattice thickness and periodicity. By mapping the energy of the critical points, the optical transitions are identified, thus extending the optical absorption to lower energies [2]. This phenomenon is shown to provide an optical fingerprint for a straightforward and nondestructive probe of the subnanometer broadening in heterostructures.

2. Results and Discussion

2.1. Experimental and theoretical methodology

Using SiGe/Si as a model system, Figure 1a illustrates the basic band-to-band absorption for a type-I SiGe/Si quantum well (QW) along with the localized energy levels induced in the band structure at the interface. To evaluate the hypothesized interface-related changes in the band structure, a framework was implemented to quantitatively include the absorptive effects of buried interfaces. The band structure and the electron and hole wave functions are calculated within the 14-band $k{\cdot}p$ formalism, where the microscopic effect of the interface is accounted for through the interface asymmetry Hamiltonian (H_{IF}) [3]. Figure 1b displays the calculated absorption coefficient (α in cm^1) for a $\mathrm{Si}_{0.71}\mathrm{Ge}_{0.29}$/Si QW at different interface values between 0 and $0.32\,\mathrm{nm}$.

To evaluate the theoretical findings experimentally, a series of ultrashort SiGe/Si SLs were epitaxially grown on a 300 mm undoped Si(001) substrate at a Ge content of below 30% in a RPCVD reactor. Four $(\mathrm{Si}_{1-x}\mathrm{Ge}_x)_m/(\mathrm{Si})_m$ SLs with different periodicity (m = 3, 6, 12, or 16) were investigated, as shown in Fig.1c. Next, the corresponding absorption coefficient was measured with spectroscopic ellipsometry, as shown in Fig.1d.

2.2. Optical Fingerprint of Interface Broadening

To enhance the interfacial broadening, SLs were subjected to rapid thermal annealing in the 780 to $950°\mathrm{C}$ temperature range under flowing N_2 ambient gas for 50 s. Figure 1e displays the $2\theta-\omega$ high-resolution X-ray diffraction (HRXRD) scans around the (004) diffraction order of the as-grown (blue) and annealed (red) S_3 SL. The corresponding $d^2\varepsilon_2/d\omega^2$ around the $E_{4\tau}$ critical point (CP) transition are exhibited in Fig. 1f. The vertical blue and red lines represent the $E_{4\tau}$ CP peak position for the as-grown and annealed SL,

respectively. Interestingly, the transition energy shift $\Delta E_{4\tau}(= E_{4\tau}^{300°C} - E_{4\tau}^{T})$ increases as a function of the annealing temperature from $10\,\mathrm{meV}$ at 780°C to $33\,\mathrm{meV}$ at 950°C. This redshift agrees well with the predicted theoretical results shown in Fig. 1b.

3. Conclusion

In summary, atomic-level interfacial broadening was found to create localized energy states in heterostructures. This phenomenon was initially predicted through a rigorous theoretical formalism providing a qualitative and quantitative description of the absorption coefficient α in presence of smeared-out interfaces. The experimental measurements of CP provided a direct evidence of this behavior and identified the associated optical transitions between 2 and $2.5\,\mathrm{eV}$. Furthermore, thermal annealing-induced interfacial broadening confirmed that these transitions are interface-induced.

Acknowledgment

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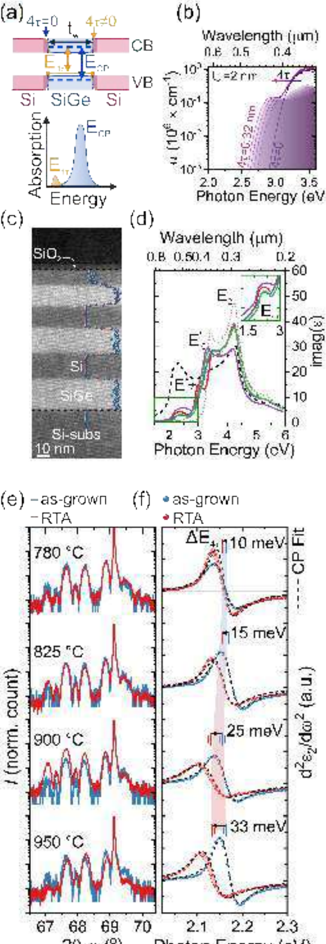

Figure 1. (a) Schematic representation of a SiGe/Si QW with (orange) and without (blue) the effect of interfaces broadening. The critical point optical transitions (E_{CP}), as well as the interface-related transition ($E_{4\tau}$) are shown, in conjunction with a schematic of the resulting absorption coefficient. (b) Next, the 14-band $k \cdot p$ absorption coefficient (α) of the QW with a variable interfacial broadening 4τ from 0 to $0.32\,\mathrm{nm}$ with a $0.1\,\mathrm{nm}$ step. (c) HAADF-STEM image of the $(Si_{0.71}Ge_{0.29})_3/(Si)_3$ SL overlaid with the concentration profile of Ge extracted from the corresponding APT $3D$ reconstruction. (d) The imaginary (ε_2) part of the complex dielectric function of the four $(Si_{1-x}Ge_x)_m/(Si)_m$ SLs with increasing periodicity $m(= 3, 6, 12, 16)$ are presented. (e) XRD $\omega - 2\theta$ scans around the (004) diffraction order of the as-grown (blue) and annealed (red) S_3 SL. (f) The interfacial broadening CP energy shift $\Delta E_{4\tau}$ was analyzed as a function of the annealing temperature.

X-ray Nanobeam Mapping of Lattice Strain Modulations caused by CMOS-Processed Gate Electrodes for Quantum Technologies

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1. Introduction

The quantitative characterization and control of elastic lattice strain over sub-micron length scales is essential in the development of semiconductor quantum devices. Such devices can be based on Si/SiGe heterostructures, which are a material platform for spin qubits that has evolved in recent years by the demonstration of high coherence times and multi-qubit algorithms. [1,2] In this technology platform, single electrons are housed in electrostatic quantum dots (QDs) in strained Si quantum well (QW) layers of < 10 nm thickness sandwiched between plastically relaxed SiGe buffer layers on a Si substrate. [3] Recently, we demonstrated that strain exerted from metallic electrodes significantly affects the band energy levels of gate-defined quantum dots in SiGe heterostructures, which is of particular importance in the context of establishing communication pathways between qubits. [4] Such connections may be achieved by coherent shuttling of electrons with the quantum bus (QuBus) architecture, shown in **Fig.1a**, through adiabatic motion of a QD by sets of claviature gate electrodes. [5] An investigation of the strain landscape around the electrodes for the shuttling requires a technique combining fine strain sensitivity with nanoscale spatial resolution. Our method of choice for this study is Scanning Xray Diffraction Microscopy (SXDM), [6] performed at the nanodiffraction beamline ID01/ESRF, to map non-destructively the lattice strain tensor around several sets of CMOS-processed Titanium Nitride (TiN) gate electrodes.

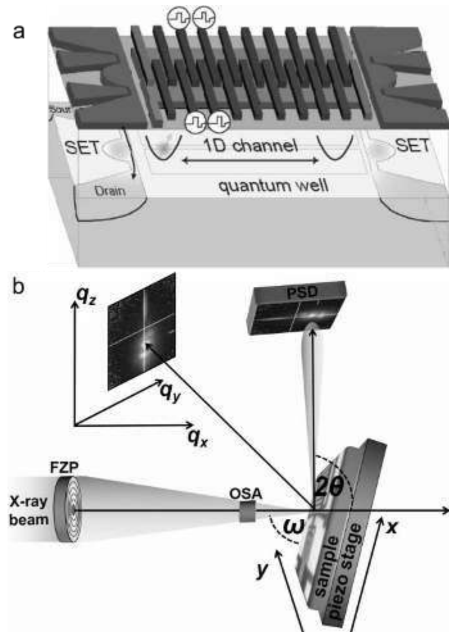

Figure 1. **(a)** *Schematic of a QuBus electron shuttling device.* [7] **(b)** *Experimental setup for X-ray nanobeam strain mapping by SXDM at ID01/ESRF.*

2. Results

We utilize the experimental setup depicted in **Fig. 1b** to record spatially resolved X-ray diffraction maps around sets of TiN electrodes for multiple Bragg reflections of the {335} family from a 10 nm thick Si QW layer in a $Si/Si_{0.7}Ge_{0.3}$ heterostructure. Linear combination of several Bragg reflections allows us to extract the individual components of the strain tensor ε_{ij} at each spot. [6] By simultaneously detecting the fluorescence from the Ti K-edge, we are able to observe and track the shape of the device during measurement, as shown in **Fig. 2a**. Our experiment benefits from the recent extremely bright source (EBS) upgrade to the ESRF, enabling a mapping of the Si lattice constants with a lateral resolution of approximately 50 nm. Maps of the ε_{xx}, ε_{zz} and ε_{xz} strain components are calculated from the lattice constants, shown in **Fig. 2b-d.** For all components, we observe local modulations larger than $\Delta\varepsilon_{ij} > 4 \cdot 10^{-4}$, which are linked to stress exerted from

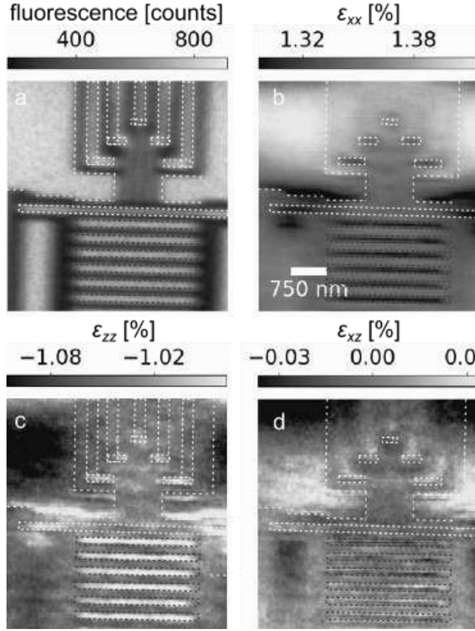

Figure 2. Maps of Ti K-edge fluorescence **(a)**, *the strain tensor components* ε_{XX} **(b)**; ε_{ZZ} **(c)**; ε_{XZ} **(d)**. *The electrodes are outlined bv the dotted lines.*

the TiN electrodes onto the Si layer by comparing strain and fluorescence maps.

Based on the experimental data, we determine the mechanical stress within the TiN, allowing us to generate a Finite Element Method (FEM) model to reproduce the strain distribution within the sample, shown for a line profile of ε_{xx} across six electrodes in **Fig. 3.** From this model, we extrapolate the strain profile across the claviature electrodes at the qubit operation temperature T = 20 mK and translate them into local modulations of the Si conduction band energy level by bandstructure calculation. This energy level variation is found to be larger than +/- 1.5 meV, and therefore of a similar magnitude as the charging energy of electrostatic QDs.[8]

3. Conclusions

From SXDM measurements with an X-ray nanobeam, we observe local modulations of the symmetric and shear components of the strain tensor with a magnitude of several 10^{-4}, which are verified to stem from the stressing action of TiN gate electrodes Moreover, we compare sets of electrodes deposited with different process conditions, and find a scaling of microscopic strain with macroscopic stress. Band structure calculations predict that the resulting fluctuations in the band energy level are strong enough to affect coherent electron shuttling in electrostatic QDs, especially at cryogenic temperatures.

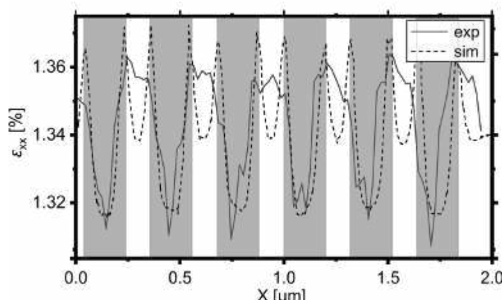

Figure 3. Experimental and simulated ε_{xx} *strain profile across six claviature electrodes, the extent of the electrodes is shaded in grey.*

Thus, we demonstrate that the effect of TiN electrodes on the lattice strain must be taken into account in the optimization and design architecture for CMOS-compatible quantum computing scaled towards extended arrays for error correction schemes.

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Isotope- and strain-engineered germanium quantum wells

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1. Introduction

Hole-based solid-state devices made of group IV semiconductors are now increasingly explored as reliable architectures for quantum processors and memories.[1] The inherently large and tunable spin-orbit coupling (SOC) of holes and their reduced hyperfine coupling with nuclear spins, is essential to establish scalable spin qubits. To this end, confinement of heavy-holes (HHs) in Ge/SiGe quantum well (QW) heterostructures has been extensively studied as a promising solution to develop scalable quantum processors on Si. Despite the reduced hyperfine interaction, the residual nuclear spin bath still perturbates the HH spin qubit behavior.[2] Developing nuclear spin-depleted QWs would thus shed light on the sensitivity of Ge qubits to hyperfine interactions, while decoupling the role of charge noise on the dephasing process. Isotopically engineered QW heterostructures that are depleted from ^{73}Ge, which is the only Ge nuclear spin-full stable isotope, would open new avenues in the fabrication of scalable, robust Ge qubits. With this perspective, herein we demonstrate the epitaxial growth of isotopically purified ^{70}Ge QW using a chemical vapor deposition (CVD) reactor.

While a high degree of control over the HH states can now be routinely achieved, similar behavior using light holes (LH) states has been out of reach for decades due to the absence of suitable materials that could provide the required valence band character and its energy offsets. The precise engineering of LH states remains a serious obstacle toward coherent optical photon-spin interfaces needed for a direct mapping of the quantum information encoded in photon flying qubits to stationary spin processors.[3] In this work, we propose an all-group-IV semiconductor low-dimensional system, consisting of a highly tensile strained Ge QW with GeSn as barriers, grown on Si. [4-5] The ability to engineer LH states in group-IV semiconductors enables a unique Si-integrated platform combining the Ge large SOC, the hole quiet quantum environment, and the spin 1/2 of LH, in addition to the tunable bandgap directness and energy in strain-engineered Ge and GeSn. These properties create valuable opportunities to implement new scalable quantum devices and potentially integrate qubits, spin coherent photodetectors, and quantum emitters on the same Si chip.

2. Methods

The epitaxial growth of Ge/SiGe and Ge/GeSn QW heterostructures was carried out in a reduced-pressure chemical CVD on a 4-inch (100) Si wafer. Ultrapure H_2 was used as a carrier gas, while 2% disilane (Si_2H_6), 10% monogermane (GeH_4), and tin-tetrachloride ($SnCl_4$) were selected as precursors for the Si, Ge, and Sn atoms, respectively. Isotopically purified monogermane ($^{70}GeH_4$) with an isotopic purity higher than 99.9 %, and isotopically purified monosilane ($^{28}SiH_4$) with an isotopic purity higher than 99.99 %, were used for the growth isotopically-engineered QWs. The isotopic content and chemical composition of the QW heterostructure was investigated by time-of-flight secondary ion mass spectrometry (ToF-SIMS) and atom probe tomography (APT). Band structure calculations were performed with a eight-band k·p theory for the derivation of an effective Hamiltonian for the 2D LH gas incorporating the Bir-Pikus Hamiltonian and thus the effects of biaxial strain.

3. Results and Discussion

3.1. Isotopically-engineered HH-based QW

First a 2.5 µm-thick Ge virtual substrate on Si (Ge-VS/Si) was grown at 600 °C, followed by thermal cyclic annealing >800 °C and then a 1.4 µm-thick, reverse-graded $Si_{0.18}Ge_{0.82}$ layer was grown at 600 °C. Without interrupting the growth, the precursor supply is then switched to $^{70}GeH_4$ for the growth of the $Si_{0.15}{}^{70}Ge_{0.85}$ barrier (BR1). The growth was then interrupted for 90 s prior to the compressively-strained ^{70}Ge QW layer growth. The same growth interruption was performed before the growth of the second $Si_{0.15}{}^{70}Ge_{0.85}$ barrier (BR2). Lastly, a thin Si capping layer was deposited. The $^{70}Ge/Si_{0.15}{}^{70}Ge_{0.85}$ QW is visible in the scanning transmission electron micrograph (STEM) and APT measurements in Fig. 1a, with thicknesses of 290/18/28 nm. Interface widths of 1.5-2.0 nm were obtained, with an excess Si content (>20 at.%) that was observed in the proximity of both BR1-2 interfaces with the ^{70}Ge QW. ToF-

SIMS analysis (Fig. 1b) shows the high ^{70}Ge purity, with a ^{70}Ge/^{76}Ge intensity ratio of 99.98% in the BR1, 99.97% in the ^{70}Ge QW, and 99.94% in the BR2. Similar levels of purities are obtained when using the intensity ratios for other Ge isotopes. A reduction in the ^{70}Ge purity was estimated at the BR1-2 interfaces with the ^{70}Ge QW. Oxygen contamination was only detected near the surface of the sample.

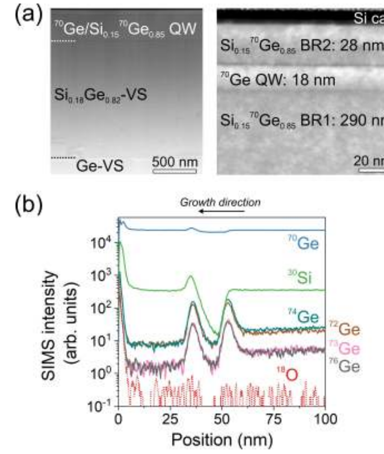

Fig. 1. (a) STEM image of the ^{70}Ge/Si$_{0.15}$^{70}Ge$_{0.85}$ QW. (b) ToF-SIMS profile for the Ge isotopes acquired in the upper QW region of the heterostructure. Unpublished data.

3.2. *LH-based QW*

The Ge/GeSn low-dimensional system allows to control LH-HH coupling and hence the hole states, where the LH selective confinement is obtained at a biaxial tensile strain exceeding 1 %.[4] The growth of the tensile-strained Ge QW was performed at 320 °C on a multi-layered GeSn buffered heterostructure on Ge-VS, with Sn contents up to 14.6 at.% in the upper BR1-2 layers (Fig. 2c-d).[5] Control of the Sn content was achieved through a gradual reduction of the growth temperature from 350 to 310 °C. This protocol relaxes the compressive strain in the growing GeSn layers while simultaneously enhancing the Sn incorporation, resulting in a Ge QW region with high crystallinity. Interfacial width of ~0.8 nm was achieved for both QW interfaces when measured in APT. Fourier transform infrared spectroscopy (FTIR-SE) was coupled with spectroscopic ellipsometry (IRSE) to demonstrate the presence of quantum confinement in the LH QW. The nature of the critical points (CPs) changes into an excitonic line shape in the QW. The CP broadening decrease with increasing tensile strain, with a simultaneous increase in the CP energy. Moreover, the CP energy increases with decreasing QW thickness. All together, these observations clearly show LH confinement in the Ge/GeSn QW.

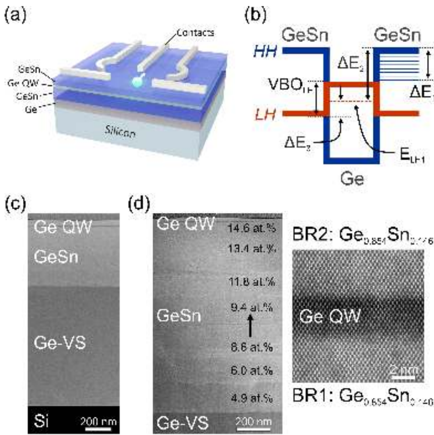

Fig. 2. LH-based Ge QW grown on a Si substrate using GeSn as barriers. Adapted from Ref. [5].

4. Conclusions

An isotopically purified, compressively-strained ^{70}Ge/Si^{70}Ge HH QW heterostructure grown with CVD and with >99.9% ^{70}Ge purity was demonstrated. Ongoing efforts aim at improving the sharpness of the ^{70}Ge-Si^{70}Ge interfaces and removing ^{29}Si nuclear spins by supplying isotopically purified ^{28}Si instead of ^{nat}Si during growth. Optimization of the growth process is underway to achieve sharper QW interfaces and improve the performance of the resulting HH-based spin qubit devices. A LH QW grown on a Si wafer was demonstrated using a highly tensile strained Ge on relaxed, composition step-graded GeSn buffers. High crystalline quality with sub-nanometer interfacial broadening was enabled by the low-temperature, multilayer buffered growth. LH confinement was achieved by increasing the tensile strain above 1 %. Moreover, the QW excitonic optical transitions were identified and their energy modulated and extended in the mid-wave infrared range by controlling strain and thickness.

Acknowledgements

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Heterogeneous-integrated CFETs Realized by Layer Transfer Technology

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1. Introduction

Novel CMOS architectures such as nanosheet FETs, forksheet FETs, and Complementary FETs (CFETs) have been proposed to replace Si FinFETs for better performance and lower power consumption. Among them, CFETs with vertically stacked nFET/pFET channel structure can effectively shrink down the layout area in conjunction with excellent DC performance [1]. Therefore, CFETs have been considered as the ultimate CMOS architecture for beyond N2 technology. However, CFETs suffer from n/p FET balance issues [2] due to the restriction on the same channel layout. As shown in Table I, different materials and different surface orientations have great impacts on the electron and hole mobility in the channel. Therefore, to enhance the channel mobility and to balance the n/p performance, we developed heterogeneous-integrated CFETs structures utilizing the layer transfer technology [7,8].

Orientation/ mobility (cm^2/Vs)	$\mu_{e,Si}$	$\mu_{h,Si}$	$\mu_{e,Ge}$	$\mu_{h,Ge}$
<100>	350[3]	75[3]	730[4]	437[6]
<110>	230[3]	180[3]	926[5]	526[6]
<111>	300[3]	120[3]	1100[4]	345[6]

Table I. Si and Ge carrier mobility for different surface orientations extracted by split *C-V*.

2. Low temperature hetero-layer bonding technology for 8-inch wafer

To realize the multi-layer stacked nanosheet hetero-structure for CFETs, we developed a new layer transfer technology called Low Temperature Hetero-Layers Bonding Technique (LT-HBT) for 8-inch wafer (Fig. 1). As the donor wafer for the top Ge channel, Ge epitaxial layer is grown on an 8-inch SOI wafer by reduced pressure chemical vapor deposition (RPCVD). Before direct wafer bonding, SOI host wafer for the bottom Si channel was implanted with As, making the junction-less Si nFET. ALD SiO_2 on Ge epitaxial layer and thermal oxidized SiO_2 on SOI were formed as a bonding oxide. After the surface activation by wet chemical treatments, the direct bonding was performed at room temperature in the press machine. The infrared (IR) image shown in Fig. 1(a) indicates that the bonding interface is free of voids and defects after direct wafer bonding. Then, the SOI donor substrate was thinned down to 50~100-μm-thick by the back grinding process (Fig. 1(b)). Subsequently, deep RIE was used to remove the remaining Si of SOI substrate, where BOX layer would serve as an etch-stop layer. Finally, BOX layer and thin SOI layer would remove selectively by HF and TMAH solutions afterward. As shown in Fig. 1(c), the 8-inch Ge/Si hetero-layer wafer with Ge/Si nanosheets can be successfully fabricated through LT-HBT.

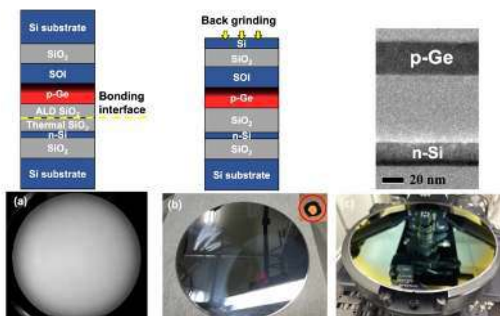

Fig. 1. Process flow of Low Temperature Hetero-Layers Bonding Technique (LT-HBT) for fabricating 8-inch Ge/Si hetero-layer wafer. (a) The IR image after the direct wafer bonding. (b) The photograph of 8-inch Ge/Si hetero-integrated wafer after Si back grinding process. (c) The photograph of 8-inch Ge/Si hetero-integrated wafer after Ge exposure.

The thermal stability of the bonding strength is the crucial parameter in LT-HBT. To ensure the fabricated hetero-structures can sustain the thermal budget of CFET fabrication process afterward, we investigated the temperature dependence of the bonding strength

with different bonding oxides. Fig. 2 shows the comparison of bonding strength of ALD SiO_2/ALD SiO_2 and ALD SiO_2/thermal oxidized SiO_2 bonding interface with and without wet activation. Wet activation can effectively enhance the thermal stability of ALD SiO_2/ALD SiO_2 bonding interface. On the other hand, the strong bonding strength can achieve even for 200 °C annealing for ALD SiO_2/thermal SiO_2 bonding interface with the wet activation. Since the different heat expansion coefficients for Ge and Si would lead to large thermal stress during the 8-inch bonding process, we chose ALD SiO_2 and thermal oxidized SiO_2 as a bonding oxide.

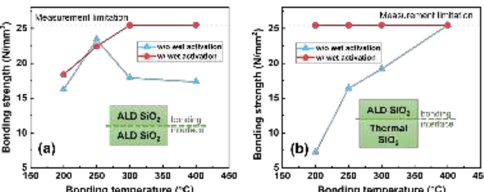

Fig. 2. The comparison of the temperature dependence of the bonding strength of (a) ALD SiO_2/ALD SiO_2 and (b) ALD SiO_2/thermal SiO_2 bonding interfaces with and without wet activation.

3. Heterogeneous-integrated CFET structure

Using the Ge/Si hetero-layer wafer, the heterogeneous-integrated CFET structures were fabricated. The cross-sectional channel structure with high κ metal gate (HKMG) in heterogeneous-integrated CFETs was analyzed by TEM and EDS as shown in Fig. 3. The Ge gate all around (GAA) channel structure is well covered by conformal Al_2O_3 and TiN. We found that the Ge/Si hetero-structure fabricated by LT-HBT can sustain various thermal and wet processes in CFET fabrication.

LT-HBT is also applicable to realize the stacked channels with different surface orientations. We demonstrated heterogeneous-oriented CFETs, consisting of Ge(111) nFET/ Ge(100) pFET, which orientations offer the highest electron and hole mobility, respectively. Fig. 4 shows the TEM cross-sectional image of the hetero-orientation Ge CFET, showing the fully suspended Ge (111) channel. To investigate the crystal orientation in size below 10 nm, we implemented CBED analysis. The clear diffraction discs in CBED pattern from Ge (111) and Ge (100) nanosheet channels indicates the successful integration with the hetero-orientation Ge channel through LT-HBT.

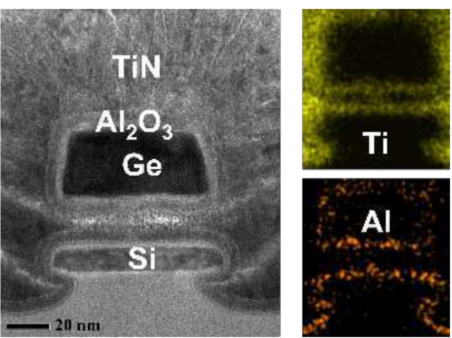

Fig. 3. Cross-sectional TEM image of Ge/Si hetero-structure after HKMG process and the corresponding EDS mapping results of Ti and Al.

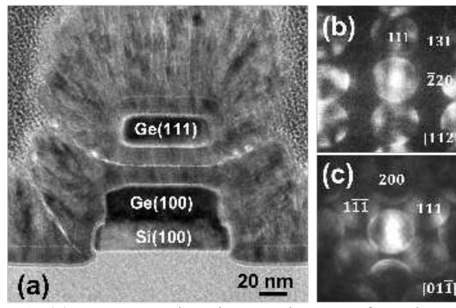

Fig. 4. (a) Cross-sectional TEM image of Ge hetero-orientation structure after HKMG and the CBED patterns of (b) Ge (111) and (c) Ge (100).

4. Conclusions

We demonstrated heterogeneous-integrated CFETs using the hetero-layer wafer realized by LT-HBT. By optimizing not only different channel materials but also different channel orientations, new dimension for CFETs can be explored.

Acknowledgements

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Electron Tomography Analysis of Ge/SiGe Asymmetrically Coupled Quantum Wells

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1. Introduction

We present an electron tomography (ET) method for the three-dimensional (3D) characterization of interfaces in a Ge/SiGe asymmetrically coupled quantum well (ACQW) structure. Real semiconductor interfaces mostly do not match the ideal of a smooth and chemically abrupt boundary and can be described with a parametric set. Here we determine quantitative values for the interface width as a measure of chemical intermixing and for the morphological roughness, the root mean square (rms) σ_{rms} of the interface position plus a lateral correlation length $\xi_{\|}$. These quantities can be used in the device engineering process to fine-tune (opto)electronic properties. The advantage of this method is the simultaneous determination of the quantities for buried interfaces and the same specimen site, additionally, avoiding the projection problem of conventional transmission electron microscopy (TEM).

2. Material and Methods

The sample is grown by ultrahigh-vacuum chemical vapour deposition on a Si(001) substrate. A stack of 20 Ge/$Si_{0.2}Ge_{0.8}$ ACQWs modules is deposited on a Si-Ge reversed-graded virtual substrate tuned for strain compensation in the stack. A module, cf. Fig. 1(a), has the following Ge/**$Si_{0.2}Ge_{0.8}$** thickness sequence in nanometers: 5/**2.3**/12/**20**. For more growth details see Ref. [1].

For the tomographic examination, an about 200-nm-thick needle, see Fig. 1(b), is prepared with focused Ga^{+}-ion beam milling with its longitudinal axis coinciding with the direction of growth [2]. We examined the four uppermost modules with ET.

In ET, a 3D image or tomogram of the sample is reconstructed from a series of two-dimensional (2D) projections from different viewing angles [3]. We use high-angle annular dark-field (HAADF) scanning (S)TEM images as projections that show a chemically sensitive contrast, making the Ge and SiGe layers distinguishable, cf. Fig. 1(a). Using a Cs-corrected JEOL ARM 200F microscope, operated at 200 kV, 86 projections of the target volume are taken. For this, the needle is rotated in 2° steps in a range of 170° around its longitudinal axis. The projections are then digitally aligned before the tomogram is reconstructed (a 3D data set of voxels) using a simultaneous iterative reconstruction technique algorithm [4] and tomogram artefacts caused by non-linearities of the HAADF contrast are corrected with an approach described in [5].

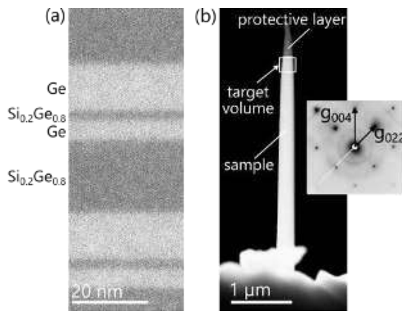
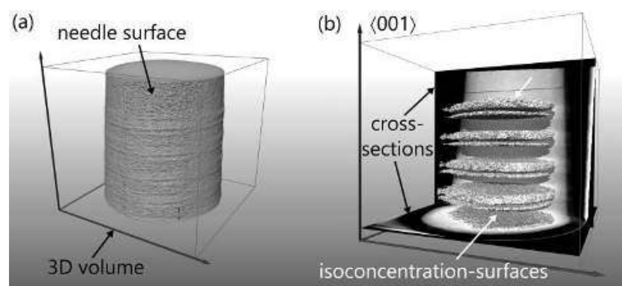


Fig. 1 (a) Conventional HAADF STEM image of two ACQW modules from a lamella. (b) For ET prepared needle of the sample with longitudinal axis in [001] direction, see diffraction pattern on the right.

3. Results

The data from the tomogram can be analysed and visualised in various ways. For example, Fig. 2(a) shows the reconstructed needle surface highlighting the 3D shape and the surface relief. The internal interfaces are visualized using iso-concentration surfaces extracted from the 3D reconstruction at a fixed voxel intensity of 90 at% Ge, i.e., at the value in the middle between 80 and 100 at% Ge of the adjacent layers. Figure 2(b) shows the corresponding iso-surfaces of the Ge/SiGe and SiGe/Ge interfaces of the top four complete ACQWs. For further quantitative analysis, these iso-surfaces are rasterized into topographic height maps [2] (see inset in Fig. 2(c)) and the one-dimensional height-height



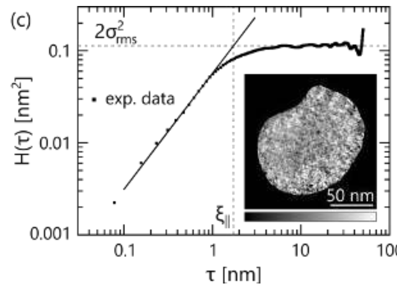


Fig. 2 (a) The reconstructed 3D volume with rendered needle surface. (b) Isoconcentration-surfaces at 90 at% Ge (two marked by an arrow) representing the Ge/SiGe and SiGe/Ge interfaces and 2D cross-sections of 1-voxel thickness (0.488 nm). (c) Example of a 1D HHCF calculated from the topographic height map in the inset. The scalebar of the map ranges from −1.00 to 1.00 nm.

correlation function (1D HHCF) can be calculated for each interface (Fig. 2(c)). The HHCF describes the average height difference z between two interface points separated by a distance τ [6]:

$$H(\tau) = \langle (z(x+\tau) - z(x))^2 \rangle. \quad (1)$$

Assuming a Gaussian distribution of heights and a limited self-affinity, σ_{rms} and $\xi_{||}$ are obtained as graphically indicated in Fig. 2(c): The rms roughness σ_{rms} is derived from the saturation level at large τ and the correlation length $\xi_{||}$ as the intersection of the linear fit at small τ with the saturation level. Our results reveal that all 16 interfaces are very smooth with a mean rms roughness of 0.242 nm (< one monolayer) determined over an area of (80×80) nm^2. The mean lateral correlation length is 1.8 nm, which appears plausible considering the low rms roughness because differences of already one Si atom between neighbouring unit cells drastically change the composition and thus break its correlation along the interface.

Various sub-nanometre-thin cross-sections can be taken from the tomogram in each crystallographic direction and at any spatial position. The voxel intensity of these slices is proportional to the Ge concentration and thus the slices allow a clear distinction between all Ge-wells and SiGe-barriers enabling the quantitative analysis of interface widths and layer thicknesses. To investigate the spatial fluctuation of these quantities, Ge concentration profiles are taken from several cross-sections along the direction of growth. The profiles are simulated as a series of sigmoidal functions. Thus, each interface position and its width are determined via the parameters of the sigmoidal profile [7] (not shown here). Preliminary results indicate interface widths of 1 to 2 nm. Based on this evaluation, we aim to map the chemical widths of the individual interfaces and the layer thickness fluctuations within the reconstructed needle.

4. Conclusion

With our contribution, we will demonstrate that ET allows to determine a complete set of structural parameters for the characterisation of buried interfaces in 3D. Our results may contribute to a further understanding of the growth process and the quantitative values can be used directly for device engineering.

Acknowledgements

The authors are grateful to Margarita Matzeck for the careful FIB preparation of the tomography needles. This work was partially supported by the European Union and the state of Berlin within the frame of the European Regional Development Fund (ERDF), project number 2016011843.

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Epitaxial SiGe/Si Multi-Layers for CFET Devices, Grown with a High Throughput Process

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1. Introduction

The complementary field-effect transistor (CFET) is an attractive device architecture for beyond 1 nm technology nodes (Fig. 1) [1]. In a CFET architecture, n- and p-MOS devices are formed on top of each other, removing the n-p spacing, allowing further maximization of the effective channel width and, hence, the drive current [1-3]. This architecture can be fabricated in either a monolithic or a sequential approach. In the monolithic approach, both n- and p-MOS transistors are built on the same wafer, while the sequential fabrication flow is based on wafer-to-wafer bonding techniques. In [1], it has been concluded that CFETs fabricated following a monolithic approach consume less area and outperform their sequential counterpart.

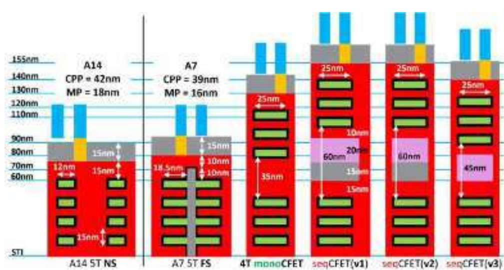

Fig. 1. Gate cross sections for nanosheet (NS), forksheet (FS) and monolithic (mono) and sequential (seq) CFET, discussed in [1].

The monolithic device fabrication flow starts with the epitaxial growth of a complicated SiGe/Si multi-stack with at least two different Ge concentrations (Fig. 2) and where a Ge-rich $Si_{1-y}Ge_y$ layer is later replaced by an isolating dielectric. Owing to the very small dimensions (e.g., sub-10 nm nanowire channel diameter), high etching selectivity of the $Si_{1-y}Ge_y$ layers towards both $Si_{1-x}Ge_x$ and Si, and excellent process controls are mandatory. This sets stringent requirements on the epitaxial stacks (thicknesses and composition control, sharpness of interfaces, and absence of strain relaxation) [4,5] as well as on the etch process (high selectivity, limited consumption of $Si_{1-x}Ge_x$ and Si) [5-8]. In our previous publications, the epitaxial layer stack was grown using higher order precursors and temperatures ≤ 500°C. This allowed the two-dimensional (2D) epitaxial growth of smooth, fully strained SiGe/Si multi-stacks with Ge concentrations up to 50%. However, the low growth temperature resulted in an extremely long process duration and a concern for the incorporation of point defects in the active layers of the device [9]. Improvements in the wet-chemical etching selectivity allow to reduce the Ge concentrations in the multi-stack. This opens the door to consider conventional process gases and higher growth temperatures for the epitaxial growth of the SiGe/Si multi-stack used in CFET devices. The current work describes the material properties of such layers which have been grown with more conventional process conditions.

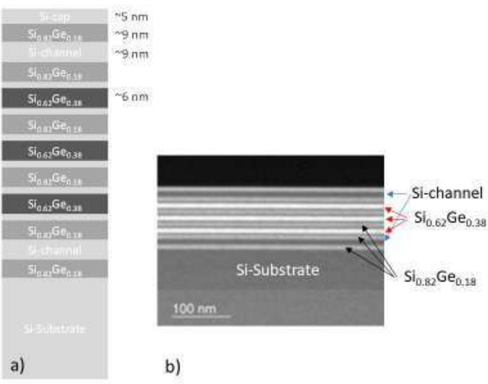

Fig. 2. a) Scheme and b) HAADF XTEM of a SiGe/Si multi-stack as used for CFET devices.

2. Experimental

The epi-layers were grown in a production compatible ASM Intrepid™ RP-CVD cluster tool. Before layer deposition, the 300 mm Si(001) wafer surface received a conventional wet-chemical clean. The native oxide was removed in-situ by a thermal treatment at a sufficiently high temperature (> 1000°C). The temperature profile within the epi-reactor has been carefully optimized to avoid the formation of slip lines during the pre-epi bake and to deposit epitaxial layers with a uniform thickness over the wafer (relative standard deviation < 1.3%). Epitaxial growth was carried out at reduced pressure using H_2 as carrier gas and conventional precursor gases (SiH_4, SiH_2Cl_2, and GeH_4 (5% in H_2)).

3. Results and Discussion

The chosen growth conditions enable 2D $Si_{1-y}Ge_y$ growth, without 3D islands, for Ge concentrations up to 40% as confirmed for single layers as well as for the complete CFET stack (Fig. 2b). The smooth surface of the resulting CFET stacks is confirmed by SEM inspections and haze measurements. No defects are observed across the wafer surface, in opposition to the low temperature process for which larger defects have been observed. The material quality is further confirmed by X-Ray Diffraction (XRD) (Fig. 3), X-Ray Reflectivity (XRR), and XRD-Reciprocal Space Maps (RSM) (Fig. 4). XRD and XRR spectra show well resolved peaks. The main XRD peaks at ~ -1800 arcsec and ~ -4000 arcsec are assigned to the $Si_{0.82}Ge_{0.18}$ and $Si_{0.62}Ge_{0.38}$ layers, respectively, although the peak position is not only given by the composition of these layers but also by the thicknesses of all individual layers (Fig. 3).

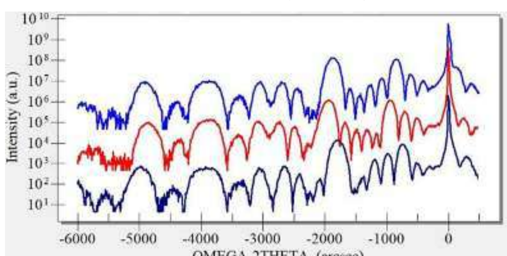

Fig. 3. Blue curve depicts the XRD ω-2θ scan acquired around the Si(004) Bragg reflection for the layer stack shown in Fig. 1a. Red and dark blue curves show the XRD ω-2θ scans as measured on samples for which the nominal $Si_{0.62}Ge_{0.38}$ thicknesses have been changed from 6 nm to 7 nm and 5 nm, respectively.

The RSMs, for which an example is shown in Fig. 4, confirm that the grown CFET stacks are fully strained. The narrow peaks of the individual layers reflect the high material quality. The peaks are narrower compared to those obtained for the low temperature epi process using higher order precursors. Except for the area near the wafer edge, the crystalline defect density, as measured on the layers grown in this work, lies below the detection limit of Electron Channeling Contrast Imaging (ECCI), which is ~1×10^5 defects/cm^2. Near the edge of the wafer, misfit dislocations are nevertheless present, because the wafer edge reduces the critical thickness for layer relaxation [10].

The required high etching selectivity of the $Si_{1-y}Ge_y$ layers towards both $Si_{1-x}Ge_x$ and Si, sets requirements on the sharpness of the interfaces between different layers. Extremely Low Impact Energy Secondary Ion Mass Spectrometry (EXLIE-SIMS) [11] and Energy-Dispersive X-ray spectroscopy (EDX) confirm that these gradients in Ge concentration are, within the experimental accuracy, the same for the layers grown at high temperature and conventional precursors as for those grown at low temperature and higher order precursors. After fin etching, a successful selective $Si_{0.62}Ge_{0.38}$ removal could be demonstrated.

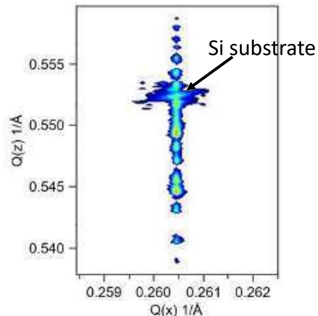

Fig. 4. XRD-RSM around the Si 113 Bragg reflection as measured for a CFET stack.

4. Conclusions

The material properties of complicated SiGe/Si multi-stacks used for CFET devices have been presented. The epitaxial layers contain two different Ge concentrations and have been grown using conventional process gases. Despite the higher growth temperature, island growth can be suppressed for Ge concentrations up to 40%. Excellent material properties have been reported with improved surface morphology and reduced defectivity compared to the low temperature growth process.

Acknowledgements

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Electron Emission Properties of Multiple-Stacked SiGe-Nanodots/Si Structures

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1. Introduction

Si and SiGe nanodots (NDs) formed on c-Si substrates have been attracted considerable attention because of their importance in practical applications such as electron-emission devices [1], light-emitting diodes [2], and functional nano-devices with quantum transport. To obtain reliable device operation, the QD size, uniformity in size, density, and position must be controlled with great precision and reproducibility [3]. In this study, we fabricated multiple-stacking staggered and vertical-aligned SiGe-NDs in Si by using a reduced-pressure chemical vapor deposition (RP-CVD) [4, 5], and demonstrated electron emission characteristics through the multiple-stacked SiGe-NDs and interpreted their emission mechanisms. In addition, we also characterized local electron transport properties by means of atomic force microscopy (AFM) using a conductive probe.

2. Experimental

After conventional wet-cleaning steps, ~50 nm-thick Si layers were epitaxially grown on n-Si(100) by the RP-CVD using SiH_4 at 700°C. Subsequently, $Si_{0.65}Ge_{0.35}$-NDs were deposited using a SiH_4 and GeH_4 gas mixture at 550°C. After that, the SiGe-NDs are covered by a 50 nm-thick Si spacer deposited by SiH_2Cl_2 or SiH_4 at 700°C to form the vertical-aligned and the staggered SiGe-NDs, respectively, to engineer the Si surface morphology [5]. By repeating the SiGe-NDs and Si-spacer deposition, 20-stacked SiGe NDs buried in Si structures were formed. For reference, 20-stacks $Si_{0.65}Ge_{0.35}$ quantum well (QW) structure is also fabricated by depositing Si spacer at 650°C [4]. After the formation of SiGe-ND and QW multiple-stacked structures, ~5.0 nm-thick SiO_2 layers were formed by atomic layer deposition (ALD). Finally, Au/Ti top- and Al bottom-electrodes were formed by thermal evaporation.

3. Results and Discussion

Formation of the 20-stacking staggered and vertical-aligned SiGe-NDs structures was also confirmed by TEM and AFM measurements (Fig. 1), where dot height was roughly estimated to be ~20 and ~15 nm for staggered and vertical-aligned NDs, respectively.

After the formation of top and bottom electrodes, sample current and electron field emission current were measured simultaneously in the vacuum of $\sim 10^{-2}$ Pa by applying DC sample bias to the bottom electrode with respect to the grounded top electrode. In this experiment, the anode electrode was placed ~10 mm away from the sample surface and biased at 40 V with respect to the top electrode as an acceleration voltage. With an increase in the sample bias in the forward direction, sample current increased due to electron injection from the n-Si(100) substrate, where no significant change in the current level between the vertical-aligned NDs and the QWs (Fig. 2). Notice that, electron emission was clearly detected at an applied bias over -4.5 and -5 V for the vertically-aligned NDs and the QWs, respectively. In addition, electron emission current was increased exponentially with an increase in the applied bias and tended to be saturated. No electron emission was observed in the reverse bias condition. Thus, it is likely that, in electron tunneling from the n-Si(100) through the SiGe/Si multiple-stacked structure, electrons can gain kinetic energies efficiently as a result of the reduced inelastic scattering rate. It is important noted that, electron emission current of the QWs was an order of magnitude lower than that of the vertical-aligned NDs. We also confirmed, for the vertical-aligned NDs structures without ALD-SiO_2, electron emission current was hardly detected. Considering the energy level difference of valence band between the strained SiGe-ND and the Si-spacer [6] and quantum confinement effect of the NDs, these results can be explained by the electric field concentration on the upper SiGe-ND layers caused by holes stored in the deep potential well of the SiGe-ND layers due to valence electron extraction and enhancement of electron injection from the substrate. We also found that, electron emission was observed for the staggered SiGe-NDs at an applied bias of -3.5 V and over. It is interesting to note that, for the staggered-NDs, although a threshold value of the emission current was almost the same as that of the aligned-NDs, the sample current decreased slightly.

This result is interpreted in terms of a decrease in the electron injection rate from the n-Si(100) to the NDs. However, in the applied bias below ~4.8 V, the electron emission efficiency of the staggered-NDs stack was dominant (Inset in Fig. 3). In addition, for the staggered-NDs, stable electron emission was obtained at lower input powers compared with the aligned-NDs.

To get an insight into the difference in electron emission efficiency between vertical-aligned and staggered NDs structures, topographic and current images were measured simultaneously by an AFM with a conducting probe at -3.5 V applied to the backside contact with respected to the tip. Although the current image for the staggered-NDs shows no relationship between high-conductive area and protrusions in the topographic image, protrusions of the vertical-aligned SiGe-NDs are corresponding to high conductive region. These results indicate difference in electron concentration between SiGe NDs and Si spaces, namely aligned-NDs act as electron transport pass. Therefore, an improvement of electron emission efficiency for the staggered-NDs can be explain by a decrease in current leakage with staggered structure. These results indicate that vertical-aligned SiGe-NDs structures is effective in enhancing the electron emission under the high-voltage application and that the staggered-NDs is suitable for low-voltage operation.

4. Conclusions

We have demonstrated stable electron emission from the multiple stacked SiGe-NDs embedded in Si/n-Si(100) under forward bias conditions over a threshold bias. In the case of staggered SiGe-NDs, the electron emission efficiency was enhanced markedly in comparison to the case of vertical-aligned SiGe-NDs under the same applied bias caused by a decrease in current leakage.

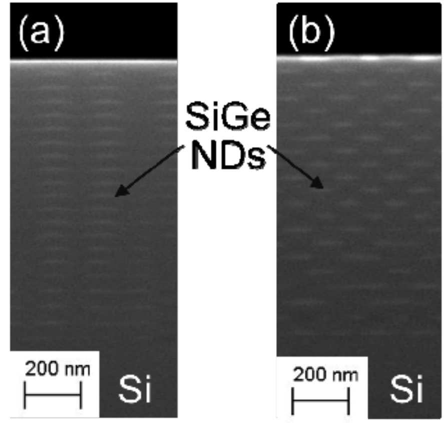

Fig.1 Cross-sectional TEM images of (a) vertical-aligned and (b) staggered SiGe-NDs/Si multiple-stacked structures.

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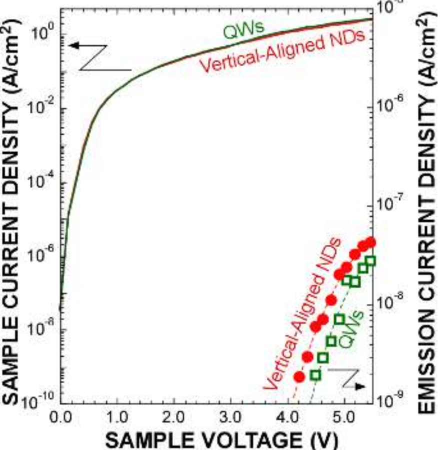

Fig. 2 Electron emission- and sample current-sample voltage characteristics of the aligned-NDs and QWs.

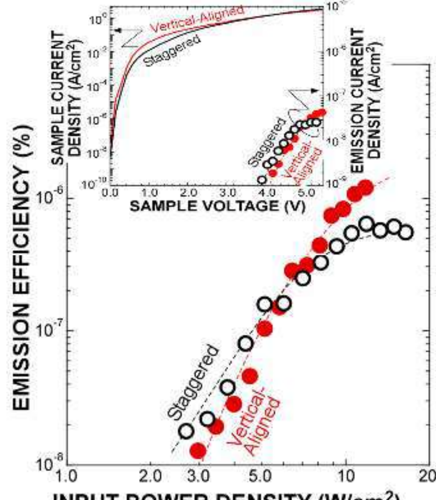

Fig. 3 Input power dependence of electron emission efficiency for aligned- and staggered-NDs. Electron emission- and sample current-sample voltage characteristics are also shown in the inset.

Multi-micrometer thick Ge/Si-Ge heterostructures for integrated THz photonic devices

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1. Introduction

Ge and Ge-rich multilayers are attracting a growing interest due to their CMOS compatibility and the wide range of possible applications, spanning from far- and mid-infrared integrated photonics to quantum computing. Their widespread adoption is however hindered by two distinct intrinsic issues of the material: the high threading dislocation density (TDD), arising from the large lattice mismatch between Si and Ge, and the need to manage the strain in the active region by introducing strain-compensation in the superlattice (SL) and lattice-matching between the latter and the virtual substrate[1]. These issues are particularly impactful in the deposition of quantum cascade structures, requiring the growth of several μm thick, strain-compensated active regions made of hundreds of quantum wells and thin tunneling barriers (~ 2 nm).

The recent observation of THz electroluminescence originating from intersubband transitions in the L-valley of n-type $Ge/Si_{0.15}Ge_{0.85}$ quantum cascade structures[2] suggests that the maturity of this material system may finally be approaching the standard required for this kind of application.

Here, we report on the growth of multi-μm thick n-type Ge/Si-Ge quantum cascade laser (QCL) active regions by ultra-high-vacuum chemical vapor deposition (UHV-CVD). We combine a thorough structural investigation with THz spectroscopy absorption measurements and simulations to assess the suitability of the UHV-CVD technique for the deposition of these complex quantum structures.

2.Results and discussion

Samples were grown by UHV-CVD in a cold-wall reactor (base pressure $2x10^{-10}$ Torr) using ultrapure germane and silane precursors with no carrier gases. The active layer stack was deposited on a reverse-graded Si-Ge/Ge/Si(001) virtual substrate (VS) suitably designed to obtain the right Ge content (~ 95%) for the strain compensation condition and a state-of-the-art TDD ~ $2x10^6$ cm^{-2}[3].

QCL active layers and VSs are structurally investigated by scanning transmission electron microscopy (STEM) and high-resolution X-ray diffraction (XRD). This structural information is complemented by the assessment of the TD density. Fourier transform infrared spectroscopy (FTIR) complemented by numerical simulations has been used to investigate the complex electronic subband structure and to probe the control acquired over the effective doping density and the dopant profile in the QCL active region.

In view of the realization of a QCL, the samples have been deposited on silicon-on-insulator substrates (SOI) to facilitate the double metal waveguide fabrication process. We focused on the 4-quantum well design for which non equilibrium Green's function (NEGF)-based calculations predict a net optical gain up to room temperature[4]. The conduction band diagram, Wannier-Stark states and carrier densities at 80 K predicted by NEGF at 50 mV/period are displayed in Fig 1 (a). Samples featuring up to 200 repetitions of the cascade structure (overall thickness of about 10 μm) were grown and characterized. The STEM images (Fig.1b) indicate high reproducibility of the structure with period variations <1%, i.e. at the sub-nm level. This reproducibility is confirmed by the sharp SL peaks present in the XRD θ/2θ curve (Fig.1c). XRD data also demonstrate the successful compensation of the strain in the active region. As such, a very low threading dislocation density of $2.0x10^6$ cm^{-2} has been measured by etch-pit method on the top surface after a total grown thickness of approximately 15 μm.

To gain further insight on the degree of control achieved by the growth process, we have investigated the THz intersubband features by means of FTIR spectroscopy. To this purpose, we used samples made of 20 repetitions of the single well QCL design (SW) from Ref. [2]. By relying on a multi-valley effective

mass Schrödinger-Poisson solver, we designed two QCL-like structures differing only for the doping-profile, which theoretically leads to radically different intersubband absorption features. The two samples have been doped with a nominal phosphorus doping of ~ $3x10^{17}$ cm^{-3} in the central 3 nm of either well 2 (SW2) or well 4 (SW4). The corresponding simulated L-band profiles, energy levels and square moduli of the electron wavefunction are reported in Fig. 2 (a) and (b), respectively. The calculated optical spectra for both samples are reported in Fig. 2(c). Absorption spectra were measured at a temperature of T=10 K in side-illuminated single-pass waveguide configuration. A single absorption peak at 16 meV related to the lasing transition of the design, i.e. the intersubband transition (ISBT) between the first two confined states in the undoped 5th well (W5), has been observed in both samples, in good agreement with the electroluminescence emission peak observed in [2].

A second more intense peak at 32 meV, related to the ISBT in W4, is also present in the spectrum of the SW4 sample. Since the significant difference in the absorption spectra of the two samples is entirely ascribable to the position of the dopants, the agreement between measured and simulated spectra demonstrates a precise control over the placement of dopants at the nanometric scale during growth.

These results represent a significant step forward in the Si-Ge epitaxy and in the use of this material platform for the development of integrated photonic quantum devices.

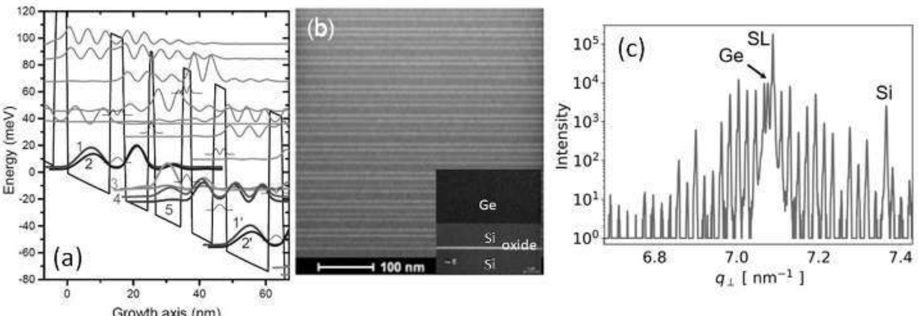

Fig. 1. (a) Numerically calculated L-band electronic structure highlighting key eigenstates, (b) STEM images and (c) XRD (004) θ/2θ curve of a 200 periods QCL sample.

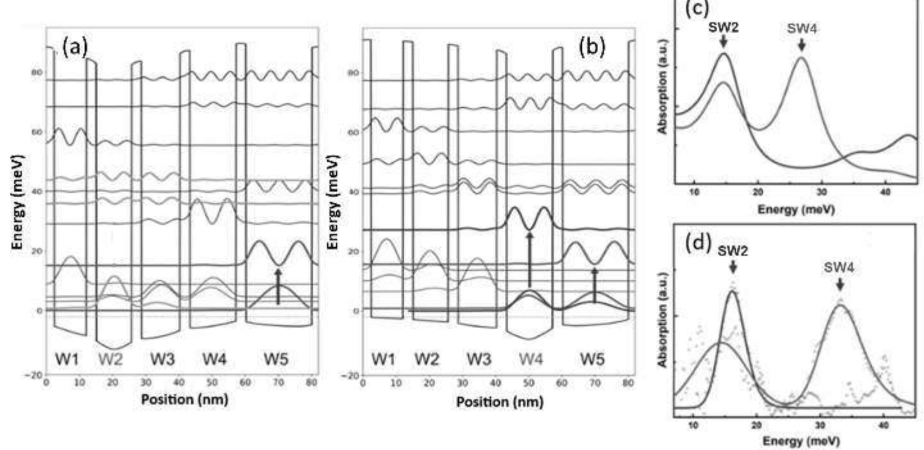

Fig. 2. Theoretical L-band electronic structures of the SW2 (well 2 doped) (a) and SW4 (well 4 doped) (b) samples. Theoretical (c) and experimental (d) THz absorption spectra of the two samples.

Acknowledgements

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Advanced (opto-)electronic Si devices based on supersaturated epitaxial (Si)Ge layers with high Ge content

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1. Introduction

Micro- and nanostructured silicon-germanium (SiGe) epitaxial alloys are integrated in many modern semiconductor devices that, in turn, form the basis of nowadays high-performance information- and communication technology. Hence, in particular, the properties of thin epitaxial (Si)Ge films with high Ge contents grown on Si(001) substrates still wake high prospects towards the realization of novel advanced device concepts essential for classical- and emerging quantum technology [1,2]. However, in the underlying epitaxial growth of pseudomorphic $Si/Si_{1-x}Ge_x$ heterostructures the accessible parameter range concerning Ge fraction (x) and layer thickness (d) is fundamentally limited [3] by the lattice mismatch of ~4.2% among crystalline Si and Ge. At typical growth temperatures, $T_S \geq 500°C$ the inherent strain quickly leads to plastic or elastic relaxation, in the former case via islanding or increase of the surface roughness or, in the latter case, via the insertion of dislocations above a misfit strain-dependent critical film thickness (d_c). This limiting thickness significantly reduces the flexibility of the SiGe system with respect to possible device designs and -functionality. An obvious approach to circumvent this issue and delay the relaxation processes to increase d_c for a given Ge content is to reduce the applied growth temperature [4]. However, so far, the use of $T_S < 500°C$ has often been excluded expecting a significantly reduced structural quality [5] due to the increased presence of point defects with respective drawbacks on electronic and optical properties of the heterostructures.

2. Experimental Methods and Results

In this contribution, we present the growth of SiGe nanosheet layers grown on Si(001) substrates using molecular beam epitaxy (MBE) at excellent chamber growth pressures that are regularly reaching the extreme high vacuum (XHV), i.e., $<10^{-12}$ mbar. This condition allows for the epitaxial growth of $Si/Si_{1-x}Ge_x$ heterostructures at ultra-low substrate temperatures (ULT) of $T_S \leq 350°C$ and enables us to push the previously assumed limits for pseudomorphic growth of (Si)Ge layers while maintaining an excellent structural quality of the samples.

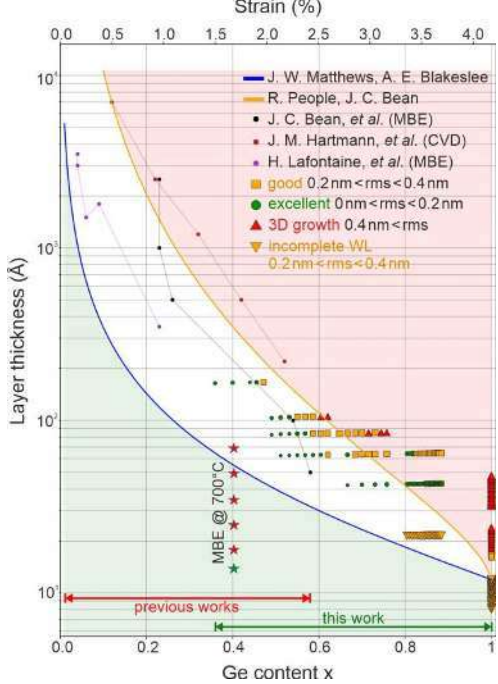

***Fig. 1**. Film thickness versus Ge content x of epitaxial Ge-rich $Si_{1-x}Ge_x$ on Si(001) layers [6]. Blue and yellow lines mark theoretical results from Matthews-Blakeslee (J. Cryst. Growth 27, 118 [1976]) and People-Bean (Appl. Phys. Lett. 47, 322 [1985], Appl. Phys. Lett. 49, 229 [1986]), respectively. Black, violet, and dark-red full-circles mark literature results from MBE and CVD-grown samples (J. Vac. Sci. Technol. A 2, 436 [1985], J. Appl. Phys. 110, 083529 [2011] and J. Vac. Sci. Technol. B 14, 1675 [1996]). Related to the present work, green circles, orange squares, orange downward pyramids, and upward red pyramids mark ideal 2D growth with a root mean square (rms) surface roughness <0.2 nm, 2D growth with slightly enhanced roughness (0.2 nm<rms<0.4 nm), growth of incomplete wetting layers, and 3D nucleation, respectively. While the above-mentioned Ge-rich $Si_{1-x}Ge_x$ epilayers were grown at $T_s \leq 350°C$, red and green stars mark the results obtained for the growth of $Si_{0.6}Ge_{0.4}$ grown at a 700°C.*

To illustrate the latter and highlight the usability for general device applications, we present an extensive study of $Si_{1-x}Ge_x$ epilayers with variable Ge contents of $0.35 < x < 1$ and layer thicknesses of $1.6 < d < 16.6$ nm [6]. These layers were grown at various growth temperatures in the range of $150°C < T_S < 350°C$. Here we initially focus on the surface roughness and -morphology of the layers characterized via atomic force microscopy, characterizing excellent samples as those with a root mean square (rms) surface roughness, rms < 0.2 nm and "good" samples with 0.2 < rms < 0.4 nm. Samples with higher surface roughness are referred to as three-dimensional (3D). See Fig. 1.

The excellent structural quality of the epilayers is further supported via X-ray diffraction line scans and reciprocal space maps, Hall mobility measurements, photoluminescence spectroscopy (PL), and transmission electron microscopy (TEM).
This approach allows us to grow several nanometer-thick Ge layers on Si without emerging plastic relaxation and only limited surface roughening.
In this presentation, we demonstrate that these high-quality nanosheets can be used in novel electronic device concepts relying on Al/SiGe exchange mechanisms since the SiGe nanosheet layers can withstand thermal annealing at least at 400°C without any detriment to their structural or electronic properties [1].
In light of recent advances regarding classical [7-9] and quantum [10] group-IV-based light emitters, the extended growth limits open up entirely new perspectives, not only for electronic- but also for optoelectronic devices. Here, emitter integration in efficient electrically-pumped devices is commonly limited by the absence of lattice-matched compounds that allow confining injected carriers to the emitter-site dot-in-well structures, as it is state-of-the-art for the III-V (Al)GaAs system. Here we show the realization of a first-generation of group-IV double-heterostructure LEDs, operating up to a sample temperature of 80°C, the limit of the used experimental setup.

4. Conclusions

In summary, we demonstrate that Ge-rich SiGe films with high epitaxial quality, deposited at extreme high vacuum conditions and unconventionally low growth temperatures (XHV-ULT growth), can be the means to add significant device functionality to the group-IV semiconductor system.

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1D Van der Waals Nanostructures: Harnessing Defects for New Functionality

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1. Introduction

Vapor-liquid-solid (VLS) growth using molten metal catalysts has been used to synthesize nanowires from a variety of 3D-crystalline semiconductors, including Si, Ge, III-V compounds, as well as oxides and nitrides. 1D nanostructures of 2D/layered crystals present opportunities for tuning structure and function far beyond those offered by 3D-crystalline semiconductors.

While the well-known hexagonal (or trigonal) 2D/layered crystals including graphene, boron nitride, and transition metal dichalcocenides tend to roll up into nanotubes, layered monochalcogenides (MX) where the anion species (M) includes Ge, Sn, and Ga, and X denotes one of the chalcogens S or Se, form a variety of different 1D nanostructures during VLS growth. Here, we discuss our recent progress in exploring new structural degrees of freedom arising from the integration of these layered crystals into nanostructures as well as unusual functionality emerging from ubiquitous defects.

2. Dominant (Fast-Growing) Defect Morphologies

While VLS growth of 3D crystals typically produces defect-free, single-crystalline nanowires, 1D van der Waals nanostructures are dominated by two types of fast-growing morphologies (Fig. 1): (i) nanoribbons, where material is incorporated from the VLS catalyst into open edges of the layered crystal [1-4]; and (ii) defect morphologies, in which a crystal defect enables nucleationless (*i.e.*, barrier-free) incorporation [5-8]. For van der Waals ribbons (Fig. 1a), the layer orientation can be adjusted *via* additives to the VLS catalyst [4]. Defect morphologies include chiral twisted nanowires that form by spiral growth around an axial screw dislocation (Fig. 1b) [5-7], and bicrystals where the nucleation-barrier is reduced in a twin-plane reentrant process (Fig. 1c) [8]. In comparison with defect-free wires, such fast-growing nanostructures are more numerous and grow to significantly greater length. Hence, the nanostructure selection during VLS growth follows an evolutionary process, where the system initially explores a large number of possible morphologies, of which the fastest-growing ones collect most of the incoming vapor and become the predominant synthesis product.

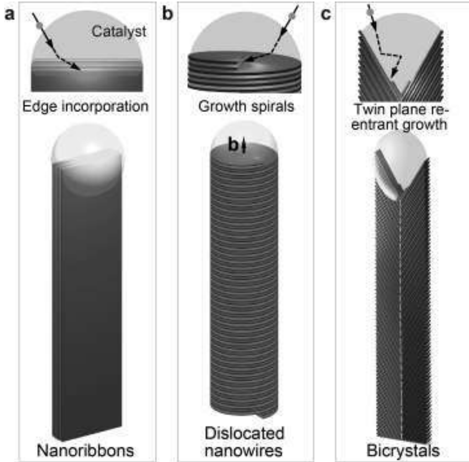

Fig. 1. Fast-growing van der Waals nanostructures obtained by VLS growth. a. Nanoribbons growing by incorporation from the VLS catalyst into exposed layer edges. b. Chiral twisted van der Waals nanowires, in which an axial screw dislocation enables nucleationless growth. c. Van der Waals bicrystals that grow by a twin-plane re-entrant process.

3. New Functionality from Defects

1D van der Waals nanostructures derive distinct functionality from both their layer orientation and from embedded defects. Prominent among these properties are intense light emission [8], nanophotonic light-matter hybrids [1,3], as well as stacking-fault induced symmetry-breaking and ferroelectricity [9].

An unconventional way of obtaining novel properties from 2D/layered materials involves layer stacking with a small interlayer twist. Effects arising from the resulting interlayer moirés include superconductivity, moiré excitons, ferroelectricity, *etc*. To date, twisted layers have been realized

exclusively by top-down mechanical assembly. In bottom-up van der Waals epitaxy, adjacent layers tend to lock into their (aligned) equilibrium registry, and interlayer twist has only been obtained for few systems and for special (typically large) twist angles.

We discovered that VLS growth of GeS produces nanowires that each host a single axial screw dislocation [5-7]. The dislocation induces Eshelby twist, which for a layered crystal translates into interlayer twist at a helicoid-shaped van der Waals interface. The twist angle is precisely tunable *via* the nanowire diameter, selected by the VLS catalyst size, and the screw dislocation stabilizes the twist moiré against re-orientation to the aligned registry. Twist moirés in nanowires open up degrees of freedom that have no equivalent in planar systems, *e.g.*, continuously variable twist in tapered wires and twist junctions connecting dislocated (twisted) and defect-free segments in the same wire [6]. Single nanowire spectroscopy demonstrates a modulated light emission accompanying the changing moiré registry along the twisted nanowires. Alternative VLS catalysts can be used to grow ultrathin nanowires that show exceptionally large twist as well as strong quantum confinement [7].

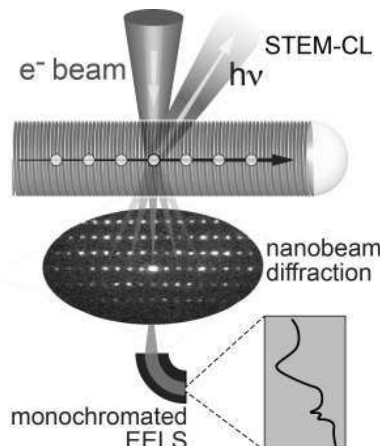

Fig. 2. Nanometer-scale structure probing correlated with electron beam stimulated spectroscopy. (Scanning) transmission electron microscopy ((S)TEM) and nanobeam electron diffraction, along with local absorption (EELS) and luminescence (STEM-CL) spectroscopies.

4. Nanometer-Scale Optoelectronic Spectroscopy

1D van der Waals nanostructures pose significant challenges of interrogating structure, morphology, and local changes to the electronic structure, photonic properties, *etc.*, due to layering, defects, and changing moiré registry. To address these challenges, we have developed advanced electron microscopy and associated electron-stimulated spectroscopy methods (Fig. 2). These approaches allow a full characterization of structure and function by combining imaging by (scanning) transmission electron microscopy ((S)TEM) with atomic-scale crystallography using nanobeam electron diffraction, as well as local cathodoluminescence (STEM-CL) and absorption spectroscopy using monochromated electron energy loss spectroscopy (EELS). We will discuss applications of these powerful experiments to the probing of photonic modes in nanoribbon waveguides, modulated electronic structure in chiral twisted nanowires, and effects of crystal defects on light emission, quantified *via* the spontaneous emission quantum efficiency.

5. Conclusions

Unique opportunities for tuning of crystal structure, morphology, and defects, along with the resulting effects on optoelectronics, photonics, and other properites create a rich playground for the discovery of new functional nanomaterials based on van der Waals crystals.

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Van der Waals Epitaxy of Quasi Two-Dimensional GeTe-Rich $(GeTe)_m(Sb_2Te_3)_n$ Layered Alloys on Silicon

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1. Introduction

The Ge-Sb-Te chalcogenide family possesses a generous variety of functional properties, spanning topological, [1] thermoelectric (TE), [2] ferroelectric (FE) [3,4] and phase-change properties. [5] In Fig. 1 the TE properties of epitaxial $Sb_{2+x}Te_3$ thin films are shown.

Phase-change memory (PCM) devices employing the pseudo-binary $Ge_2Sb_2Te_5$ (GST225) compound as the active material are nowadays an established non-volatile technology. PCM devices are based on reversible phase transitions from amorphous to crystalline and vice versa induced by short current pulses. New interest in $(GeTe)_m(Sb_2Te_3)_n$ (GST) has been ignited by its possible use for brain-inspired computing. [6]

For embedded PCM devices requiring a higher crystallization temperature, e.g. for automotive applications, the use of GST225 is prevented. The tailoring of the crystallization properties of GST by engineering the alloy composition is therefore fundamental. In this framework, GST alloys with Ge-rich composition have shown increased crystallization temperatures proportional to the excess of Ge. [7]

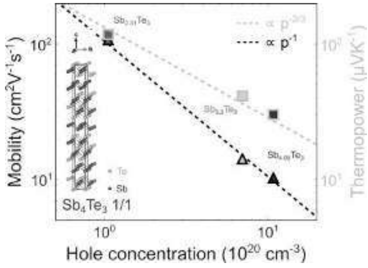

Fig. 1. TE properties of epitaxial $Sb_{2+x}Te_3$ thin films. Adapted from Cecchi et al.. [2]

Germanium telluride (GeTe) is the father compound of a new class of materials, namely FE Rashba semiconductors. GeTe was proposed to achieve both memory and spin-orbit transduction in a single, silicon-compatible semiconductor. The giant bulk Rashba-like spin texture of GeTe can be reversed by its non-volatile ferroelectricity, providing a chance to obtain FE control of spin-to-charge conversion. [3] Such FE-driven switching has been recently demonstrated in GeTe epitaxial films at room temperature (see Fig. 2). [4]

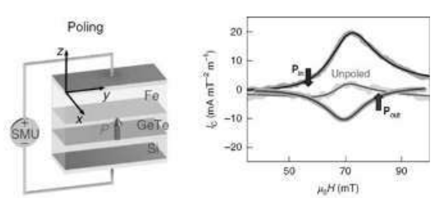

Fig. 2. FE-switching-controlled spin-to-charge current conversion in GeTe. Adapted from Varotto et al.. [4]

2. Methods and Results

A key element for the exploitation of the rich playground offered by Ge-Sb-Te layered chalcogenides is the high crystal quality achieved for the material deposited by molecular beam epitaxy (MBE) on Sb-passivated Si(111) substrates. The main aspects of the fabrication of epitaxial GeTe and Ge-Sb-Te quasi van der Waals alloys and multilayers will be recalled. [8–10]

Strategies to grow high-quality epitaxial GST films with GeTe-rich composition will be discussed next, aimed at controlling the epilayer composition between GST225 and GeTe. Indeed, a tuning of the FE

properties would be desirable to facilitate the spin-orbit transduction operation. Moreover, the possibility to combine the phase-change switching properties, typical of GST alloys, with the FE ones of the binary compound GeTe is extremely appealing for the design of novel multifunctional memory devices.

The characterization of structural, vibrational and FE properties as function of composition, supported by density functional theory calculations, will be presented.

3. Conclusions

The tuning of the composition of epitaxial GST films towards GeTe has been accomplished. The evolution of the epitaxial quality with composition is evaluated. The evidence of composition-dependent FE properties is found.

Acknowledgements

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Electronic and morphological properties of the graphene/Ge(110) interface as a function of temperature

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1. Introduction

Graphene gives rise to many unique properties and device concepts, with transformational opportunities for integrated solid state device technology [1]. In this contest a viable growth route for obtaining metal-free, CMOS-compatible graphene suitable for electronic and optoelectronics applications is the CVD graphene on Ge system. Indeed, thanks to the catalytic activity of Ge on carbon precursors combined with Ge carbides instability, and low C solubility, the controlled synthesis of graphene on the Ge surface is allowed [2]. Initially, most of the attention has been focused on the technologically relevant Ge(001) surface. However the development during the growth of Ge(001) nanofaceting under the graphene [3-4] questioned its suitability for technological processing, and has led to interest in graphene/Ge(110) for which the underlying Ge surface not only remains flat but also promotes the formation of a graphene single crystal. The data reported in literature reveal a complex scenario for the graphene/Ge(110) interface properties depending on hydrogen presence and annealing temperature, questioning a possible interaction between graphene and Ge surface [5-7]. However, a clear picture of the graphene/Ge(100) interface properties is still lacking. In this work we will investigate in detail the role of the growth and annealing temperatures on the properties of the graphene/Ge(110) system.

2. Results and discussion

The graphene films on Ge(110) substrate were deposited by chemical vapor deposition (CVD) using methane, hydrogen and Ar as carrier gas. Deposition temperature was set in the 910 - 930 °C range using a raising procedure that ensures an accurate control of temperature close to the Ge melting. Post growth annealing up to 800 °C were performed in UHV. The samples were characterized by X-ray, angle resolved photoemission spectroscopy (ARPES) and Raman spectroscopy, atomic force microscopy (AFM) and scanning tunneling microscopy (STM).

We investigated the role of the deposition temperature T_D on the graphene quality by depositing samples at T_D equal to 910, 920 and 930 °C for a deposition time of 60 min. All the samples are single layer graphene: we found that the total amount of carbon did not depend significantly on the T_D in this range explored [8]. Raman spectra, AFM and STM images of the three samples are reported in Fig. 1. The small variation of the growth temperature has a significant effect on the quality of the grown graphene. In all the samples Raman spectra (panel a) show the features of graphene, i.e. 2D and G bands respectively at about 2700 and 1600 cm^{-1}. The D peak originating from the scattering due to defects is also visible. At the higher T_D we observe the larger I_2/I_G and lower I_D/I_G intensity ratios. These findings evidence as in this temperature range an increase of T_D as low as 20 °C produces a major improvement in the crystalline quality, and it is also effective in the reduction of the defect density in the as-grown graphene sample. AFM and STM images of the three samples (panels b-d) reveal that also the morphology changes dramatically. AFM measurements acquired at large size scale evidence the presence of the Ge terraces in all the samples but their width increases remarkably with T_D, from being <70 nm at 910 °C to be larger than hundreds of nm at 930 °C. At higher magnification, STM data reveal that in all the samples graphene covers uniformly the Ge surface following the corrugation of the substrate surface. In the samples grown for T_D below 930 ° C ridges and round bumps are present; graphene became flat in the sample grown at 930 °C that shows a rms roughness of 0.21 Å, a value half of that found at lower T_D. We attribute this abrupt temperature dependence to the formation of a quasi-liquid Ge surface that favors the formation of high quality graphene, through a mechanism observed also on the graphene/Ge(100) system [8].

We investigate the graphene/Ge(110) interface properties of the best quality sample (i.e the sample deposited at T_D=930 °C) by performing post-growth

annealing at different temperature *T*. The annealing temperature affects both the graphene quality and interface characteristics, as shown in Fig. 2: by rising *T* up to 800 °C three different phases appear characterized by different Ge surface reconstruction underneath the graphene layer and different graphene electronic properties. For *T* below 350 °C the hydrogenated Ge(110) surface shows a 1x1 reconstruction. ARPES measurements reveal that the graphene overlayer is *p* doped. The corresponding Raman spectrum is similar to that of the as-grown sample. The *T* increase above 350 °C produces hydrogen desorption from the Ge surface meanwhile novel (6x2) Ge surface reconstruction is detected by STM. ARPES investigation reveals that graphene is now intrinsic in this condition with the Fermi level pinned at the Dirac point. All these changes produce defects in the graphene layer, as well evident in the Raman spectra of the samples annealed at 450 °C and 650 °C where a well evident D peak develops. Interestingly, these defects can be healed by a further annealing at 800 °C. Indeed, in this case the Raman spectrum of the sample is characterized by the absence of the D peak due to defects, and also the I_{2D}/I_G ratio increases up to the same values found in the pristine graphene, indicating that the pristine (or better) graphene quality has been restored by the high temperature process. This defect healing process is accomplished by a further evolution of the Ge surface underneath the graphene detected by STM, that now is 1x1 reconstructed, while graphene appears n-doped during ARPES measurements.

Thus we proved that post-growth annealing can tune the interface properties of the system in terms of doping and Ge surface reconstruction, and significantly are able to restore high quality graphene by healing the defects induced by hydrogen desorption.

Acknowledgements

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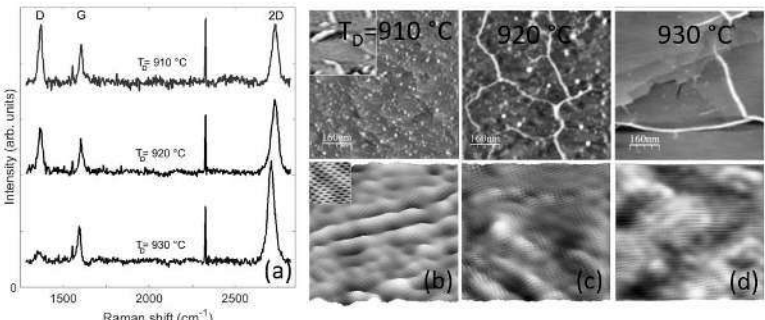

Fig. 1 Samples grown at different T_D. (a): Raman spectra. (b-d): AFM (upper panels) and STM (lower panels) images

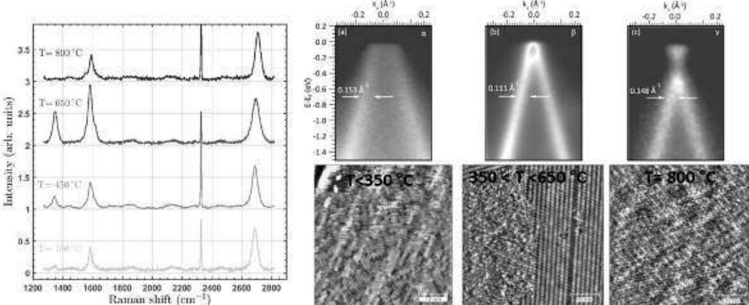

Fig. 2. Samples grown at 930 °C and annealed at different temperature *T*. Right panel: Raman spectra. Left lower panels: STM measured at 10 K; left upper panels: ARPES measurements.

Applications of Graphene-Semiconductor Schottky Junctions to Reconfigurable Field-Effect Transistors

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1. Introduction

Graphene has attracted broad interest in the last decade because of its extraordinary properties, such as very large carrier mobility at room temperature. Due to its semimetal nature, graphene forms a Schottky junction with a wide variety of semiconductors. The graphene-semiconductor diodes have been used to fabricate photodetectors [1] and solar cells [2]. However, they can also be exploited to modulate the conductivity of the channel of a graphene-semiconductor field-effect transistor (FET) [3].

In this talk, we will discuss the characterization of the Schottky junctions between graphene and the following three n-type semiconductors: Si, Ge, and GaAs. We will also demonstrate that the graphene-GaAs Schottky diode can be used as a gate of a FET, capable of adjusting its threshold voltage during operation, paving the way for a new class of reconfigurable devices.

2. Device Fabrication and Characterization

2.1. Graphene-Semiconductor Schottky Diodes

We fabricated graphene-semiconductor Schottky junctions on four lightly n-doped substrates. We used n-type GaAs grown by molecular beam epitaxy (MBE), n-Si and n-Ge grown by low-energy plasma-enhanced chemical vapor deposition (LEPE-CVD), and commercially available n-Ge wafers. Fig. 1 shows the electrical characterization of the fabricated Schottky junctions. Graphene-Si diodes show a poor rectifying behavior with an ON/OFF ratio of ~10, while CVD-Ge and commercial Ge show an acceptable ON/OFF ratio of $\sim 10^2$ and $\sim 10^3$, respectively. Graphene-GaAs diodes show the largest ON/OFF ratio ($\sim 10^5$) and have a very low OFF current compared to all the other substrates, which is crucial for a low gate-leakage current of a FET.

2.2. Graphene – GaAs FET

In a metal-semiconductor FET (MESFET), the conductivity of the channel is controlled by the metal-semiconductor Schottky junction. We realized a similar device by using the graphene-GaAs Schottky diode as a gate of the FET. The graphene gate modulates the depletion layer width in the GaAs channel and, therefore, the drain current (I_D). A schematic of the device is reported in Fig. 2a.

In conventional MESFETs, the threshold voltage (V_{th}) of the device is set by the work function of both the metal gate and semiconductor channel during fabrication. However, due to the semimetal nature of graphene, it is possible to adjust its the Fermi level, i.e., its work function, by an additional metal/oxide stack (control gate), which is placed on top of the graphene gate, as shown in Fig. 2b.

A variation of the work function of graphene resulted in the modulation of the graphene-GaAs Schottky barrier height (SBH), which set V_{th}. Such effect has been used in the past to realize graphene barristors [4] and vertical heterostructures [5].

We exploited the modulation of the SBH to realize GaAs FETs in which V_{th} was shifted from negative to positive values by changing the control gate voltage V_{GC}. The transfer characteristics of such a GaAs FET are shown in Fig. 3. This allowed the fabrication of logic inverters with positive switching threshold, which is a fundamental requirement for the realization of integrated circuits (ICs).

3. Conclusions

We investigated the formation of a Schottky diode between graphene and different n-type semiconductors. The graphene-GaAs junction was exploited to fabricate an innovative FET, in which the threshold voltage can be adjusted during operation. This paves the way for novel ICs exhibiting additional functionalities.

Acknowledgements

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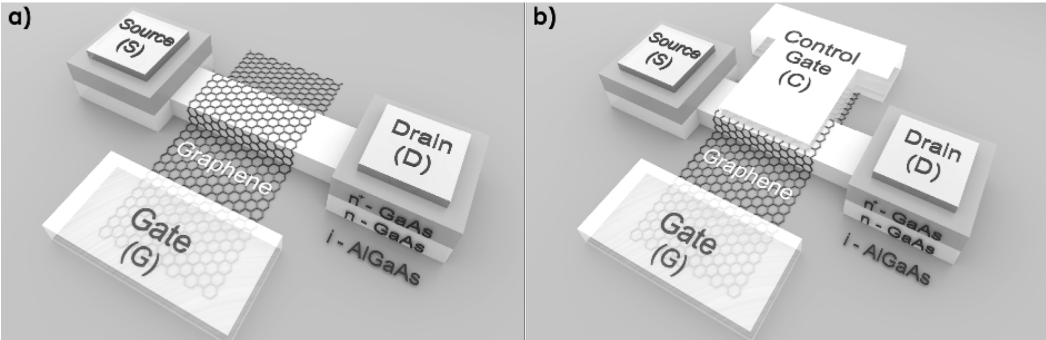

Fig 1. A GaAs FET with a graphene gate. (a) Schematic of a single-gate graphene-GaAs FET on an insulating AlGaAs substrate. The graphene gate is deposited on top of an n-GaAs layer with a donor concentration of 10^{17} cm^{-3} and connected externally by an Au gate pad (G). The graphene gate controls the conductivity of the GaAs channel, modulating the current flow between source (S) and drain (D). (b) Schematic of a dual-gate graphene-GaAs FET. The additional control gate (C) controls the graphene Fermi level and, therefore, the Schottky barrier height (which affects the modulation of the current in the transistor channel).

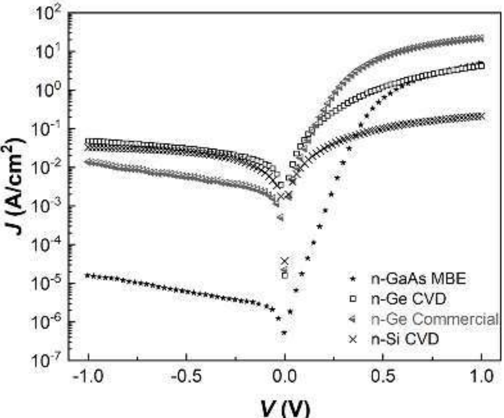

Fig 2. Electrical characteristics of the graphene-semiconductor diodes showing the rectifying behavior. The OFF current of the GaAs-graphene diode (stars) is three orders of magnitude smaller than that of the other devices, while its ON current is comparable to the CVD grown Ge (squares).

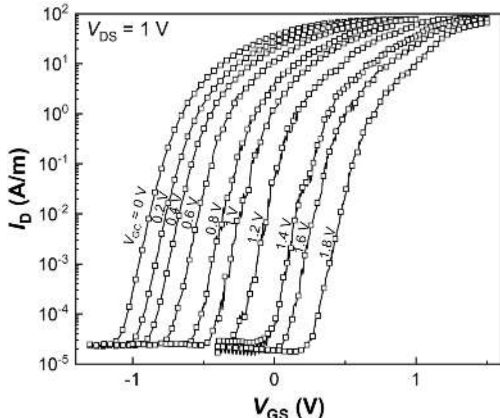

Fig 3. Transfer characteristics of a dual-gate graphene-GaAs FET where the drain current I_D (normalized by the channel width) is measured as a function of V_{GS} at different V_{GC}. Increasing V_{GC} from 0 to 1.8 V shifts the curves and V_{th} to more positive V_{GS}. All curves were measured at V_{DS} = 1 V.

Growth of Nd_2O_3 layers on germanium-rich, (111)-oriented SiGe layers

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1. Introduction

The charge carrier mobility is a crucial parameter in modern MOS-devices. Thus, a lot of efforts have been undertaken to increase the mobility, e.g. by inducing strain [1]. However, substituting the silicon channel by another material, which features even higher mobility, is a challenging task and various investigations with this subject were conducted [2,3]. Germanium has shown a very high hole mobility making it especially desirable for p-MOS devices [2]. Besides the challenge of integrating Ge on Si, Ge-based MOS devices suffer from a high density of interface states when conventional high-k gate dielectrics are used [3]. Promising candidates as a high-k dielectric with low density of interface states are rare-earth oxides as shown for amorphous $(La\text{-}Lu)_2O_3$ [3] and crystalline Gd_2O_3 [4].

Another material among the rare-earth oxides is Nd_2O_3. The cubic phase of Nd_2O_3 matches the lattice of Si(111) with a mismatch of 2 %. It grows with an A/B stacking and shows promising dielectric behavior with a dielectric constant above 14 [5,6]. If the hexagonal phase can be achieved like on Si(001), an even higher dielectric constant of up to 27 is expected [6].

For other rare-earth oxides it has been shown that the phase can be altered by inducing strain [7]. Since the cubic lattice of Nd_2O_3 matches $Si_{0.48}Ge_{0.52}$, $Si_{1\text{-}x}Ge_x$ layers enable a systematic variation of the surface lattice parameter and thus the strain by varying the Ge content. This could enable a determination of the formation mechanism and thus a transfer to germanium.

In this work, we focus on the structural characterization and growth of Nd_2O_3 layer on fully relaxed Ge and germanium-rich $Si_{1\text{-}x}Ge_x$ layers with $0.5 < x < 1$ on Si(111) substrates. By varying the Ge content in the $Si_{1\text{-}x}Ge_x$ layer, the effect of tensile strain on the growth and a possible phase transition is investigated.

The germanium-rich $Si_{1\text{-}x}Ge_x$ layers were grown in a molecular beam epitaxy system by carbon-mediated epitaxy (CME) [8]. The Nd_2O_3 layers were deposited afterwards at a starting temperature of 400 °C. During oxide growth, the oxide partial pressure was kept constant at $5 \cdot 10^{-7}$ mbar and the temperature was increased by 50 K/min to 650 °C. The samples were analyzed using reflection high-energy electron diffraction (RHEED), X-ray diffraction (XRD), X-ray photoelectron spectroscopy (XPS) and transmission electron microscopy (TEM).

2. Results and Discussion

After growth of the virtual substrates as described in [8] the *in situ* RHEED control showed a smooth surface and the $Si_{1\text{-}x}Ge_x$ layers exhibited a c(2×8) surface reconstruction. During annealing to 400 °C the surface reconstruction of the $Si_{1\text{-}x}Ge_x$ layers changed to a 7×7 reconstruction while the Ge layers still showed a 1×1 reconstruction as described in more detail in [9]. After growth of the oxide layer, RHEED control showed a smooth surface for layers grown on higher Ge contents and surface roughening for contents below 70%.

We also investigated the crystallographic phase and strain in the oxide layer by utilizing XRD. Measurements in skew geometry showed strong tensile strain in the oxide layer when grown on pure Ge. In contrast, layers grown on $Si_{1\text{-}x}Ge_x$ layers exhibited a relaxed cubic phase. Even more, measurements as shown in Fig. 1 show hexagonal parts in the oxide layers regardless of their layer thickness when grown on $Si_{1\text{-}x}Ge_x$ layers.

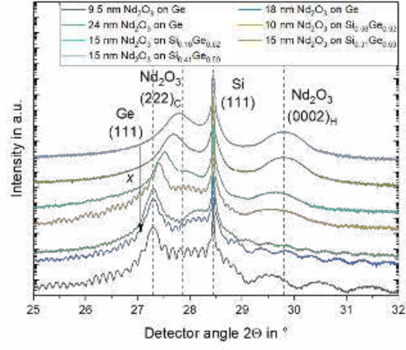

Fig. 1. XRD measurements of various Nd_2O_3 layers grown on fully relaxed $Si_{1\text{-}x}Ge_x$ layers with $0.59 < x < 1$ and pure Ge layers on Si(111) substrates.

In order to determine the epitaxial relation, we also performed grazing incidence XRD. This resulted in

$Nd_2O_3(0001)[2\bar{1}\bar{1}0] \parallel SiGe(111)[1\bar{1}0]$ for the hexagonal phase and $Nd_2O_3(111)[\bar{1}10] \parallel SiGe(111)[1\bar{1}0]$ for the cubic phase.

TEM analysis as shown in Fig. 2 was performed in order to investigate the interface and phases in the oxide layer. The oxide layer grown on a pure Ge layer shows a sharp interface and no interfacial layer is observed. This is supported by the thickness fringes in Fig. 1.

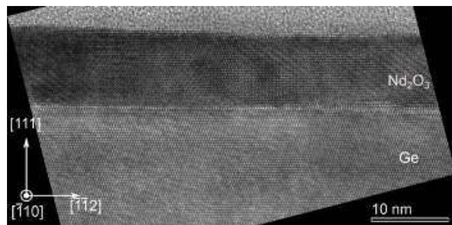

Fig. 2. Cross sectional high resolution REM image of a Nd_2O_3 layer on Ge in $[1\bar{1}0]$ direction.

According to the XRD results the oxide layer seems to relax the induced strain in the cubic phase by a phase transformation to the hexagonal phase. In contrast to this, layers grown on Ge with even higher layer thickness show no indication of hexagonal parts despite larger strain. Because of this, the phase transformation should not only be related to strain but also effects at the interface between the oxide and the $Si_{1-x}Ge_x$ virtual substrate. For example, the different surface reconstruction of the $Si_{1-x}Ge_x$ surface with a 7×7 reconstruction compared to the 1×1 reconstruction of the Ge surface might influence the growth. Furthermore, segregation effects might play a significant role at the interface formation. Investigation of this interface is still subject to further investigation.

Furthermore, we investigated the interface and surface *in vacuo* with XPS. The results showed a silicate-like interface and analysis of the valence band offset resulted in an offset of around 2 eV. Taking the band gap of Nd_2O_3 of around 5.7 eV [10] into account this results also in more than 2 eV offset at the conduction band edge.

3. Conclusions

In conclusion, this work established the growth of Nd_2O_3 layers on virtual germanium-rich $Si_{1-x}Ge_x$ substrates on Si(111). It was shown that the oxide grows tensile strained on pure Ge layers and exhibits hexagonal parts when grown on germanium-rich $Si_{1-x}Ge_x$ layers. TEM indicated a sharp interface between the Nd_2O_3 layer and the virtual substrate. In addition, we found band offsets for the valence band and conduction band between the oxide layer and virtual substrate of more than 2 eV.

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Direct Exchange Interactions in Epitaxially Self-Assembled Heterostructures of Ternary Silicides on Si

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1. Introduction

Miniaturization has been an important trend in all kind of contemporary devices - electronic, optoelectronic, mechanical, and magnetic alike. Each of them for good reasons pertinent to their respective fields, e.g., ability to fabricate magnetic High Density Data Storage (HDDS) memory devices. Small cell size also increases magnetic coercivity and anisotropy, and consequently the cell stability and non-volatility. However, the above magnetic properties and advantages derived from them, do not monotonically grow with decreasing cell size. In fact, once magnetic crystal shrinks to dimensions comparable with a single domain size, the opposite trend ensues. In case of a magnetic nanoparticle assembly, it enters the notorious superparamagnetic (SPM) state and loses magnetic anisotropy.

Among plausible solutions to this problem, spintronics utilizes layered structures with direct exchange interactions between materials with different magnetic properties. Such interactions between harder and softer ferromagnets (FM) lead to an exchange spring magnet effect, or to exchange bias effect in case of coupled FM and antiferromagnet (AFM). The layered structures are usually realized in epitaxial multilayers or in core-shell nanoparticles.

2. Results

In this work, we demonstrate how such effects can take place by means of natural layering in self-assembled ternary (Ni-Fe-Si) nanometric silicide heterostructures on silicon. In these experiments, commercial $Ni_{80}Fe_{20}$ Permalloy was solid-phase epitaxially reacted with Si substrate atoms in vicinal (001) and (111) orientations. In both Si substrate orientations, the first silicide phase to form was CaF_2-based γ-$(NiFe)Si_2$. This structure is a well-known interface-stabilized precursor in a binary Fe/Si epitaxial system, that on a Si(111) surface can transform into a thermodynamically stable α or β disilicide phase [1]. However in the ternary FeNi/Si(111) case, while both Fe and Ni are fast diffusants in Si, Ni is the faster one, and prolonged annealing at elevated temperatures cause indiffusion

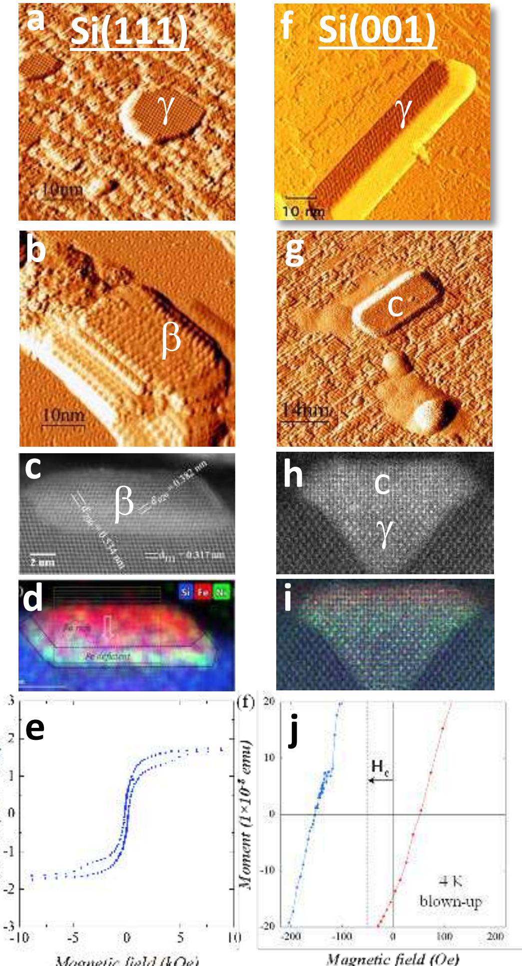

Fig. 1. Evolution Fe-Ni-Si nanoheterostructure assembly and respective magnetic properties on vicinal (a)-(e) Si(111) and (f)-(j) Si(001) substrates. (a) and (f) STM images of characteristic γ-phase nanostructures on these respective substrates, and transformation into (b) β-phase and (g) c-phase, respectively. (c)-(d) X-sectional HAADF and STEM-EDS of the β-nanostructures with the (e) resulting SQUID magnetization reversal curve. (h)-(i) X-sectional HAADF and STEM-EDS of the c/γ-nanostructures with the

(j) resulting SQUID magnetization reversal curve. Adopted from Refs. [1], [2].

of Ni towards the silicide/silicon interface. As a result, a layered structure is formed within the silicide nanoislands, with Fe-rich top parts, and Ni-rich bottoms. On Si(111) substrates, this compositional layering occurred inside the otherwise crystallographically uniform orthorhombic β-(FeNi)Si_2 islands, creating *de facto* coupling between the harder Fe-rich FM on top and softer Ni-rich FM on the bottom, and so forming an exchange spring magnet [1]. On the Si(001) substrate, not only compositional, but structural transformation took place, with the Fe-rich top island parts undergoing γ-Fe(Ni)Si_2 to c-Fe(Ni)Si phase transformation, while the bottom Ni-rich parts retained their γ-Ni(Fe)Si_2 crystal structure. The spontaneously formed coupling in this case lead to creation of exchange bias, because the coupling this time was created between the top c-Ni(Fe)Si monosilicide layer, known to exhibit AFM order, and the FM bottom γ-Fe(Ni)Si_2 disilicide [2].

3. Conclusions

In this work, we demonstrated how complex functional heterostructures can be bottom-up fabricated on silicon, exploiting natural thermodynamic and kinetic tendencies. Specifically, different diffusivities of Fe and Ni in silicon were used to create functionally graded layered heterostructures inside self-assembled epitaxial nanometric islands, where coupling of Fe-rich and Ni-rich layers spontaneously created direct exchange interactions, increasing magnetic stability of the nanoisland assembly. The above compositional inhomogeneity and layering, as well as faceting of the interface with Si substrates, can be avoided by controlling the temperature of the thermal annealing regime. We have shown, for example, that this way the precursor compositionally-uniform γ-(FeNi)Si_2 discs, with atomically flat coherent interfaces and no intermixing, can be prepared [3].

Acknowledgements

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Bandgap Determination of Lattice-Matched SiGeSn on Ge with pin Diodes

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1. Introduction

In the past decade, the ternary alloy semiconductor SiGeSn has emerged as promising material for Group-IV heterostructure devices due to its unique properties [1–5]. The alloying of Si, Ge and Sn allows not only the decoupling of its bandgap and its lattice-constant whereby it is predestined for strain-reduced heterostructures on Ge [6,7]. Furthermore, it becomes a direct bandgap semiconductor at specific compositions [2,8,9]. Possible applications for SiGeSn range from the Si-integrated laser to tunneling field effect transistors for the next complementary metal oxide semiconductor (CMOS) generation.

However, due to the novelty of the material, many of its electronic parameters, such as the bandgap and band offsets, are not well known although essentially needed for the design of heterostructures. In view of the quasi-directness of SiGeSn, the determination of its bandgap requires pre-considerations. On the one hand, the lowest band transition affects the possible applications. Furthermore, the direct bandgap of a semiconductor can be determined in a different way than the indirect bandgap.

In this work, we present experimental data for the indirect bandgap of SiGeSn, lattice-matched on Ge. Using the simulative results of Moontragoon et al. [9], we plotted the Γ, L and X band transitions of SiGeSn in dependence of its composition (see Fig. 1) to determine the dominant band transition of the investigated composition range. The bandgap data was determined by capacitance voltage (CV) measurements on MBE-grown SiGeSn pin diodes. Furthermore, we give some first estimations for effective masses and the effective density of states for SiGeSn for the necessary calculations.

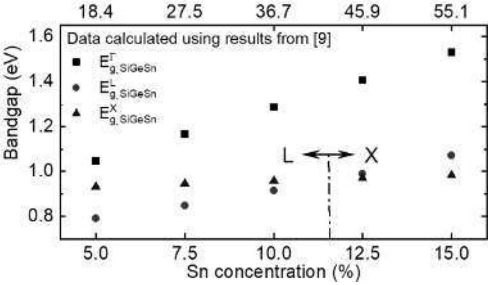

Fig. 1. Band transitions of SiGeSn

2. Experimental Details

All presented samples were grown in a 6” MBE system with Si, Ge and Sn as used matrix materials and B and Sb as dopants. All elements, except Si, were evaporated with Knudsen effusion cells and Si with an e-beam evaporator respectively. The substrate temperature T_S was controlled using a calibrated thermocouple for all processes T_S > 200°C and a mid-infrared pyrometer for the SiGeSn growth at $T_S \leq 200$ °C.

All device structures are based on Si(001) substrates. For further reduction of the threading dislocation density, the growth process of the Ge-VS, consisting of a 100 nm thick Ge layer and a thermal annealing step at T_S = 830 °C for 5 min [10], was repeated for a total of 5 times. Afterwards, the SiGeSn pin diode starts with a 400 nm thick p-type doped SiGeSn bottom layer (BL), followed by a 300 nm thick intrinsic region and closed with a 200 nm thick n-type doped top layer (TL). The dopant concentrations for the BL as well as the TL was adjusted to $N_{A,D} = 5 \cdot 10^{19}$ cm^{-3}. The SiGeSn composition was kept constant throughout the complete pin diode stack. In total, we grew three samples with a variation of the SiGeSn composition for 5.0 %, 7.5 % and 10.0 % Sn. In order to fulfill the condition for lattice-matching on Ge, a constant ration of Si/Sn =3.67 was applied.

Subsequent to the material growth, discrete devices were fabricated using a CMOS-compatible single mesa process, similar as reported in [7]. A schematic layer stack and a scanning electron microscopy (SEM) image of a final device with a mesa radius of 20 µm are shown in Fig. 2.

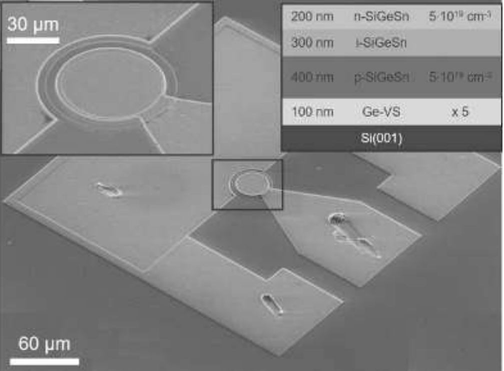

Fig. 2. SEM image of the device and schematic layer stack

3. Results

For a first evaluation of the device and material quality, current voltage (IV) measurements were performed using a Keithley 4200 semiconductor characterization system. For comparison, we normalized the results on the device are, leading to exemplary current density voltage characteristics (JV) of devices with a mesa radius of 5 µm, which can be seen in Fig. 3.

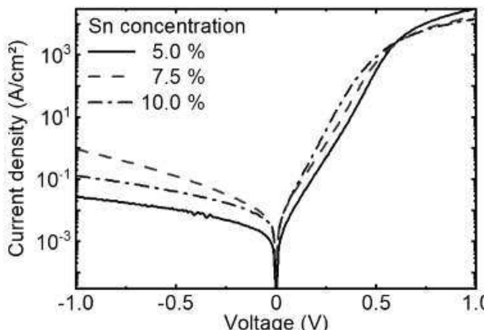

Fig. 3. JV characteristics of SiGeSn diodes of varying composition with a mesa radius of 5 µm

Afterwards, we performed CV measurements on the fabricated SiGeSn pin diodes to determine the indirect bandgap in dependence of its composition. At this point, the CV intercept method [11] allowed the extraction of the built-in voltage V_{bi} of the characterized pn junction. According to the schematic band diagram, as it can be seen in Fig. 4, the bandgap can be calculated using V_{bi} and the gaps between the fermi-level and the corresponding band edge in the n-type and p-type doped region $\Delta E_{F,n}$ and $\Delta E_{F,p}$.

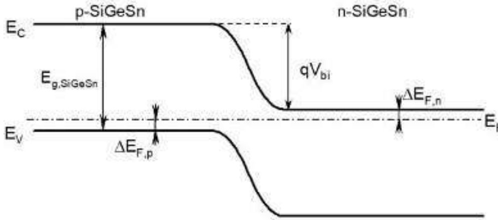

Fig. 4. Schematic band diagram of a SiGeSn pn junction

This leads in the next step to eq. (1), which was used for the calculation of the bandgap $E_{g,SiGeSn}$.

$$E_{g,SiGeSn} = qV_{bi} + \Delta E_{F,p} + \Delta E_{F,n} \quad (1)$$

In order to the calculate $\Delta E_{F,n}$ and $\Delta E_{F,p}$, the effective density of states in the valence band $N_{V,SiGeSn}$ as well as the conduction band $N_{C,SiGeSn}$ has to be known for SiGeSn. Therefore, we made a first-level approximation of the effective masses of SiGeSn using Vegard's law, resulting in the values for $N_{V,SiGeSn}$ and $N_{C,SiGeSn}$ in dependence of the SiGeSn composition. All results are summarized in Table I.

Table I. Results for the effective density of states $N_{C,SiGeSn}$ and $N_{V,SiGeSn}$ and the bandgap $Eg_{,SiGeSn}$ of SiGeSn.

Parameter	Sn concentrations			Unit
	5.0	7.5	10.0	
$N_{C,SiGeSn}$ (cm^{-3})	1.10	1.15	1.18	10^{19} cm^{-3}
$N_{V,SiGeSn}$ (cm^{-3})	4.88	5.44	5.88	10^{18} cm^{-3}
$E_{g,SiGeSn}$ (eV)	0.797	0.807	0.514	eV

4. Conclusion

We successfully performed the growth and fabrication of SiGeSn pin diodes, which were then used for the determination of essential material parameters of Ge lattice-matched SiGeSn. In our contribution, we present first experimental data for the indirect bandgap of SiGeSn and give an outlook how SiGeSn diodes can be utilized for the extraction of further material parameters, such as the direct bandgap or the band offsets.

Acknowledgements

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Monolitically integrated GaAs/Ge/Si visible-infrared photodetector

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1. Introduction

Sensors for Hyperspectral Imaging System (HSI) into the short wavelength infrared SWIR spectral region (up to 1.6 µm) is a fundamental tool to add depth of information to each pixel of the image via high resolution measurement of the electromagnetic spectrum emitted from the object under observation.

Measuring the spectral characteristics of the image makes possible to identify objects with greater precision, to perform remote chemical analysis of objects or to identify pathologies.

The HSI, performed by satellite or unmanned aerial vehicles, can be used to monitor emissions and chemical or plastic contamination of waters and fields, crop development and health and to detect the chemical composition of plants.

On a smaller dimension, HSI can be used for the early detection of human diseases and the prevention of these through a real-time monitoring of the degree of contamination of food and crops.

A relevant application taking place is the augmented reality support for surgery, where the cancer tissue can be highlighted to the surgeon due to its different spectral fingerprint, especially in the SWIR band.

2. Contents

The aim of this abstract is the presentation of a new compact and efficient dual band detector with extended spectral sensibility in the VIS and SWIR bands.

Within this approach it will be possible to obtain images with a high spatial and spectral resolution, with the same field of view, in an extremely wide spectral range, from 440 to 1660 nm.

This certainly represents a step forward compared to many current hyperspectral systems limited to 1 µm wavelength due to the use of Si based detectors or constituted by different focal plane arrays for the different spectral bands.

As a consequence, these systems, besides being bulky and heavy, present great challenges in terms of signal synchronization of the different channels.

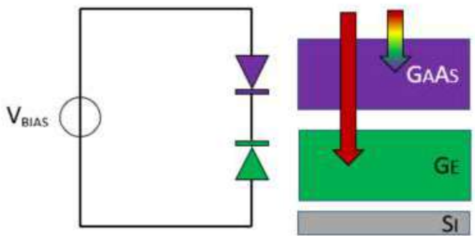

Fig. 1. Principle of operation of the back-to-back GaAs/Ge/Si photodiode. The light coming from the top is measured by the GaAs diode, while the SWIR wavelengths are measured by the Ge diode only.

The active layer of the detector is based on a GaAs thin film monolithically grown on a Ge-on-Si substrate.

The Ge layer constitutes the SWIR sensitive material, while the VIS is absorbed by the GaAs thin film. The two photosensitive layers are structured as "back-to-back" photodiodes, allowing the separate selection of each spectral band simply by switching the polarity of the externally applied bias voltage (see Figure 1).

The VIS component of the light coming from the top is measured by the GaAs diode for an applied positive bias, while under negative bias the SWIR wavelengths are measured by the the Ge diode and the GaAs is working as passive filter for the VIS light (Figure 1).

3. Device growth and processing

The samples were grown on Si(001) substrates, misoriented by 6° toward [110] to prevent the formation of anti-phase domains (APDs). APDs result

from the different step heights of (001)-oriented Si and GaAs crystals. Their nucleation can be suppressed by suitably off-cut Si substrates exhibiting majority of double layer steps.

The growth is performed in two steps.

The deposition of Ge was carried out in a Low-Energy Plasma-Enhanced Chemical Vapor Deposition (LEPECVD) tool [1,2]. One layer of Ge-i of 1 µm and one of Ge-p of 100 nm were deposited. Six cycles of thermal annealing between 600-780°C were performed to improve the crystalline quality. The Ge thin film serves as the SWIR sensitive layer and as a virtual substrate for the subsequent III-As deposition

The wafer was then moved into a Molecular Beam Epitaxy equipment where the III-As growth was performed [3,4]. An initial layer of 10 nm GaAs-p was deposited followed by a layer of 30 nm $Al_{0.8}$GaAs layer. Finally a structure with 100 nm of GaAs-p, 1 µm of GaAs-i and 700 nm of GaAs-n were grown.

The thickness of the different layers was carefully selected by running simulations in order to minimize the cross-talk between the two diodes and to optimize the absorption of each diode.

In Fig. 2 we report the results of the simulation performed in order to study the effect of the GaAs thickness on the responsivity. By increasing the thickness of the deposited GaAs the responsivity of the GaAs diode is increasing fast for an applied positive bias and is decreasing for negative bias, while the responsivity of the Ge diode is slowly decreasing for negative bias. The selected thickness is a trade-off in order to have good responsivity from both diodes and for the suppression of cross-talk between the two diodes.

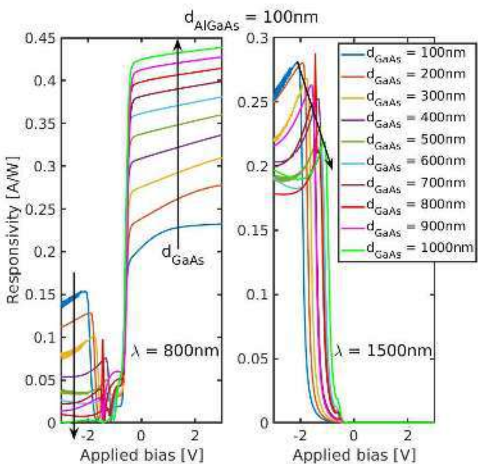

Fig. 2. Simulations showing the effect of the total thickness of GaAs absorber on the responsivity of GaAs and Ge diodes (left and right panel, respectively) at given wavelength.

The device was finally fabricated using standard micro-fabrication techniques. The single device was defined by UV optical lithography and etching.

The top contact has been realized by the deposition of an Au/Ge/Ni metal stack on the n-GaAs layer followed by an annealing at 420 °C for 5 minutes. The bottom contact was made by an Ti/Au metal stack directly deposited on the n-type Si substrate.

4. Measurements

Photocurrent measurements were performed by shining light on the device and reading the generated photocurrent. A monochromator was used to scan wavelenght between 600 and 1600 nm.
It is possible to see in Fig 3 that by changing the applied voltage on the device, the photocurrent generated is collected only from the Ge (-1 V) or from the GaAs (+1 V).

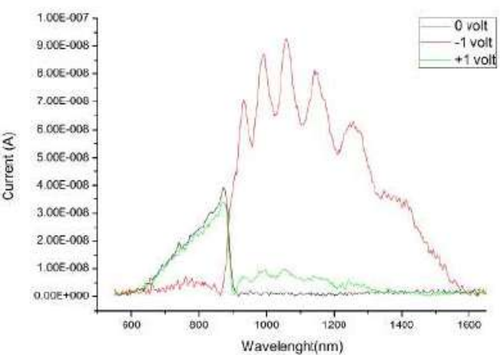

Fig. 3. Photocurrent generated by the device illuminated by light radiation at different wavelength for three different voltages (black, red and green line at 0, -1 and +1 V, respectively)

5. Conclusions

The results obtained show that the Ge/GaAs material stack can detect light in the VIS-SWIR spectral region and that the two spectral channels can be separately acquired just by switching the sign of the bias voltage applied to the device.

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Tellurium-hyperdoped Si for infrared optoelectronics

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1. Introduction

Deep-level impurities, such as chalcogens, even transition metals, entered the research interest for doping Si to extend its infrared photoresponse [1]. If a reasonable amount of chalcogen ions are doped into Si, they will form an impurity band, permitting the absorption of light below the Si bandgap. This additional absorption in the infrared range brings Si, the prevalent semiconductor, two new functionalities. One is a further increase in solar cell efficiency by building a tandem cell [2] and the second is for building all-Si-based photonics working in the telecommunication wavelength range [3]. Compared with shallow dopants, such as B, P, Chalcogens, S, Se, and Te, have much lower solubility in the order of 10^{16} cm^{-3} in thermal equilibrium Si. To form an impurity band, the doping concentration should be in the range of 10^{19} – 10^{20} cm^{-3}. Doping markedly exceeding the thermal equilibrium limit is often termed hyperdoping.

In this work, we report on the preparation of Te-hyperdoped Si. The hyperdoped Si layers are homogeneous, do not show cellular breakdown, and have a flat surface. Based on the obtained materials, we demonstrate a room-temperature mid-wavelength infrared Si p-n photodiode working in photovoltaic mode. The fabricated photodiode exhibits enhanced performance, e.g. regarding spectral photoresponse, specific detectivity, bandwidth and response speed. Moreover, inherited from the high free carrier concentration, mid-infrared-localized surface plasmon resonances (LSPR) are also observed in hyperdoped Si. We show that the mid-infrared LSPR can be further enhanced and spectrally extended to the far-infrared range by fabricating two-dimensional arrays of micrometer-sized antennas on a Te-hyperdoped Si chip. Since Te-hyperdoped Si can also work as an infrared photodetector, we believe that our results will unlock the route toward the direct integration of plasmonic sensors within a one-chip CMOS platform, greatly advancing the possibility of mass manufacturing of Si-based infrared photonic systems.

2. Experiments and results

Double-side polished Si (100) wafers (intrinsic or p-type, boron-doped, $\rho \approx$ 1-10 Ωcm) were implanted with Te ions at different fluences at room temperature. The Te depth profile was calculated using SRIM code and then verified by Rutherford backscattering spectrometry. A combined implantation at different energies varying from 50 keV to 350 keV was applied to obtain a uniform distribution of Te within the implanted 100-200 nm. The Te concentration was varied from 0.5 at.-% to 2.5 at.-%. Subsequently, the ion-implanted samples were molten using a pulsed XeCl excimer laser (Coherent COMPexPRO201, wavelength of 308 nm, pulse duration of 28 ns) in ambient air, or annealed by a flash lamp in flowing N_2. Both annealing approaches allow for Te concentrations beyond the solid solubility limit while preserving the epitaxial single-crystal growth.

Figures 1 and 2 shows the key experimental results. After pulsed laser melting or flash lamp annealing, the implanted Si layer is well recrystallized. Te impurities are found to mostly substitute the Si lattice position. Optical absorption is extended beyond 2 µm. The carrier concentration is as high as 8.3×10^{20} cm^{-3}. A plasma frequency ω_p of around 1880 ~1630 cm^{-1} is also observed. These results are published in references [4-7].

3. Conclusions

By ion implantation and sub-second annealing, it is possible to dope Si with tellurium, a kind of deep-level impurity, up to a few atomic percent. The obtained materials have enhanced optical response in the mid-infrared wavelength range. We have demonstrated a prototype photodetector and mid- and far-infrared localized surface plasmon resonances. These results broaden the Si-based optoelectronic applications to the infrared regime.

Acknowledgements

We would like to express sincere thanks to the ion beam center and the Nano-Fabrication group at HZDR. M.W. and M. S. S. thank for the financial support by the Deutsche Forschungsgemeinschaft (DFG) (grant No. WA4804/1-1).

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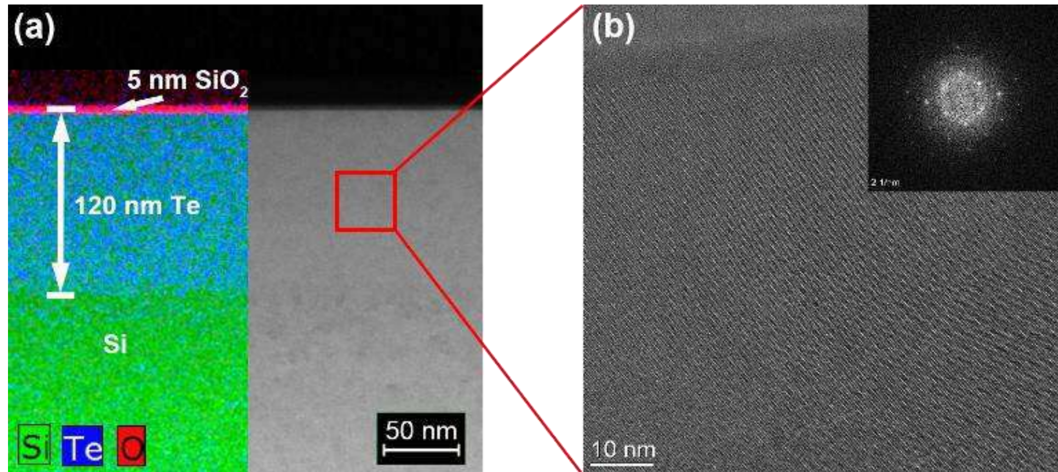

Fig. 1 (a) Cross-sectional HAADF-STEM image superimposed with the corresponding EDXS element maps (blue: tellurium, green: silicon, red: oxygen) for the PLM-treated Te-hyperdoped Si layer Te-1.5%; (b) representative HRTEM image with corresponding fast Fourier transform (inset) for a field of view as depicted by the red square in image part (a) [ref. 4].

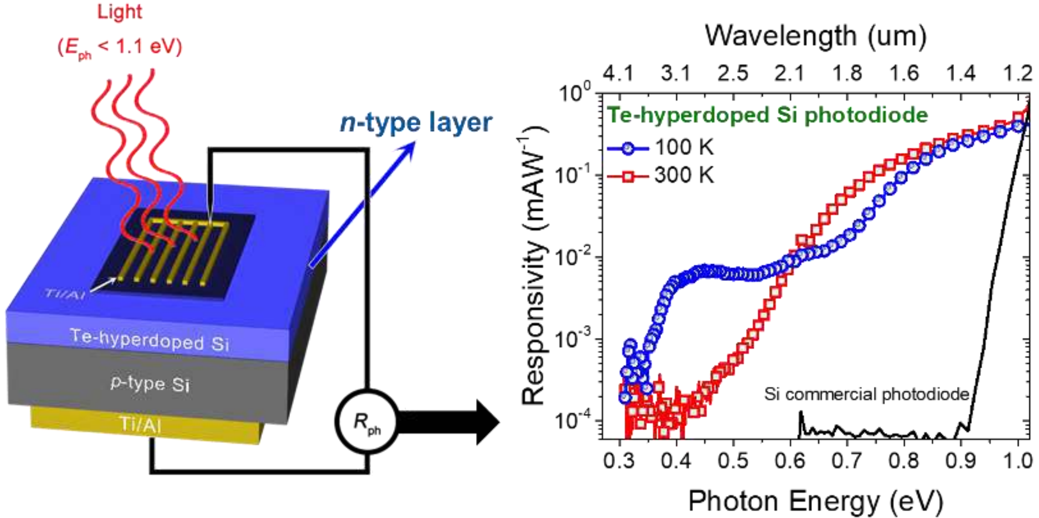

Fig. 2 The schematics of photodiode based on Te-hyperdoped Si and its spectral responsivity measured at zero bias (i.e. photovoltaic mode). The room temperature data for commercial Si PIN photodiode is shown for comparison.

Integrated Ge LED for cryogenic quantum applications

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1. Introduction

For the high-volume manufacturing of photonic integrated circuits, it is important to fabricate efficient CMOS compatible optical emitters [1]. Furthermore, the need for integrated optical quantum information processing chips is increasing. For the realization of such chips, an integrated optical source is needed [2]. As current single photon sources are working in a cryogenic environment, integrable, optical pump sources operating at those temperatures are needed. Due to the lack of phonons, efficient light emission is only achievable in direct semiconductors. Nevertheless, it is also possible to manipulate indirect semiconductors to get direct band gap behavior. Feasible approaches to get such direct behavior with Ge are applying tensile strain in combination with high n-type doping or adding a high amount of Sn to Ge to lower the offset of the direct (Γ-Valley) and indirect (L-Valley) conduction band (CB) [3, 4, 5, 6]. The approach used in this paper is to inject electrons into the direct CB by direct tunneling from the valence band (VB) into the direct CB [7].

2. Samples and fabrication

The layer stacks shown in Table I are grown on p^- Si (100) substrates in a 6-inch Molecular Beam Epitaxy (MBE) system. To grow relaxed Ge layers with a low threading dislocation density on Si, an annealing step is performed after the growth of the first 100 nm of Ge, as described in Ref. [8]. To maintain a sharp PN tunneling junction, all temperatures used in the fabrication process are kept below 250 °C. Patterning of the mesa, oxide windows, and metallization is done by contact lithography using the i-line of a Hg-vapor lamp. The mesa and metallization are structured via inductive-coupled plasma reactive ion etching (ICP-RIE) with HBr as process gas. For the passivation, a SiO_2 layer is deposited using plasma-enhanced chemical vapor deposition (PECVD). Oxide windows are opened with an RIE process using CHF_3 followed by a buffered HF etch. As metallization sputtered Al is used.

3. Tunnel Injection for direct behavior Ge-LED

Most of the radiative recombination in Ge-light emitting diodes (LED) results from scattering of electrons from the indirect CB into the direct CB, as illustrated in Fig. 1. Due to a higher phonon density, the light emission gets stronger when increasing the temperature, Fig. 2. This is a typical behavior for indirect materials. To improve the device performance for lower temperatures, a high electron population in the direct CB is essential. This can be achieved by tunneling of electrons from the VB into the direct CB, called direct band-to-band tunneling (direct BTBT) as described in Ref. [9, 10]. Due to the small energetic difference between the Γ- and the L-CB, high direct BTBT rates can be reached in a Ge PN tunneling junction. As can be seen for sample 1 in Table I and Fig. 1, a PIN diode is connected to the tunneling junction with a shared n-doped region. In forward direction, this PIN diode delivers the holes necessary for the radiative recombination process.

4. Results and discussion

With the combination of the PN junction and the PIN diode we show that radiative recombination is possible with direct BTBT, as seen in Fig. 3. The PN junction in reverse bias without the PIN diode shows no emission. For sample 1, the PN junction is operated with reverse bias (Zener) and the PIN junction with forward bias. The PN junction of sample 2 and the PIN junction of sample 3 is used with forward bias. The

Table I. Layer stack grown via MBE

Sample 1 (PINP)			Sample 2 (PN)			Sample 3 (PIN)		
Material		Doping (cm^{-3})	Material		Doping (cm^{-3})	Material		Doping (cm^{-3})
200 nm	p-Si	$N_A = 1 \cdot 10^{20}$	100 nm	n-Si	$N_D = 1 \cdot 10^{20}$	100 nm	n-Si	$N_D = 1 \cdot 10^{20}$
50 nm	p-Ge	$N_A = 1 \cdot 10^{20}$	100 nm	n-Ge	$N_D = 1 \cdot 10^{20}$	100 nm	n-Ge	$N_D = 1 \cdot 10^{20}$
200 nm	n-Ge	$N_D = 2 \cdot 10^{19}$	300 nm	n-Ge	$N_D = 3 \cdot 10^{19}$	300 nm	i-Ge	
500 nm	i-Ge		400 nm	p-Ge	$N_A = 1 \cdot 10^{20}$	100 nm	p-Ge	$N_A = 1 \cdot 10^{20}$
400 nm	p-Si	$N_D = 1 \cdot 10^{20}$	50 nm	p-Si	$N_A = 1 \cdot 10^{20}$	400 nm	p-Si	$N_A = 1 \cdot 10^{20}$
Si-Substrate			Si-Substrate			Si-Substrate		

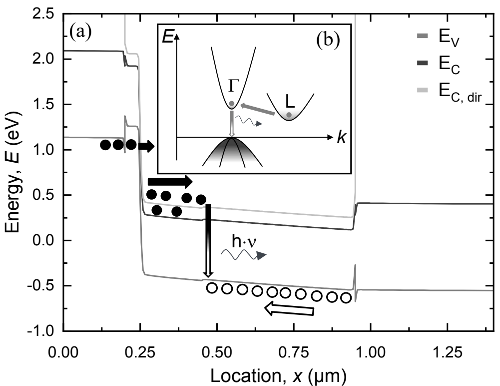

Fig. 1. Band diagram of sample 1 at a Voltage of $V = 2$ V. Inset: Band structure of Ge and scattering of electrons from the indirect CB into the direct CB

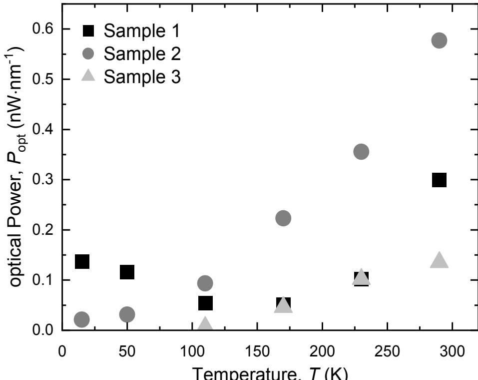

Fig. 2. Peak optical power of the emission spectra at a current density of $J = 63$ kA · cm^{-2}

temperature dependent electroluminescence measurements, Fig. 2, show a decrease of the emission power with a decrease in temperature for all three samples. This behavior is due to the indirect material properties of Ge. For different temperatures, all samples show a spectral shift of the emission peak, shown in Fig. 3, for sample 1 as a representative. The spectral shift corresponds to the temperature dependent energy band gap of Ge [11]. When decreasing the temperature below 140 K, sample 1 shows an increase of the emission power, as seen in Fig. 2. At those temperatures the tunneling rate into the direct CB increases. Additionally, scattering of electrons from the direct to the indirect CB gets reduced due to a lower phonon density. Thus, more electrons make it through the n-Ge without getting scattered, leading to a high electron population of the Γ-valley and hole population of the VB in the intrinsic Ge. This corresponds to a direct band gap behavior of the sample. Due to the PN and PIN structure, we demonstrate direct and indirect behavior in the same device.

5. Conclusion

By utilizing the tunneling effect, electrons are injected into the direct CB of Ge. Combining a PN tunneling diode with a PIN diode enables radiative recombination in Ge at cryogenic temperatures., e.g. at 15 K. This leads to the possibility of monolithic integration of Ge-LEDs on top of a Si chip to build an integrated optical source that can be used for quantum applications such as pumping Quantum dots [12, 13].

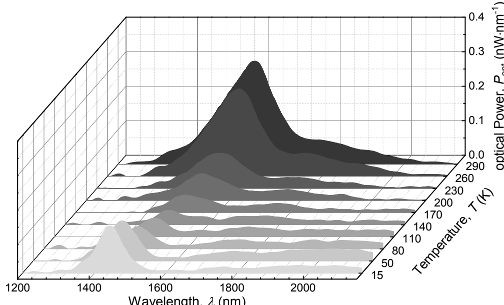

Fig. 3. Emission spectra of sample 1 for different temperatures

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Control of Schottky Barrier Height at Metal/Polycrystalline Ge Interfaces with Fermi-Level Pinning Alleviation

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1. Introduction

Ge is an attractive material to fabricate complementary metal-oxide-semiconductor devices because of its high carrier mobility for both electrons and holes. In addition, Ge crystal can be formed on processed Si substrates and general-purpose substrates, namely glass and plastic, because of its low crystallization temperature.

We developed an advanced solid-phase crystallization (SPC) technique using a densified amorphous Ge precursor and updated the Hall hole mobility of poly-Ge to 690 $cm^2\ V^{-1}\ s^{-1}$ [1], [2]. Based on our SPC-Ge, we fabricated an accumulation-mode p-channel thin-film transistor (TFT), demonstrating high field-effect mobility (170 $cm^2\ V^{-1}\ s^{-1}$) [3].

For the source/drain application of an inversion-mode n-channel Ge transistor, we demonstrated low electron barrier (high hole barrier) contact on bulk-Ge using sputter-deposited transition-metal nitrides such as TiN, ZrN, and HfN [4–6]. These contacts have amorphous interlayers (*a*-ILs) contained N atoms and alleviate Fermi-level pinning (FLP) position toward the conduction band side. Recently, we applied this technique to p-type poly-Ge formed by our SPC and demonstrated rectifying characteristics of the ZrN/poly-Ge diode for the first time [7].

In this study, we investigate the *a*-IL at the ZrN/poly-Ge interface and fabricate a metal/*a*-IL/poly-Ge diode using metals with various work functions Φ_M to control the Schottky barrier height.

2. Sample preparation

We fabricated a lateral Schottky barrier diode using SPC-Ge on glass formed at 450 °C (Fig. 1). After thinning SPC-Ge, the photoresist was coated and patterned into a circular shape (200 μm radius). Then, reactive ion etching, sacrificial oxidation, and ZrN sputter-deposition were sequentially performed. Here, the rf power of ZrN sputtering P_{ZrN} ranged from 50 to 200 W. The ZrN was patterned by the photoresist removal. After the selective removal of ZrN by diluted HF, four kinds of metals, Ag, Al, Cu, and Pt, were deposited using a resistive heating or electron beam evaporation system. Finally, two concentric Al electrodes were formed using a thermal evaporation system and lift-off photolithography.

3. Results and Discussion

Figure 2(a) shows the presence of bright contrast IL between ZrN and Ge. The nano-beam diffraction pattern in Fig. 2(a) indicates that the IL is an amorphous phase. Figure 2(b) shows that the *a*-IL contains N atoms. These results suggest the formation of N-contained *a*-IL during ZrN sputter deposition.

Figures 3(a)–3(c) show that *a*-IL thickness increases with increasing P_{ZrN}. The reverse current of the Al/*a*-IL/poly-Ge Schottky diode decreases with increasing P_{ZrN}, i.e., *a*-IL thickness (Fig. 3(d)). These results suggest that thicker *a*-IL shifts the FLP position toward the conduction band side and exhibits higher hole barrier height Φ_{BP}.

Figure 4(a) shows that *a*-IL remains after ZrN removal by dilute HF and metal (Ag) deposition. As shown in Fig. 4(b), the reverse current varies with the metal species. Figure 4(c) shows the relationship between Φ_{BP} and Φ_M. The Φ_{BP} was estimated from the reverse current at 0.3 V using the Richardson constant of 40.8 $A\ cm^{-2}\ K^{-2}$ for p-Ge [8]. We estimated the pining factor S and effective charge neutral level $\Phi_{CNL,\ eff}$ at P_{ZrN} = 200 W by liner fitting for Φ_{BP}-Φ_M plot using the following equation [9]:

$$\Phi_{BP} = S(\Phi_{CNL,\,eff} - \Phi_M) + ([\chi + E_g] - \Phi_{CNL,\,eff}), \quad (1)$$

$$S = -\partial\Phi_{BP} / \partial\Phi_M, \quad (2)$$

where χ is the electron affinity of Ge (4.0 eV), E_g is the bandgap of Ge (0.66 eV). Figure 4(c) shows that $\Phi_{CNL,\ eff}$ at P_{ZrN} = 200 W shifts toward the conduction band side compared to the conventional metal/Ge interface [9]. This result is because N contained *a*-IL plays a role in FLP alleviation. The Φ_{BP} at P_{ZrN} = 50 and 100 W more significantly decreases with increasing Φ_M than that at P_{ZrN} = 200 W, likely suggesting the thinner *a*-IL provides the better controllability of Φ_{BP} by Φ_M. In the presentation, the *a*-IL thickness dependence of the S and $\Phi_{CNL,\ eff}$ will be discussed in detail.

4. Conclusion

We investigated controlling Schottky barrier height at metal/poly-Ge interface using N-contained *a*-IL formed during ZrN sputter-deposition and metals with various work functions. The *a*-IL thickness increase with increasing P_{ZrN}. The Φ_{BP} can be controlled by P_{ZrN}, i.e., *a*-IL thickness. This study will be helpful in controlling Schottky barrier height in metal/poly-Ge contacts.

Acknowledgements

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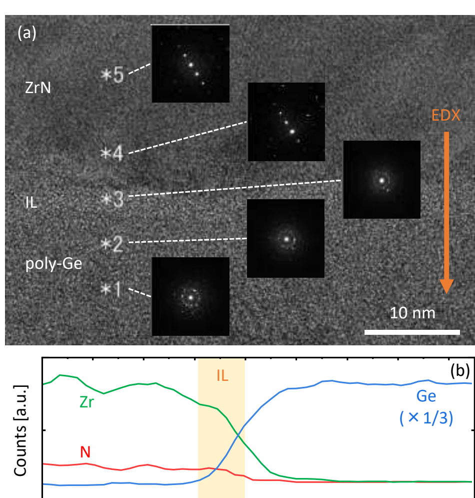

Fig. 2 Characterization of cross-sectional structure of ZrN/poly-Ge interface with P_{ZrN} = 200 W.
(a) STEM image and nano-beam electron diffraction pattern. (b) EDX depth profile of Zr, N, and Ge along the arrowed line in (a).

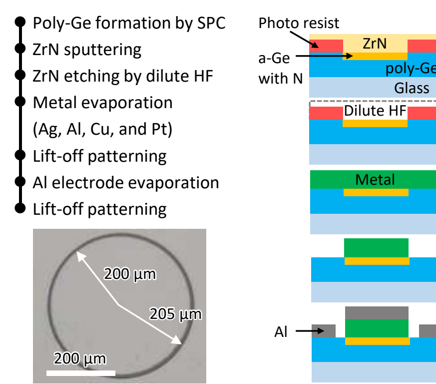

Fig. 1 Sample preparation procedure.

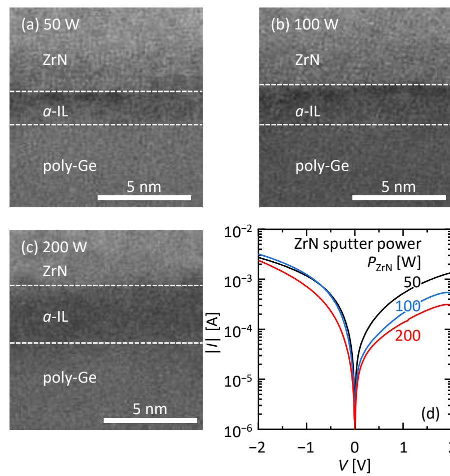

Fig. 3 P_{ZrN} dependence of (a)–(c) cross-sectional TEM images of ZrN/*a*-IL/poly-Ge structures and (d) *I-V* characteristics of Al/*a*-IL/poly-Ge Schottky diodes.

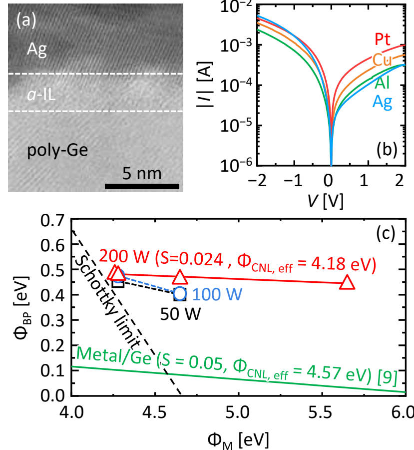

Fig. 4 (a) Cross-sectional TEM image of Ag/*a*-IL/poly-Ge structure and (b) metal species dependence of *I-V* characteristics of metal/*a*-IL/poly-Ge Schottky diode, where P_{ZrN} = 200 W. (c) Relationship between Schottky hole barrier height Φ_{BP} and metal work function Φ_M.

Nano-Ridge Engineering - a Versatile Approach for Integration of III-V Devices on 300 mm Silicon

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1. Introduction

Nano-ridge engineering (NRE) [1, 2] is a novel approach to monolithically integrate III-V devices on Si without needing thick strain-relaxed buffers or expensive (native) substrates followed by a complex transfer process. Starting from selective area growth (SAG) of III-V alloys on trench-patterned Si substrates, the heteroepitaxial growth continues outside of the pattern to increase the III-V volume. A nano-ridge (NR) with a specific shape is engineered for a particular III-V device integration scheme on 300 mm Si wafers in a cost-efficient way while profiting from an advanced and mature industrial tool park.

2. Discussion

NRE begins with SAG of III-V alloys by metal-organic vapor phase epitaxy on Si substrates with a nano-scaled Si/SiO_2 pattern of trenches. Their high aspect ratio (AR, i.e. height/width) guarantees efficient blocking of misfit defects introduced by the lattice mismatch between III-V and Si [3]. With NRE the NR volume can be expanded outside of the trench while maintaining a low defect density. The NR shape is controlled by the growth conditions which determine the growth rate hierarchy of the different NR facets. Examples are shown in Fig. 1 for various III-V alloys [2, 4, 5, 6,]. The III-V material is nucleated on Si {111} facets at the bottom of the trench, which facilitates relaxation via generation of a 60° misfit dislocation (MD) array. The example in Fig. 2 is that of an InAs NR on Si. Where the {111} facets meet a 90° MD is formed.

An electron channeling contrast imaging study of the threading dislocation (TD) and planar defect (PD) densities was done for GaAs (Fig. 3) and GaSb NRs as function of underlying trench width (i.e. screening of AR for fixed oxide thickness). For decreasing trench width (increasing AR) a TDD << 10^6 cm^{-2} can be achieved, enabling the fabrication of NR devices.

The first device demonstration was of an optically pumped $In_{0.2}Ga_{0.8}As/GaAs$ multi-quantum well (MQW) distributed feedback laser [7]. An InGaP cap layer around the device reduces non-radiative surface recombination and improves carrier confinement whereas a grating etched in the top GaAs layer creates the optical feedback for lasing (Fig. 4). The emission wavelength was recently extended from 1030 nm to 1300 nm using $In_{0.45}Ga_{0.55}As/In_{0.25}Ga_{0.75}As$ MQW NRs [8]. The nano-scale size of III-V NRs and their vicinity to silicon opens the possibility of evanescent coupling of laser light into a Si/SiO_2 waveguide (Fig. 5), clearly a beneficial concept for photonic integrated circuits [9]. Applying p-i-n doping in the GaAs regions of an $In_{0.2}Ga_{0.8}As/GaAs$ MQW NR leads to the fabrication of photodetectors with a record low dark current [10].

For next generation 6G applications (operating frequencies above 100GHz) there is a need for a mature and upscaled III-V technology to enable hybrid III-V/CMOS technology to lower power consumption while reducing footprint. An InP HBT as power amplifier will be key here. To accommodate a high current the NR size needs to be further increased and requires a double-oxide pattern to reduce sidewall deposition (Fig. 6) [11]. The first NR devices were InGaP/GaAs HBTs with a performance like a reference structure grown on a 2-inch GaAs substrate [12]. Layout of a processed III-V NR HBT monolithically integrated on Si is shown in Fig. 7.

3. Conclusion

Nano-ridge engineering is a novel and versatile technique enabling the monolithic integration of III-V materials on Si for various device applications.

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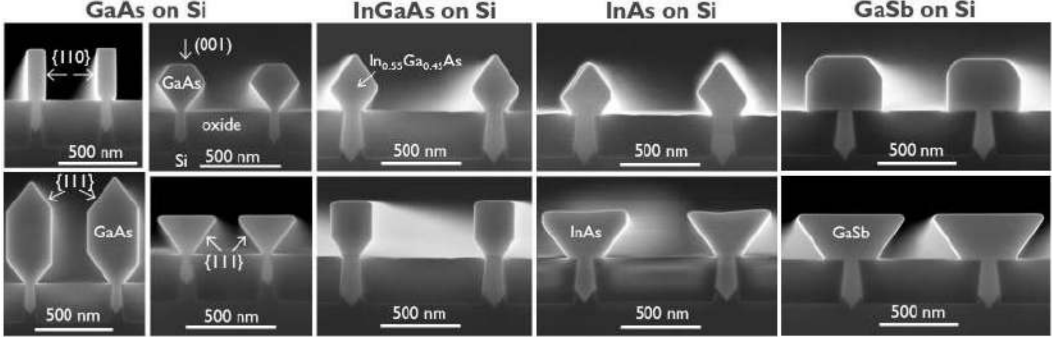

Fig. 1. Cross-section SEM images of (left to right) GaAs [2], InGaAs [6], InAs [4] and GaSb [5] nano-ridges on silicon.

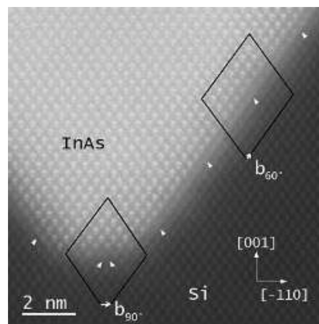

Fig. 3. HAADF-STEM image of the InAs/Si interface with Burgers circuit and projection of the Burgers vector for 60° and 90° dislocations and position of the extra {111} planes [4].

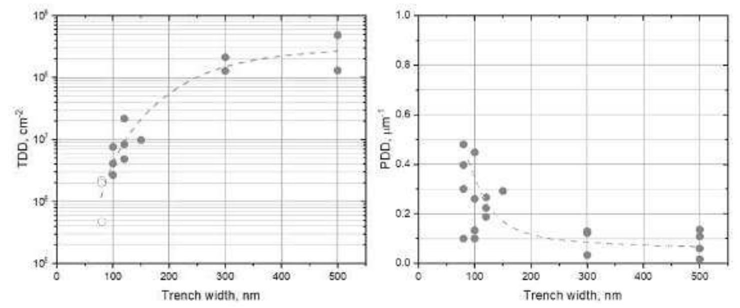

Fig. 2. (left) Threading dislocation density (TDD) and (right) planar defect density (PDD) of GaAs NRs as function of underlying trench width based on electron channeling contrast imaging (ECCI). Open data points: if no TD was found the value represents an upper limit defined by the total investigated NR surface area [5].

Fig. 6. HAADF-STEM image of an InP HBT in a double-oxide pattern. On the left the contrast is changed to clearly show the second oxide layer [11].

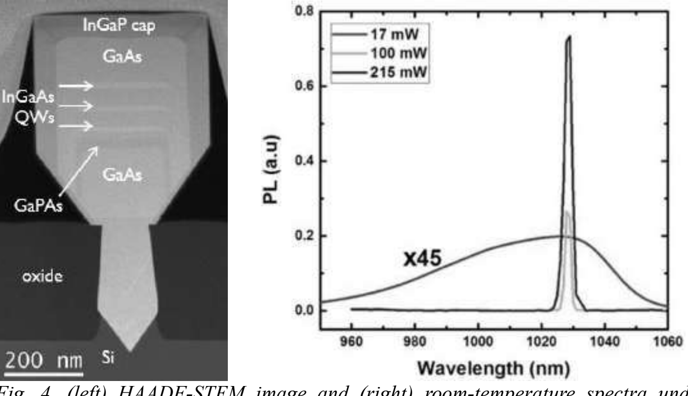

Fig. 4. (left) HAADF-STEM image and (right) room-temperature spectra under different pump powers of an optically pumped $In_{0.2}Ga_{0.8}As/GaAs$ MQW NR laser [7].

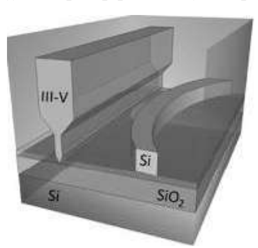

Fig. 5. 3D sketch of an advanced adiabatic light coupler [9].

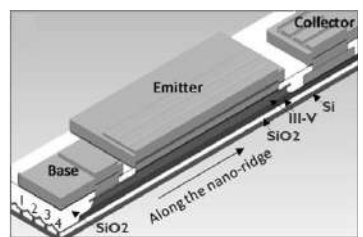

Fig. 7. Layout of a processed III-V 4-NR HBT monolithically integrated on Si [12].

Overview of Engineered Germanium Substrate Development for Opto-Electronic devices

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1. Introduction

Ge wafers are the substrate of choice for many applications. The unique properties of germanium, for example, lattice constants and small band gaps, high hole mobility, and substrate-size flexibility up to 8 inches and 12 inches, play significant roles in the development of various devices. In addition, if thin germanium foil is realized instead of thick bulk substrates, it can further accelerate the development of transistors, sensors, and other optoelectrical devices that benefit from a thin Ge thickness.

For that reason, Umicore is developing reusable Ge substrates via different routes with several partners, all based on the porosification of the wafer surface [1–6]. Shortly, the Ge substrate reuse concept is based on forming a thin Ge foil on the mother substrates. To make a detachable Ge foil, a porous structure is first formed at the surface. Through annealing, the voids in the top layer close and, when meeting the correct aspect ratios or porosity gradients, a thin monocrystalline, epi-ready Ge foil is formed. Depending on the required Ge thickness, optionally, the Ge top layer can be thickened through Ge epitaxy. Next, the III-V solar cells are grown by MOCVD and processed. Finally, the cells are detached from the mother substrates. After surface reconditioning, the mother substrate is ready for a next round.

2. Results

As shown in Table 1, three different routes were investigated to fabricate first Ge-on-Ge engineered substrates. The Ge-on-Nothing (GeON) concept is based on a lithography and dry-etch patterning process and mainly serves for the proof-of-concept and as reference, since the restructuring starts from a perfectly ordered structure. The two other routes are based on electrochemical Porosification [5,7] and are investigated for their large-scale mass production capability. The difference between the two lies in the structure of the porous stack: in the first approach, a single porous Ge layer (PGe) is used followed by a mandatory epitaxy step, while in the second a bi-porous layer is used. Detailed results are summarized in Table 1.

3. Conclusions

All routes investigated were able to form large-area uniform porous layers, that could be restructured and successfully be grown on. In addition, the adhesion turned out to be strong enough to allow MOCVD growth, and still weak enough to allow for easy foil detachment after processing. Thanks to the uniform peeling of the grown layers, substrate reconditioning by simple etching seems within reach. The mere fact that 3 totally different manufacturing routes yield similar outcomes proves the robustness of the concept and strengthens the conviction that this process can be successfully industrialized.

Acknowledgements

I. García from Universidad Politécnica de Madrid is acknowledged for the III-V layer growths on GeON samples. This work was financially supported by European Space Agency (ESA) with contract no. 4000129924/20/NL/FE, NSERC, Innovée. The view expressed herein can in no way be taken to reflect the official opinion of the European Space Agency and NSERC and Innovée.

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Table 1. Summary of the reusable Ge substrate development.

Approaches	Schematic process	Large area pore formation	Restructuring and Ge epitaxy	III-V epitaxy and device results	Detachment	Reconditning for reuse
GeON						
Single porous + Ge layer						
Bi porous layers						

Ge-on-Nothing as an alternative template to thin Ge wafers

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1. Introduction

Thin germanium (Ge) wafers or films are of interest for various applications such as solar cells [1], MOSFETs [2] or biosensors [3], whether they are used as a III-V epitaxy template or as an active layer with high mobility or with specific optical properties. A bottleneck is how to produce these substrates efficiently and at low-cost. We have developed a method based on the porosification of a thick Ge wafer that is reused multiple times, from which a thin film can be detached (Fig. 1). This Ge-on-Nothing (GeON) film can be tuned in terms of thickness, doping and area. However, the challenge of this approach is the fragility of the floating film when processing the device. It must adhere weakly enough to the wafer to be detachable, but strongly enough not to flake.

This work shows how the detachability of the foil can be adapted by controlling the density of pillars that connect the foil to the wafer, and how its roughness can be lowered, to fit a wider range of device processing needs.

2. Experimental

Bulk, 700-µm-thick Cz Ge wafers with 6-degree offcut to the (111) direction were patterned by deep-UV lithography and dry etching to form columnar macropores. After a dip in 2% HF they were loaded in an atmospheric-pressure chemical vapor deposition reactor, in 1 atm H_2, for various durations at 730 ºC to close the porous surface. For further thickening, the temperature was lowered down to 550 ºC and epitaxial growth proceeded from $GeCl_4$ in H_2. The bonding strength was characterized by peeling tests with Gelpak X4 foils and roughness measured with an AFM. Bonding to glass (Corning SG 3.4) was performed with adhesive 305 from Brewer Science at 200 ºC and detachment was done by lightly pushing a razor blade at the sample edge.

3. Results and Discussion

3.1. Tuning foil adhesion with pillars

Connections between the wafer and the foil can be introduced with GeON by simply modifying the pore pattern. Four types of irregularities were introduced with different pitches in the pore pattern during lithography (Fig. 2a). Eighteen combinations were tested in various processes to evaluate which density is required to survive which processes. Detachment ease, as expected is a direct function of pillar density and dimensions. It was also found that the additionally introduced pillars prevent foil collapse, and therefore enable safe fabrication and long anneals of very wide foils. A ~ 19-cm large foil was thus transferred to glass by adhesive bonding (Fig 2b).

3.2. Improving foil roughness

The GeON surface is inherently wavy, and pillars induce the presence of bumps or pits (Fig. 2b). This roughness does not impact the III-V epitaxy but it can be too high for other process steps like direct wafer bonding. As reported in [1], thickening the foil with epitaxial growth effectively reduces this waviness. Alternatively, longer bakes in H_2 can also reduce surface waviness and pillar bump heights by one order of magnitude (Fig 3).

It should however be noted that after detachment, the foil inner surface is rougher and could require polishing to remove the pillar remainders. An alternative solution for this foil side should still be investigated.

4. Conclusion

Transferrable Ge foils as large as 19-cm diameter wafers, with 1-30 µm thickness and tunable doping, have been achieved via the Ge-on-Nothing method. The advantage of this method is to enable, at design stage, the controlled inclusion of pillars connecting the foil to the wafer, to control its adhesion. Such pillars unfortunately increase its roughness, but the surface can be smoothened, if needed, with epitaxial thickening or longer bakes. The material can thus be adapted to various device requirements, such as solar cells or MOSFETs.

Acknowledgements

This work was carried out under a program of and

funded by the European Space Agency (ESA) with contract no. 4000129924/20/NL/FE. The view expressed herein can in no way be taken to reflect the official opinion of the European Space Agency. The authors also acknowledge financial support from JSPS-FWO Bilateral Joint Research Projects.

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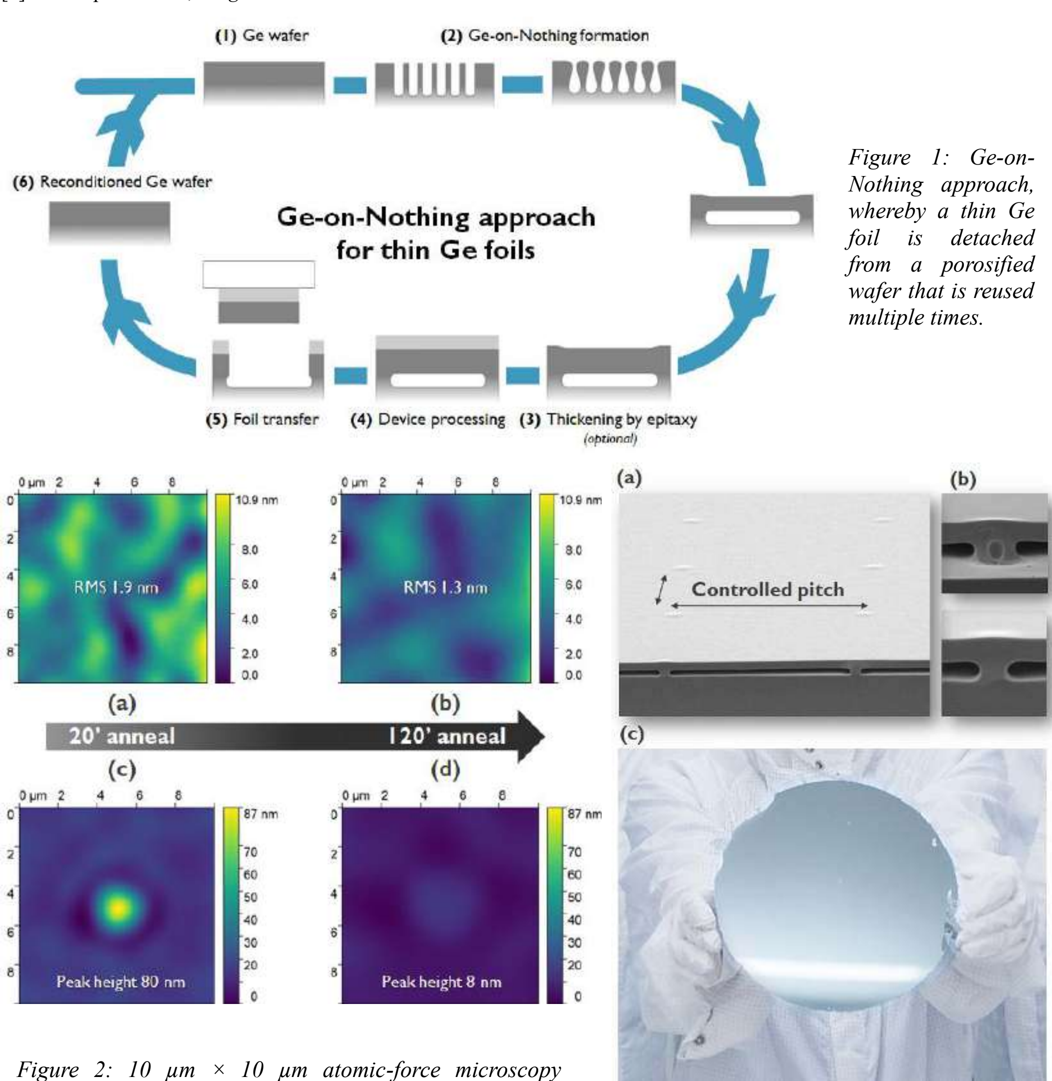

Figure 1: Ge-on-Nothing approach, whereby a thin Ge foil is detached from a porosified wafer that is reused multiple times.

Figure 2: 10 µm × 10 µm atomic-force microscopy images plotted at the same scale in pairs, showing the reduction of (a, b) surface roughness (RMS) and (c, d) pillar-bump height with increasing anneal time from 20 minutes to 2 hours.

Figure 3: (a) tilted cross-section SEM images of a GeON foil in which periodic pillars have been introduced. (b) Pillars can be made in different shapes and dimensions and leave a bump or pit in the foil topography. (c) 8-µm-thick 19-cm diameter Ge foil on glass.

Evaluation of the physical properties of Ge-on-insulator based on Ge-on-Nothing and layer transfer

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1. Introduction

Ge has received much interest due to its high carrier mobilities and bandgap suitable for near-infrared applications [1,2]. On the other hand, Ge is listed as a critical raw material and has drawbacks in terms of cost and relatively large leakage current density due to its narrow bandgap. The introduction of Ge-on-Insulator (GOI) structures therefore is appealing for the formation of advanced devices with a reduced Ge consumption. Ge layer transfer schemes combining wafer bonding and layer splitting by hydrogen ion (H^+) implantation, so-called Smart-Cut™, have been reported as a fabrication method for GOI. However, this approach suffers from the presence of high defectivity at the bonded interface, which is assigned to the H^+ implant [3]. Therefore, the GOI fabrication method is still in the fundamental research stage.

Recently, imec succeeded in the fabrication of a Ge-on-Nothing (GeON) structure based on the reorganization of macro-porous Ge at high temperature, as shown in Fig. 1 [4]. This work considers an alternative method for the fabrication of high-quality GOI. The method is based on GeON wafer bonding and layer transfer. The obtained GOI films show better optical and electrical properties than those prepared by the Smart-Cut™ approach.

2. Experiment

Figure 2 shows the GOI fabrication procedure followed in this study. The GeON is fabricated from a p-type (100) oriented Ge wafer [4]. After GeON surface cleaning, a 3 nm-thick Al_2O_3 layer was formed using ALD. In parallel, a p-type Si substrate with 50 nm-thick thermally grown SiO_2 is prepared as a bonding substrate. After surface rinse with DI water and drying by N_2 blow for both samples, the Ge and Si are bonded in the cleanroom environment. In order to enhance bonding strength, 0.3 MPa pressure is applied to the sample in the bonding vacuum chamber. The bonding is followed by an anneal at 300 °C. After these steps, the bonded GeON layer is detached by pulling the Ge substrate. The GOI layer is thinned and planarized by dry etching and CMP. The resulting GOI is characterized using micro-photoluminescence (μ-PL), Raman spectroscopy, and Hall effect. An accumulation mode back-gate MOSFET is also fabricated and characterized.

3. Results and Discussions

3.1. PL and Raman spectra

Figures 3(a) and 3(b) show the μ-PL and Raman spectra for the fabricated GOI, respectively. For comparison, bulk Ge results are also plotted. PL peaks corresponding to the direct bandgap of Ge (0.80 eV) are clearly observed. These have higher intensities than those obtained from the bulk Ge reference. In addition, signals from the indirect bandgap, around 0.7 eV, become less noticeable in the GeON spectra. The inset of Fig. 3(a) compares the results with those from GOI fabricated by the Smart-Cut™ method [3]. PL variations with respect to the measurement position are drastically reduced. Moreover, the Raman peak corresponding to GOI appears at a lower wavenumber in comparison to bulk Ge. This indicates that the GOI layer is slightly tensely strained.

3.2. Hall effect measurement

Figure 4(a) shows the depth dependence of the hole mobility (μ_p) and concentration (p). The degradations of μ_p and p, with respect to Ge thickness, are less than those obtained for the Smart-Cut™ GOI, for thin GOI in particular (Fig. 4(b)) [3]. This result suggests that the GOI fabricated from GeON has a better crystallinity than the Smart-Cut™ GOI.

3.3. Demonstration of back-gate MOSFET

The fabrication procedure of an accumulation mode back-gate p-MOSFET is shown in Fig. 5. After GOI thinning down to 67.7 nm, the active region was defined by wet etching isolation. As a source and drain, Pt electrodes were deposited by sputtering. Figures 6(a) and 6(b) show I_D-V_D and I_D-V_G characteristics, respectively. Both show typical MOSFET operation curves, illustrating that this GOI fabrication method from the GeON template can be a more straightforward way to form high-quality GOI.

3. Conclusions

A novel GOI formation scheme starting from the GeON template has been proposed. The fabricated

GOI showed better optical and electrical properties than Smart-Cut™ GOI. In addition, back-gate p-MOSFET on the GOI has been demonstrated. The proposed method has the potential to provide high-quality GOI for heterogeneous device integration.

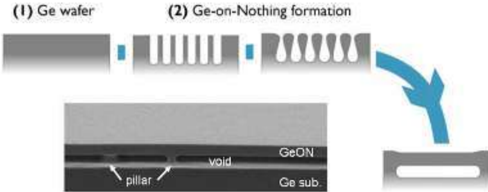

Fig. 1 Fabrication scheme for GeON and cross-section SEM image of a GeON template [4].

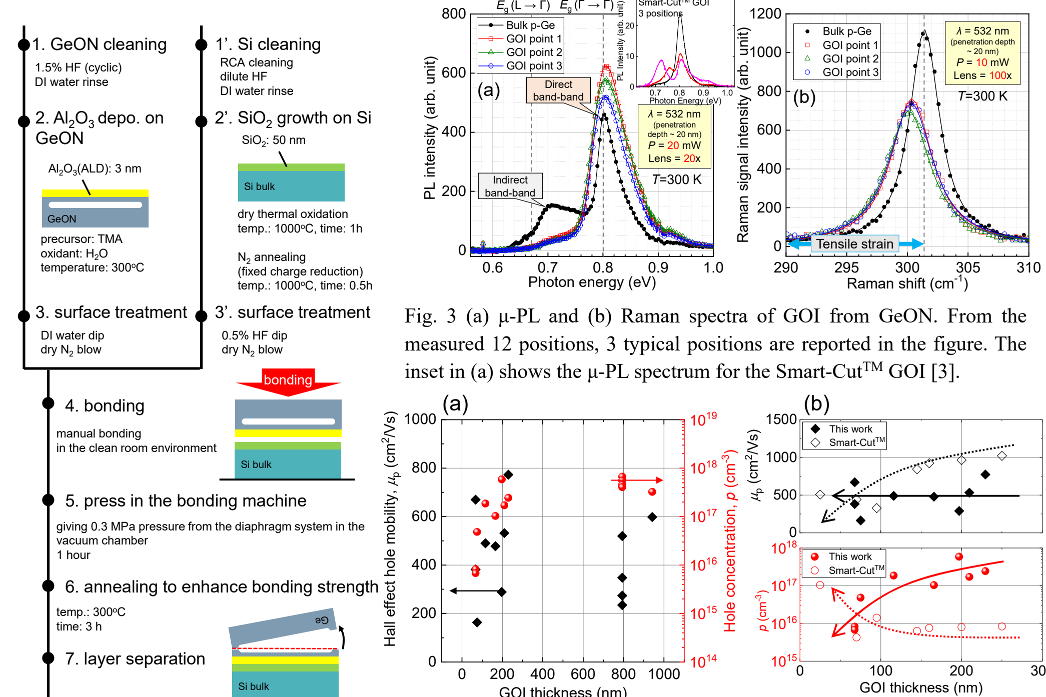

Fig. 2 GOI fabrication scheme from GeON.

Fig. 3 (a) μ-PL and (b) Raman spectra of GOI from GeON. From the measured 12 positions, 3 typical positions are reported in the figure. The inset in (a) shows the μ-PL spectrum for the Smart-Cut™ GOI [3].

Fig. 4 (a) GOI thickness dependence of the hole mobility and the concentration. (b) Comparison with the Smart-Cut™ GOI [3]. These data have been obtained by cyclic GOI thinning by dry etching and Hall measurements.

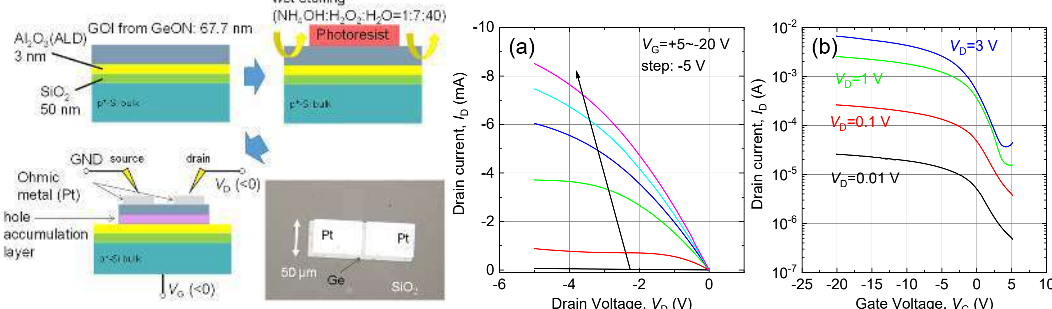

Fig. 5 Fabrication procedure of the back-gate p-MOSFET and its microscope image.

Fig. 6 (a) I_D-V_D and (b) I_D-V_G characteristics of the back-gate p-MOSFET on the GOI from GeON.

Acknowledgements

This work was partially supported by JSPS-FWO Bilateral Joint Research Projects and the Cooperative Research Project of the Research Institute of Electrical Communication (RIEC), Tohoku University. The development of the GeON template was carried out under a program of and funded by the European Space Agency (ESA) with contract no. 4000129924/20/NL/FE. The view expressed herein can in no way be taken to reflect the official opinion of the European Space Agency.

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Unravelling the growth stages on porous substrate and formation of thin detachable Ge membranes

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1. Introduction

Semiconductor-based membranes play an important role in expanding frontiers of nanoscience and technology. They offer a lightweight and a flexible format, with extra degree of freedom for implementations that cannot be matched by traditional techniques [1,2]. Multiple membranes of various dissimilar materials can be stacked on top of each other, allowing an easy coupling between their physical properties [3]. Germanium (Ge) membranes are particularly attractive for applications in high performance optoelectronics and telecommunications devices [4,5].

Various lift-off techniques such as remote epitaxy [6] or epitaxial lift-off [7] show massive potential for the fabrication of III-V materials membranes, but they are not viable for elemental materials such as Ge. Recently the Germanium-on-Nothing approach demonstrated the formation of Ge membranes using a substrate patterned with pillars followed by high-temperature annealing [8,9]. While lithography and dry etching provide an excellent control over the structure of the substrate, they increase the complexity and cost of the process. Much finer nanostructures such as porous Ge can replace the pillar pattern and enable the direct growth of the membranes. Compared to bulk materials, nanostructured substrates pose additional challenges for the epitaxial growth, due to their non-planar nature.

In this work, we shed light on nucleation and initial growth stages to understand the Ge epitaxy on porous Ge (PGe) substrate. Moreover, we study the evolution of the surface morphology during the growth to evaluate the topological quality. Finally, we demonstrate the formation of detachable monocrystalline Ge membrane, which can be easily transferred to any host substrate.

2. Results and discussions

The porous germanium (PGe) substrates are prepared using electrochemical etching of the Ge wafer [9]. This method allows to produce uniform PGe layers with low surface roughness and gives the possibility to finely tune the porosity and thickness of the nanostructure.

To study the nucleation process, Ge layers with increasing thickness are grown on top of the PGe substrate. Fig. 1 show the cross-sectional SEM images at various stages of the growth.

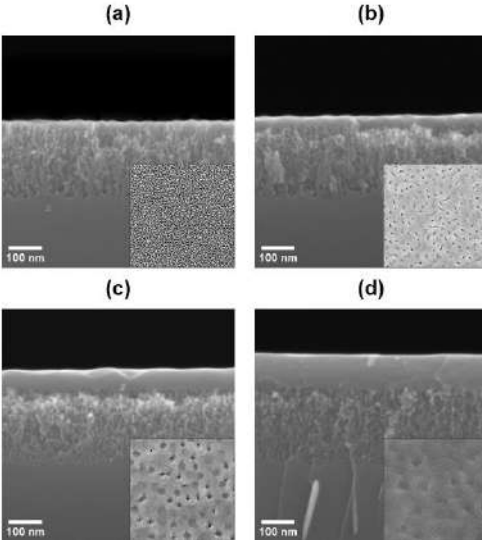

Fig. 1: Cross-sectional SEM micrographs at (a) 10 nm, (b), 30 nm (c), 60 nm and (d) 100 nm of grown Ge layer with top view SEM micrographs in inset.

The nucleation starts by the formation of 3D seeds on top of the pore walls (Fig. 1a), which continues to grow with increasing quantity of deposited material. Due to the densely packed pores, these seeds start to coalesce very early in the growth when the nuclei are only few nm in size (Fig. 1b). The coalescence is found to be completed after the deposition of 60 nm thick Ge. A complete membrane is then formed on top of the PGe substrate, with only topological defects (Fig. 1d) testifying the growth transitions from the 3D nucleation to 2D growth. This is clearly shown by the

variation of the surface roughness, which rapidly increases during the nucleation stages, spikes when the coalescence is completed and then decreases during the 2D growth as seen in Fig. 2.

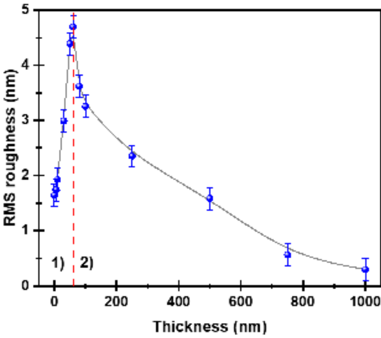

Fig. 2: Evolution of the surface roughness during all the growth stages with red dash line indicating the end of the layer coalescence.

Further growth past the coalescence enables to annihilate the topological defect and obtain a smooth surface suitable for further growth. The crystalline quality of the Ge membranes is verified by in-plane XRD measurements, demonstrating the monocrystalline nature of the layers.

Growing high-quality layers on top of the porous substrate has many advantages with the most important one being the possibility to detach the membrane from the substrate using the weak nanostructured interface. By modulation of the PGe layer's porosity the adhesion force of the membrane can be tuned to promote an easy detachment. The Ge membrane can then be transferred on a flexible substrate for further use as demonstrated by Fig. 3.

Fig. 3: Optical image of the Ge membrane transferred to flexible substrate using adhesive tape

3. Conclusions

In this work, we experimentally investigated the initial growth stages of the Ge epitaxy on porous structures starting with nucleation of 3D seeds on top of the pores that slowly grow and coalesce to form a 2D layer. We show that detachable thin Ge membranes with thickness below 100 nm can be successively grown. The adhesion force of the membrane can be adjusted by tuning the porosity of the substrate. These finding give a general understanding of the Ge growth on PGe substrate and provide a steppingstone for the fabrication of high-quality Ge membranes and their applications in flexible optoelectronics.

Acknowledgements

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Low-Temperature Germanium Condensation process on SOI for sensing applications

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1. Introduction

In the microelectronic industry, c has been used since the beginning of the 21st century. To overcome the limits of classical transistor architecture and proceed the miniaturization of electronic components, this technic contributes to significant improvements in device performances. Playing on the mechanical constraints of the crystalline layers change their electronic properties [1]. In particular, the mobility of electrons in silicon (Si) N-FET MOSFETs can be improved by applying a strain to the channel, for example by using Carbon doped silicon in source/drain regions. Radio Frequency (RF) devices using Silicon-on-insulator (SOI) substrate can present sufficiently improved characteristics to be largely competitive with III-V materials, if the channel is constrained [2]. In these RF-SOI switches, the stress is applied during the epitaxy process, which consists in depositing by chemical vapor deposition (CVD) a perfectly monocrystalline layer, without defects and whose crystalline planes are completely corresponding to those of the substrate [3–5]. The epitaxial layers can be doped or elemental Si or alloys such as SiGe or Si-C which make it possible to modulate the stress. Such structures are commonly used in BiCMOS and advanced CMOS technologies [3,4].

A specific Si-Ge heteroepitaxy technic, inducing strain engineering has been developed in 2001 by Tezuka *et al.* [6]. It consists in a dry oxidation of a low Ge concentrated SiGe layer, in epitaxy on a silicon wafer. During the process, the silicon preferential oxidation induces a migration of the germanium atoms in the underlying layers. This germanium enrichment of the SiGe layer is named germanium condensation processed. Its major interest lies in the fact that the obtained structures do not present structural defects, while they are much thicker than those which could be obtained by co-deposition technics. However, most of the studies proceed at high temperatures (T > 1000°C), and for final germanium concentration higher than 50 %, a high density of defects is generated [7]. Therefore, the challenge consists in producing high Ge concentration in condensed layers, without structural defects.

2. Results

2.1. Low temperature Ge condensation

Our team has developed an original germanium condensation process at low temperature. We have evidence a thermic threshold: below 900°C, the germanium diffusion is limited, leading to a specific germanium concentration in the germanium-rich layer [8]. By playing on initial SiGe concentration and condensation time, it is then possible to adjust the Ge-rich layer thickness [9].

Moreover, the germanium diffusion is stopped by silicon oxide. We demonstrated that Silicon On Insulator substrates can be used to overcome the germanium concentration limit of the germanium-rich layer (see Fig. *1*). Finally, thin SiGe layers (up to few monolayers) of controlled composition and strain have been achieved [10].

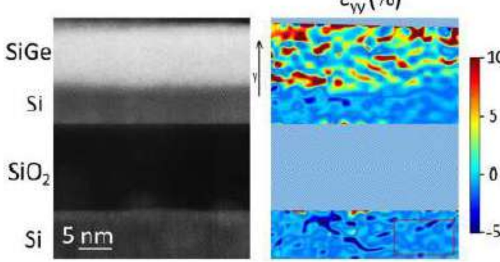

Fig. 1. HRTEM image of a SiGe condensed layer on SOI (left) and its Geometric Phase Analysis confirming the lattice deformation due to perfect heteroepitaxy (right) *[9]*.

2.2. Strain relaxation

The microelectronic industry is also interested in GOI and SGOI substrate. The condensation process would allow the realization a defect free relaxed SGOI layer under industrial conditions on a 300mm wafer. It would provide a new method for applications

such as optical or the growth of tensile Si channels. However, the strain originating from the condensation must be relaxed first. We propose to use the mechanical properties of Ge-O bonds: as they are weaker than Si-O bonds, slippage is observed at the SGOI/Buried Oxide (BOX) interface. Therefore, relaxation phenomenon has been observed on specific Silicon-Germanium On Insulator (SGOI) structures [11].

We will show that finely tuning the temperature of the condensation and subsequent annealing steps drastically modifies the relaxation processes of the SiGe layer. Another major player is the viscoelasticity of the silicon oxide: at high temperature the viscous flow of SiO_2 allow the local swelling of the embedded SiGe layer and its relaxation [2,12].

3. Conclusions

This work demonstrates that germanium condensation is a phenomenon, that can be tuned for new applications in the microelectronic industry. Thickness, germanium concentration and strain are key parameters that can be adjusted by fine tuning of the process. Moreover, when operated on SOI, on can take advantage of the BOX: the SiO_2 layer can serve as an efficient compliant substrate for strain engineering.

Acknowledgements

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Epitaxial growth of detachable Ge and GaAs/Ge membranes on mesoporous Ge substrate with the PEELER process

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1. Introduction

Recently, the epitaxial growth on porous Ge (PGe) substrate[1] has attracted a lot of interest, especially for the fabrication of large scale detachable[2] low-cost and lightweight high-performance solar cells[3,4] and substrate reuse[5]. Indeed, for III-V/Ge solar cells, the Ge substrate thickness is conventionally around 180 µm, whereas only a few µm[6] would be sufficient to ensure full cell's performance. Additionally, most of the cell weight comes from the substrate[7] which is very challenging for space application.

In this work, we demonstrate by the Porous germanium Efficient Epitaxial LayEr Release (PEELER) approach, the epitaxial growth of high-quality Ge and GaAs/Ge membrane on porous Ge substrate for detachable III-V materials based solar cells. As illustrated in Fig. 1, PEELER process is composed of four steps: (i) Single PGe layer is formed on top of the Ge substrate. (ii) Ge buffer layer is deposited at low temperature (LT) followed by high-temperature (HT) annealing step to reorganize the porous layer into weak voided layer below the Ge buffer. Then, a high-quality Ge layer is grown on top to form the Ge epitaxial template. (ii-b) III-V structure or solar cell is grown on Ge template. (iii) The Ge or GaAs/Ge membrane is then mechanically detached from the substrate. (iv) Ge substrate is reconditioned by a chemical polishing step and then reused for a new cycle

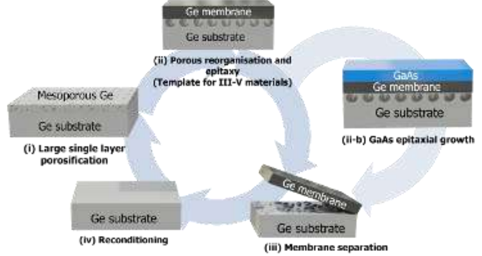

Figure 1: PEELER process

2. Results

Homogenous porous Ge layer with a medium porosity was obtained by Bipolar Electrochemical etching (BEE) on 100 mm Ge wafer. AFM measurements revealed a surface RMS roughness of approximately 2 nm[8]. Low temperature Ge buffer has been first deposited to initiate the two-dimensional layer-by-layer growth prior to the deposition of high-quality Ge at high temperature. With this two-step's growth method, a total 700 nm thick Ge epilayer has been grown. A low surface roughness below 1 nm has been measured by AFM (Fig. 1a) testifying the good morphological properties of the epitaxial Ge template. Cross-sectional SEM analysis reveals the formation of separation layer containing voids separated by pillars, as shown in Fig. 1b. Successful defect free detachment of the epitaxial structure from the parent substrate has been achieved by mechanical pull test. This demonstrates that the formed pillars characteristics fit the separation layer requirements.

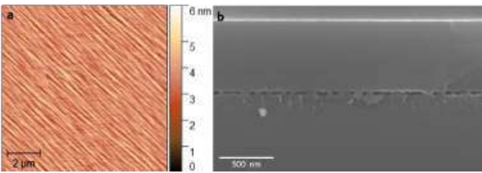

Figure 2: (a) AFM characterization of the Ge epitaxial layer surface (b) SEM cross section image of the porous structure reorganisation after epitaxy process.

To analyse the crystalline quality of the Ge epilayer, TEM characterizations were carried out. As shown in Fig 3, the deposited Ge is found to grow defect-free with high crystalline quality. The monocrystalline properties of the Ge template are shown by the similarity of SAED pattern between the Ge epilayer and the substrate. The preservation of the 6° miscut from the substrate is highly requested for the III-V material growth.

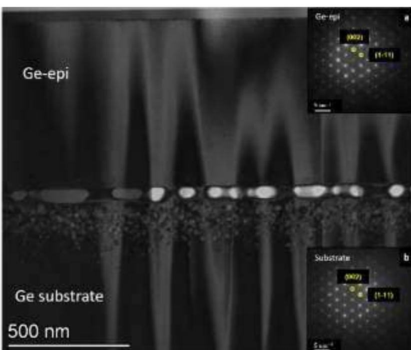

Figure 2: TEM images of the Ge epitaxial layer (a) and Ge substrate (b)

To test the viability of the Ge template on PGe for the epitaxial growth of III-V materials, 400 nm thick GaAs layer was grown at 500°C on PGe with detachable Ge template. The same growth run has also been performed on epi-ready Ge substrate for comparison. XRD measurements were carried out to investigate the epilayers quality.
Accordingly, HR XRD measurements around the (004) plan were performed. ω-2Θ rocking curves, (Fig. 4), showed separated peaks from Ge and GaAs with very similar characteristics. This indicate that the Ge template on PGe preserves the same properties as conventional Ge substrate. The Ge peak of the GaAs/Ge/PGe structure is slightly broadened compared to the reference sample and likely to attributed to the presence of the reorganized PGe.

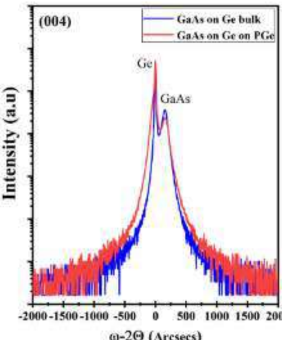

Figure 3: XRD rocking curve on (004) peak of GaAs on Ge/PGe and Ge substrate

3. Conclusion

We have successfully grown monocrystalline quality Ge template on porous Ge substrate with low surface roughness. Porous Ge reconstruction during epitaxy lead to a void layer formation allowing defect free detachment of the heterostructures from the parent substrate. The GaAs growth on the Ge template showed the compatibility of Ge/PGe structure for epitaxial growth of high-quality III-V materials and devices.

Acknowledgements

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A Review of Ge-on-Si Single Photon Avalanche Diode (SPAD) Photodetectors and Applications

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1. Introduction

CMOS single photon avalanche diode (SPAD) photodetectors are now a mature technology being used for a wide range of applications including range-finding for autonomous vacuum cleaners, facial recognition, medical imaging and prototype automotive lidar systems [1]. A SPAD consists of an absorber which generates electron-hole pairs and an avalanche gain region which amplifies the single photon into a current sufficient to be detected by electronics. SPADs are operated above the breakdown voltage of the avalanche region, in Geiger mode operation, where a single photo-generated carrier produces almost instantaneously a large multiplied current through impact ionization.

The use of Si as the absorber limits absorption of photons to ≤ 1 µm wavelength but many applications including fibre-optic based telecoms, quantum communications over fibre and range-finding / lidar over large distances (> 200 m) and/or through obscurants require longer wavelengths. InGaAs/InP SPADs operating out to ~1.7 µm wavelength have been commercially available for over a decade but at present only single pixel detectors are commercially available at significant cost (>£10k) and single photon detection efficiencies (SPDEs) of ≤ 35% are well below CMOS SPAD efficiencies in the visible region.

By added Ge heterolayers onto Si, photons can be absorbed out to ~1.7 µm wavelength enabling SPADs to be produced operating at the important short-wave infrared (SWIR) wavelengths of 1310 and 1550 nm. This review will detail some of the key steps in producing the first Ge-on-Si SPADs [2] with useful single photon detection efficiencies (SPDEs) [3][4], explain the present performance, discuss options to improve the future performance [5][6][7] and discuss requirements for key markets and applications [8].

2. Key Design Principles

All Ge avalanche photodetectors (APDs) have demonstrated photon counting applications for many years but were limited to low temperature operation due to high dark count rates (DCR) when operated in Geiger mode [9]. Si is one of the best avalanche gain materials and the indirect bandgap with a significantly larger direct gap results in efficient, low-noise avalanche multiplication [3]. Therefore the addition of SiGe or Ge as an absorber on top of a Si avalanche region in a so-called separate absorber and charge multiplication (SACM) device is the preferred approach for high performance SPADs [6].

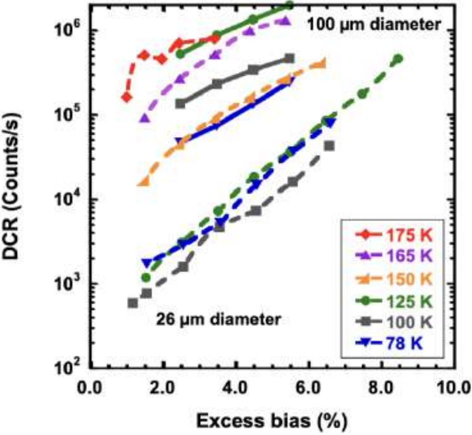

Fig. 1: The DCR as a function of temperature for 100 µm diameter (solid lines) and 26 µm diameter (dashed line) Ge-on-Si SPADs [3][4].

3. SPAD Performance

The first Ge-on-Si SPAD devices were mesa etched of 25 µm diameter and demonstrated 4% SPDE at 1310 nm when operated at 100 K with a large DCR of 6 mega-counts per second (cps) [2]. These devices were also the first SPADs to demonstrate operation at 1550 nm on a Si substrate with the indirect bandgap absorption producing 0.15% SPDE [2].

A step change in performance was obtained by moving to a planar process [3]. By locally defining the p^{++} top contact well away from any etched sidewalls, the DCR could be reduced by a factor of 40 for devices with equivalent diameters ([4] and Fig. 1). This demonstrated the importance of sidewall traps in the device performance and allowed SPDEs up to 38% at 125 K [3] (Fig. 2). A clear benefit of Group IV SPADs compared to III-V devices is reduced afterpulsing:

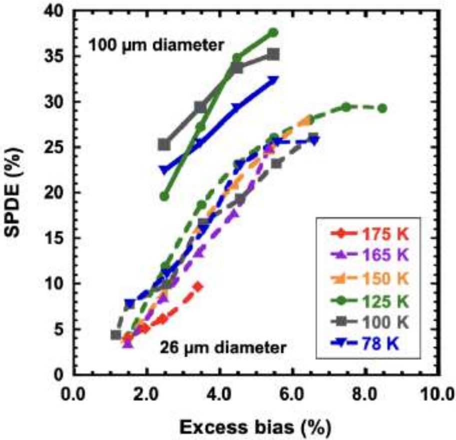

Fig. 2: The SPDE as a function of temperature for 100 µm diameter (solid lines) and 26 µm diameter (dashed line) Ge-on-Si SPADs [3][4].

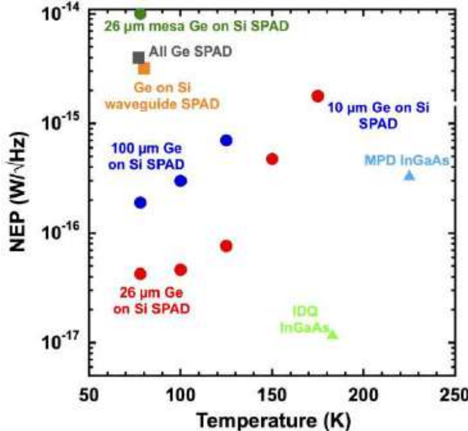

Fig. 3: The NEP as a function of temperature for a range of all Ge, Ge-on-Si and InGaAs/InP SPADs at 1310 nm [2][3][4][7][9][10].

where carriers are trapped in the avalanche region and then released at a later time. It is afterpulsing that determines the repetition rate for most applications as SPADs require long hold off times to reduce afterpulsing probabilities to a negligible level. Initial afterpulsing measurements on Ge on Si SPADs have demonstrated at least a factor of 5 reduction in afterpulsing compared to InGaAs/InP SPADs under identical operating conditions [3].

5. Comparison of SWIR SPAD Technologies

Fig. 3 compares the noise equivalent power (NEP) from the best planar Ge-on-Si SPADs with 26 µm [4] and 100 µm diameters [3] with a range of commercial InGaAs/InP SPADs and other devices [7][9][10] at 1310 nm wavelength. It is clear that signficant progress has been made with planar Ge-on-Si SPADs but further progress is required to get to the performance of InGaAs/InP SPADs at 223 K.

4. Routes to Improving SPAD Performance

All InGaAs/InP SPADs are typically run on Peltier coolers at ≥ 223 K. To date the highest operating temperature of Ge-on-Si SPADs is 175 K [4] with clear single photon detection but the DCRs at these temperatures are still high compared to III-V devices and DCR increases exponentially with increasing temperatures [6][7]. Simulations are starting to provide evidence that there are still hot spots in these planar SPAD devices which dominate the generation of DCR. It is also clear that high quality surface passivation of the deep trench isolation is essential to reducing DCR and improving the operating temperature. The present Ge-on-Si SPAD results have 1 µm of Ge which only absorbs ~50% of the photons so extending the thickness of Ge should increase SPDE and higher temperature operation will improve SPDE at longer wavelengths. Also the initial afterpulsing results suggested that threading dislocations from the Ge-Si heterointerface that thread down into the Si may dominate the afterpulsing so reducing these should allow afterpulsing values similar to those demonstrated in CMOS SPADs.

6. Conclusions

Ge-on-Si SPADs have the potential to allow far cheaper SWIR SPAD devices for a range of applications including telecoms, quantum comms., rangefinding and lidar. Already initial lidar results with Ge-on-Si SPADs have demonstrated the potential for rangefinding over 1 km with eye safe laser powers [8]. These are still early devices from an immature technology with significant potential to optimise the future performance. Simulations suggest that far higher SPDE than III-V SPADs should be achievable due to the better band-structure [4] but DCR may always be poorer [7]. The lower afterpulsing from Ge-on-Si devices may allow higher measurement repetition rates than III-V SPADs and is key for most applications.

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Strip-Width-Dependent Spectral Responsivity in a Waveguide Photodetector of Ge by Selective-Area Chemical Vapor Deposition on Si

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1. Introduction

A Ge epitaxial layer on Si has been studied as near-infrared photodetectors (PDs) and electro-absorption optical intensity modulators (EAMs) in Si photonics. A waveguide-integrated device of a narrow Ge strip structure with a lateral pin junction exhibits high response frequency over 50 GHz because of a reduced junction capacitance [1, 2]. This study reports spectral responsivity in a PD of a Ge strip structure prepared by selective-area chemical vapor deposition (CVD) on a Si-on-insulator (SOI) platform. The edge-induced lattice strain relaxation [3] induces a spectral blue shift with narrowing the strip, whereas a red shift is induced with increasing temperature. An enhanced responsivity by the Franz-Keldysh (FK) effect in combination with the avalanche multiplication is also reported.

2. Experimental

Fig. 1 shows schematic structure and typical cross-sectional transmission electron microscope (TEM) image of a lateral pin PD used in this study. A strip-loaded structure of Ge in the [110] direction on a (001) Si-on-insulator (SOI) pedestal was used. In the fabrication, a lateral pin junction was formed in the SOI layer by phosphorus and boron implantations, followed by a patterning of the SOI layer to form a Si channel waveguide (WG) connected to the pedestal. Then, a selective CVD growth of a Ge strip (200 nm in thickness) was performed on the pedestal. The strip length was 40 μm, while the width was changed as a parameter (0.5, 0.8, and 1.2 μm at the strip bottom). After phosphorus and boron implantations at the Ge sidewalls, a SiO_2 over-cladding was deposited. Finally, Al/Ti electrodes were formed.

Responsivity spectra were measured under several different applied voltages (0–5.5 V) and at several different temperatures (approximately 20–60°C) in the wavelength range of 1.455–1.640 μm, covering the S (1.460–1.530 μm), C (1.530–1.565 μm), and L (1.565–1.625 μm) bands. The temperature of the sample was thermoelectrically controlled. A lensed fiber was used to couple the TE-polarized light from a tunable laser source to the Si WG via a spot-size converter prepared at the edge of the chip.

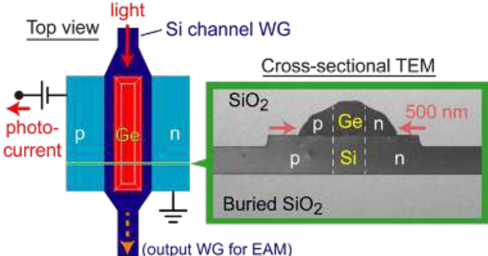


Fig. 1. A schematic top view of a lateral pin PD of a Ge strip and a typical cross-sectional TEM image for the Ge bottom width of 0.5 μm.

3. Experimental Results

3.1. Current–Voltage (I–V) Characteristics

Fig. 2 shows typical I–V curves for a 1.2-μm-wide Ge PD under dark and illumination of 1.55-μm light (2.2 mW at the fiber edge) at different temperatures. Rectifying diode properties were obtained under dark. With increasing temperature, the dark current slightly increased at reverse voltages up to ~ 3 V. Under the illumination, the reverse current increased, indicating a reasonable PD operation. No significant effect of the temperature on the photocurrent was observed. The responsivity at 1.55 μm was as high as 0.9 A/W up to the revers bias of 5 V.

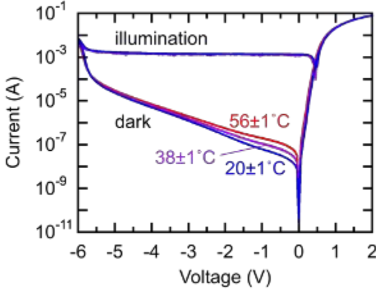
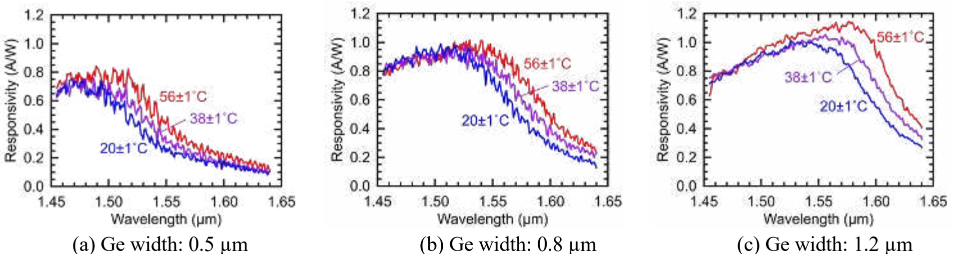


Fig. 2. Typical *I-V* characteristics for Ge PDs with the strip width of 1.2 μm.

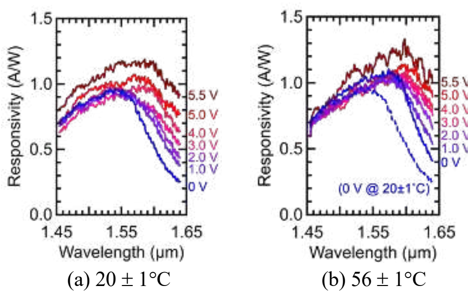


(a) Ge width: 0.5 µm (b) Ge width: 0.8 µm (c) Ge width: 1.2 µm

Fig. 3. Typical responsivity spectra at 0 V for Ge PDs with different strip widths of (a) 0.5 µm, (b) 0.8 µm, and (c) 1.2 µm.

3.2.Effect of Strip Width on Responsivity Spectra

Fig. 3 shows typical temperature dependence of responsivity spectra at 0 V for PDs with different strip widths of 0.5, 0.8, and 1.2 µm. The responsivity at the shortest wavelength of about 1.46 µm was as large as 0.7 A/W (quantum efficiency of about 60%), which was almost independent of the Ge width. At 20 ± 1°C, the responsivity of the 1.2-µm strip decreased above 1.55 µm, whereas those of the 0.5- and 0.8-µm strips started to decrease at shorter wavelengths of about 1.50 and 1.53 µm, respectively. This blue shift with narrowing the strip is attributed to the relaxation of a tensile lattice strain in a Ge layer on Si [3]. The strain relaxation induces a direct bandgap widening, i.e., a blue shift in the optical absorption edge. On the contrary, red shifts were induced with increasing the temperature. Independent of the strip width, the amount of shift was approximately 0.8 nm/°C. This value agrees well with an estimated one based on Varshni's empirical equation for the temperature dependence of the bandgap of bulk Ge [4].



(a) 20 ± 1°C (b) 56 ± 1°C

Fig. 4. Typical responsivity spectra at 0–5.5 V for a Ge PD with the strip width of 1.2 µm. The spectra at two different temperatures of (a) 20 ± 1°C and (b) 56 ± 1°C are plotted.

3.3. Effet of Reverse Bias Voltage

The effect of the reverse voltage were also evaluated, as shown in Fig. 4 for a PD of a 1.2-µm-wide strip. At both temperatures of 20 ± 1°C and 56 ± 1°C, the responsivity increased at the longer wavelength region up to the reverse voltage of ~ 5 V, resulting from the FK effect. At 20 ± 1°C, an increased reverse voltage of more than ~5 V induced an enhanced responsivity in all the wavelength range. This is attributed to the avalanche multiplication, as reported for a waveguide-integrated PD of Ge with a vertical pin junction [5]. The FK effect in combination with the avalanche multiplication under high reverse voltages is effective for the PD operation in a broad wavelength range up to the L band.

4. Conclusions

Spectral responsivity was studied for a waveguide PD of a Ge strip. A blue shift was observed with narrowing the strip, whereas a red shift was induced with increasing temperature. The responsivity was enhanced by the FK and avalanche-multiplication effects under high reverse voltages, being effective for the operation in a broad wavelength range.

Acknowledgements

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Understanding the Pseudo Planar Geometry Scaling in Ge-on-Si Single Photon Avalanche Diodes

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1. Introduction

Single photon avalanche diodes (SPADs) are of significant interest for a diverse range of applications [1] including quantum-key distribution, time-of-flight LIDAR for autonomous vehicles, terrain mapping, and defense. These applications typically benefit from, or require operation in the short-wave infrared (SWIR), where InGaAs/InP SPADs are state-of-the-art. This technology, however, suffers from strong afterpulsing effects and can be prohibitively expensive. Recently, developments have been made with Ge-on-Si SPADs [2,3], which can extend the operation of Si technologies into the SWIR, while still potentially leveraging the cost benefits of Si foundry compatibility. A pseudo-planar design was developed [2] which led to a Single Photon Detection efficiencies of up to ~38 % at 1310 nm wavelength. Record low Noise Equivalent Powers (NEPs) of 7.7×10^{-17} W/Hz$^{0.5}$ were subsequently demonstrated [3], marking a ~100 X improvement compared to a comparable mesa geometry SPAD [4]. This design uses a local p+Ge contact layer, and locally implanted p-Si charge sheet as shown in Fig 1a. This design was key to reducing dark-count rates (DCR) by reducing electric field hot-spots and moving the active area of the pixel away from etched sidewalls. Here, the relative diameters of the p+Ge layer and charge-sheet are investigated experimentally to understand the influence on the device metrics. This is achieved by comparing dark-current and DCR of devices with different geometries. Ultimately, understanding the pseudo-planar design dynamics will facilitate device optimization, enabling device operation at temperatures achievable with Peltier coolers.

2. Simulation

Devices were simulated using Synopysis Sentaurus TCAD packages. Fig. 1b shows a device simulation with the left side showing the E-field and the right showing the triggering probability, as calculated using McIntrye's model [5]. The triggering probability is the probability that the device produces a self-sustaining current pulse if a carrier is generated at that point. This simulation indicates that a SPAD's active area is dominated by the p+Ge diameter. To investigate this effect, a range of Ge-on-Si SPAD pixels were fabricated.

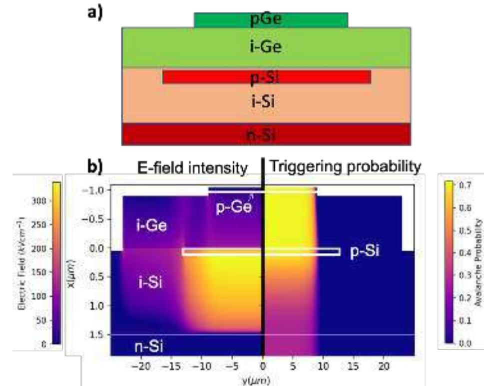

Figure 1: a) Schematic of Ge-on-Si SPAD. b) Simulation showing E-field (left) and triggering probability (right).

3. Pixel design & fabrication

Ge-on-Si SPADs were fabricated by first ion-implanting charge sheets on 150 mm Si wafers, containing 1.5 μm thick i- Si avalanche layers. Subsequently, 1 μm thick Ge absorber layers, and 50 nm thick p+ contact layers are grown using RP-CVD. SPADs are fabricated at the chip scale using standard lithographic, dry-etching and metal deposition techniques. The charge-sheet diameter is determined at the wafer scale, and the p+Ge diameter is defined by dry etching. The processing is described in detail in ref [3].The device dimensions are designated here by *'p+Ge diameter / charge-sheet diameter μm'* e.g. a 10/200 μm device has a 10 μm p+Ge diameter and a 200 μm charge-sheet diameter. Here, we investigate 10/26 μm, 18/26 μm and 10/200 μm devices. The trench isolation etch diameter is 20 μm larger in diameter than the charge-sheet for all devices.

4. Characterization

Devices were measured in a cryogenic probe station fitted with both DC and RF probes, in the temperature range of 100 K to 150 K. A gated technique is used to measure DCR using an arbitrary waveform generator to generate an electrical gate that takes the device above breakdown. This is combined with a DC bias using a bias-tee. Device triggers were counted using an

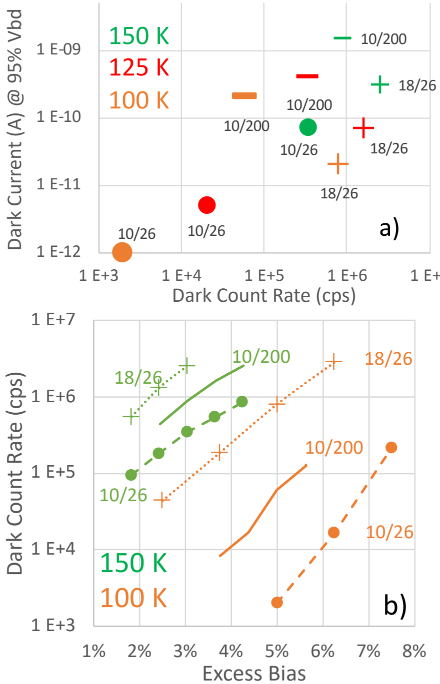

Figure 2: a) Dark count rate vs leakage current at 95% of breakdown. b) DCR vs Excess bias at 100 K and 150 K.

electronic counter, enabling DCR to be calculated based on the fraction of electrical gates that cause a triggering event.

5. Results

Figure 2a shows the dark current (at 95 % breakdown) vs the DCR, for all devices at 100 K, 125 K and 150 K. At all temperatures, the leakage current is clearly significantly larger for the 10/200 µm device compared to both the 10/26 µm and the 18/26 µm devices. This indicates there is current spreading, with contribution to the dark-current from a volume larger than that defined by region underneath the p+Ge layer. This is consistent with device simulation shown in Fig. 1b which show regions of high electric field, particularly in the Ge absorber towards the perimeter of the implanted charge sheet. When comparing DCR, however, the 10/200 µm device is between the 10/26 µm and 18/26 µm devices, Fig. 2a, consistent at all temperatures measured. This trend indicates a complex interplay between the relative spacing of the p+Ge and the charge-sheet diameters. The increase in DCR from the 10/200 µm device compared to the 10/26 µm device shows that the DCR is not solely dependent on the p+Ge layer. This is likely due to carriers being able to diffuse from the larger surrounding volume and trigger the device, which may require Monte Carlo techniques to capture in simulation. This is particularly evident when examining the DCR vs excess bias in Fig. 2b. At 150 K, there is a factor of 5 difference, increasing to 30 times at 100 K, where diffusion lengths will be increased. Interestingly, the 18/26 µm device has a reduced leakage current (5 times at 150 K) compared to the 10/200 µm device but has an increased DCR (3 times at 150 K), Fig. 2a. Comparing the 10/26 to the 18/26 at 150 K there is an improvement of 400 times in DCR and a 20 times improvement in leakage current. This indicates that a greater fraction of the leakage current is multiplied and is therefore indicative of electric-field hot-spots that contribute to increased dark counts.

These results highlight a trade-off in the design of the device geometry. It is clearly important to move electric field hot-spots away from the multiplication region of the pixel, while limiting the total volume that can contribute detrimentally to DCR. This is encouraging, as it shows there is scope for optimization of the technology. As shown in Fig. 2b, the DCR of a 10/26 µm device is ~ 2kcps at 5 % excess bias and 100 K, which is lower than the previously reported 18/26 µm device [3].

6. Conclusion & Future work

Ge-on-Si SPAD devices were fabricated with a varied p+Ge diameter relative to the implanted charge-sheet diameter. It is shown for the first time that decreasing the p+Ge diameter for a given charge-sheet can reduce the DCR, but that complex dynamics are present with regard to the relative dimensions of the layers. There is therefore significant scope to improve Ge-on-Si pseudo planar SPAD devices by optimizing these dimensions. Further work will seek to decouple these effects and investigate the spacing of the etched sidewall from the charge sheet. Single photon detection efficiencies are required to fully understand the performance scaling and will be the focus of future work. This work serves to elucidate the dynamics in the pseudo planar structure and will ultimately facilitate optimization of the technology.

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Electrically tunable Ge-on-Si photodetector

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1. Introduction

Ge-on-Si photodiodes have been firstly reported more than twenty years ago [1] opening the way for the integration of IR photodetectors on Si. A tremendous development has been done, moving from vertically illuminated, stand-alone devices, to waveguide integrated arrays of photodetectors [2] and CMOS integrated imagers [3]. Usually, the Ge epilayer act as the absorbing material for the SWIR radiation, while Si acts only as a substrate. Here we report on a dual-band Ge-on-Si photodetector where light detection can take place both within the Ge epilayer and the underlying Si substrate: the device responsivity can thus be tuned from the VIS to the SWIR spectral range by means of an external bias. Therefore, the presented device can be implemented as a VIR-SWIR CMOS imager. Moreover, the device could be used to discriminate among different chemicals by exploiting the device spectral response in the two bands and the specific absorption spectra of the materials.

2. Working Principle, Design and Growth

A schematic representation of the dual-band photodetector is shown in in Fig. 1. Two photodiodes in a back-to-back configuration are formed by p-doping the back side of a high resistivity Si wafer and by epitaxially growing a p-i-n heterojunction Ge-on-Si layer on the front side (Fig. 1a)). An external bias can be applied to the whole layer stack by means of ohmic contacts formed on the top Ge layer and on the wafer backside (see Fig. 1b)). When a positive bias is applied between the top and bottom contact, the Ge diode is forward biased while the Si diode is reversed biased. In such a configuration the photocurrent generated within the Si substrate by back illuminating the device, will flow through the external circuit and be detected. By reversing the bias polarity, still maintaining a backside illumination, the detected photocurrent will be that generated within the Ge epilayer: in this way it is possible to tune the device responsivity simply by controlling the external bias.

A TCAD model has been set up to optimize doping levels, in particular that of the Si substrate, determining the most effective position the p-n junction within the Si photodiode (at the bottom surface or at the Ge/Si interface) and investigate the role played by substrate thickness [4]. The layer stack reported in Fig. 1a) represents the outcome of such optimization procedure. The epitaxial growth of the structure has been performed by low-energy plasma-enhanced chemical vapor deposition (LEPECVD)[6] as pictured in figure 1a). the backside p-type layer has been formed by spin-on-dopant obtaining a boron-doped layer with an average concentration of 2×10^{19} cm^{-3} and a thickness of ≈300 nm. Standard lithography, dry etching and metallization have been used to fabricate the devices.

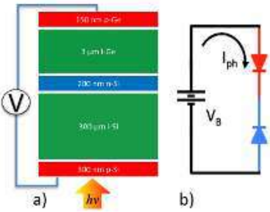

Figure 1 a) Schematic representation of the layer stack resulting in a Si p-n junction and and Ge-on-Si p-i-n junction connected back to back as sketched in panel b).

4. Device Characterization

Optical characterization was performed by means of a lamp-monochromator set-up. The bias dependent dual-band operation of the device is demonstrated in Fig. 3, where the spectral responsivity is shown for two different applied voltages. The VIS/SWIR operation of the device is clearly demonstrated. For $V_B = +1V$, the Si photodiode is reverse biased giving a photoresponse in the 400-1200 nm spectral range. When the bias voltage is reversed to $V_B = -1$ V, the Ge photodiode is reverse biased and a photoresponse in the 1000-1650 nm spectral range is obtained. Its short wavelength cut-off is due to the absorption of Si.

The peak responsivities of the two bands are 0.41 A/W and 0.63 A/W at 960 nm and 1520 nm, respectively. The overall performance of a photodetector has been evaluated by estimating the specific detectivity D* of the device, which, thanks to its low voltage operation has been found to be $7\cdot10^{11}$ $cmHz^{1/2}/W$ and $2\cdot10^{10}$ $cmHz^{1/2}/W$ in the VIS and SWIR, respectively [7].

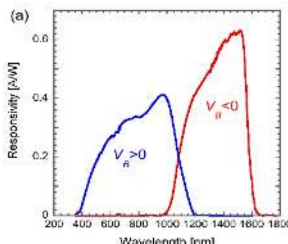

Figure 2 Spectral responses measured at V_B = +1V (blue) and at V_B = -1V (red).

VIS-SWIR single-pixel imaging was performed by mounting the chip on a rastering system and illuminating the subject with a light bulb. In this way the pixel can scan the image plane behind a piano-convex lens collecting the light diffused by the subject. Two images, one in the VIS and one in the NIR, can be obtained by repeating the scanning and changing the polarity of the bias applied to the device. Fig. 3a) shows the RGB filtered VIS image of a blue plastic bottle giving no hint on the filling level. In the NIR image (Fig 3b), instead, the water level is clearly identified thanks to the transparency of plastic and the opacity of water in the SWIR range.

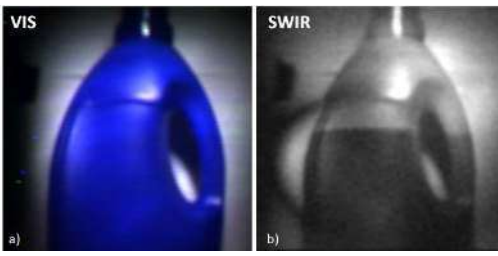

Figure 3 Images obtained with a single-pixel rastering system a) RGB image obtained with the Si photodiode b) SWIR image obtained with the Ge photodiode.

The dual band photocurrent contains spectroscopic information on the relative weight of the SWIR/VIS-NIR components of the detected light. This information can be retrieved by performing a voltage sweep on the double-diode device. Different liquids have been put in a set of identical plastic (HDPE) bottles and illuminated with an incandescent light-bulb. The diffuse reflectance from the filled bottle is then focused on the dual-band photodiode. A chopper and a lock-in amplifier are used to increase the signal-to-noise ratio.

The acquired voltage scan has distinctive features that allow a clear identification of the substance under investigation. All the analyzed look transparent in the visible range and are therefore indistinguishable to the naked eye. Indeed the photocurrent acquired in the VIS-NIR range using the Si diode is very similar for all the substances under investigation. Yet, clear differences appear in the SWIR range, acquired with the Ge diode, and in the value of V_{oc} clearly identified by the notch appearing in the semilogarithmic plot (Fig. 4), depends on the ratio between the Ge and Si photocurrent IGe_{ph}/ISi_{ph}.

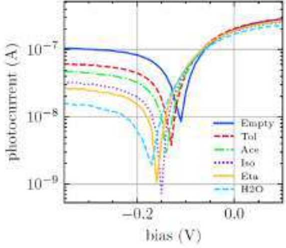

Figure 4 Comparison of the photocurrent vs. bias in the case of an empty bottle (Emp.) and a bottle filled with toluene (Tol), acetone (Ace), isopropanol (Iso), ethanol (Eta) and water (H2O).

3. Conclusions

In conclusion, we have designed and fabricated a voltage-tunable dual-band photodetector operating in the VIS and NIR range. The device is based on a couple of p-i-n photodiodes connected back-to-back formed within a Ge-on-Si epitaxial structure. The device operates between 400 and 1600 nm and its architecture enables to electronically select the shorter (400-1100 nm) or longer (1000-1600 nm) wavelength range with a relatively low applied voltage. VIS-NIR single-pixel imaging and liquid identification have been performed.

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Photodetectors based on 3D self-assembled Ge and Si micro-crystals

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1. Introduction

The direct epitaxial growth of silicon and germanium on silicon (Ge-on-Si) has fostered the development of visible - near-infrared detectors for telecom and imaging applications [1]. A viable route to enhance the responsivity of such photodetectors might be exploiting the micro-structuring of the absorbing layer to increase the effective volume of interaction between light and matter.

In this work we report on a new type of detectors, obtained from Si and Ge micro-crystals epitaxially grown on a patterned Si substrate [2,3]. The faceted morphology and relatively high aspect ratio of the micro-crystals is seen to enhance the fraction of absorbed light and the detector responsivity as compared to conventional planar devices. This enhancement is present in the indirect regime of absorption of Ge, for the Ge micro-crystals, and in the NIR for the Si micro-crystals.

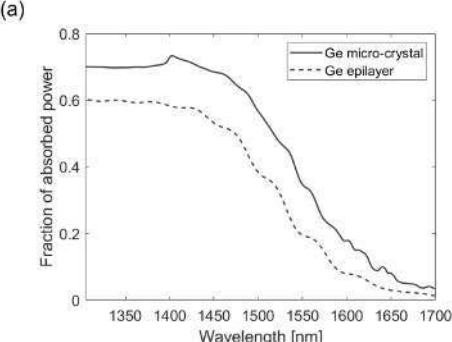
2. Epitaxial growth, modelling and characterization

2.1. Epitaxial growth

The epitaxial growth has been performed by means of Low-Energy Plasma-Enhanced CVD (LEPECVD). Micro-crystal formation is based on the self-assembly of Ge or Si crystals on a Si substrate, deeply patterned by optical lithography and reactive ion etching. 3D micro-crystals, several micrometer tall and characterized by a limited lateral expansion, are obtained by using optimized growth parameters [3]. Due to crystal faceting and pattern periodicity, enhanced light absorption as compared to conventional epitaxial layers is expected.

2.2. FDTD simulations

Modeling of the visible - near-IR absorption properties of Si and Ge-on-Si micro-crystals has been performed by finite difference time domain (FDTD) simulations [4,5]. The simulations have been implemented also for an equivalent planar epilayer, both for Si and Ge. The results of the simulations for patterns of Ge and Si micro-crystals and their equivalent planar epilayer are represented in Fig.1. The simulations confirmed that crystal faceting and pattern periodicity lead to enhanced light absorption as compared to conventional epitaxial layers and



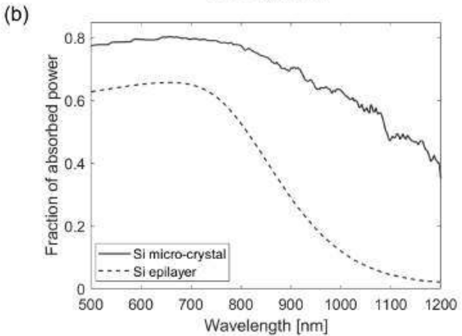


Fig. 1. Simulated fraction of absorbed power for: (a) Ge micro-crystal and Ge equivalent planar epilayer; (b) Si micro-crystal and Si equivalent planar epilayer.

make Si-Ge micro-crystals promising building blocks for optoelectronic devices operating in the VIS- NIR spectral region.

2.3. Responsivity measurements

To experimentally confirm the FDTD results we proceeded with the electro-optical characterization of a single micro-crystal. An experimental set-up based on a nanomanipulator with a tip radius of 100 nm and a confocal microscope was used. The responsivity obtained for a single micro-crystal proved the VIS-NIR photoresponse and the enhancement with respect to an equivalent planar epilayer (Fig.2).

The Si micro-crystals have been grown with a doping profile tuned for their operation as photodetector in the linear regime but also as avalanche photodiodes (APD). For this reason, with the same set-up described above, measurements in the avalanche regime, i.e. very close to the breakdown voltage, have been performed. Fig. 3 shows the measured gain as a function of the reverse bias for an incident wavelength of 900 nm. This gain reaches a maximum value of 10^4, comparable to state-of-the-art literature reports [6].

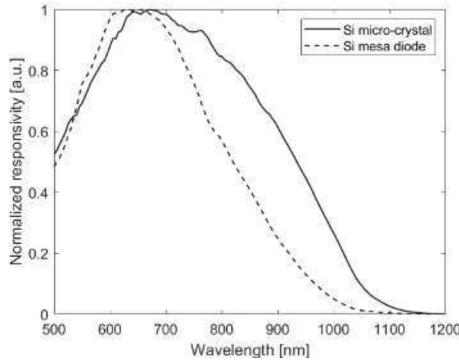


Fig. 2. Comparison between the responsivity of a Si micro-crystal and a Si mesa diode. An enhancement of the responsivity is observed in the NIR region.

After the characterization of the single as-grown micro-crystal we proceeded with the fabrication of a photodetector based on such 3D micro-crystals. The main challenge in realizing vertically illuminated photodiodes based on micro-crystals is the formation of a top transparent contact that can adapt to the surface morphology and bridge the 100-200 nm gap between adjacent microcrystals. To this purpose, we decided to use graphene as a suspended continuous top contact, with an absorption that does not exceed 2.4%.

The Ge micro-crystals fabricated devices have been characterized by electrical and optical measurements. Responsivity measurements confirm the enhanced absorption close to the germanium indirect gap. Fixing the reverse bias at -2V the responsivity of the micro-crystals is ten times that of the epitaxial layer in the 1550-1800 nm wavelength range (Fig.4) [5].

3. Conclusions

Simulations and measurements confirm the possibility of exploiting 3D self-assembled micro-crystals as a new class of photodetectors, exploiting light trapping phenomena in self assembled semiconductors microstructures.

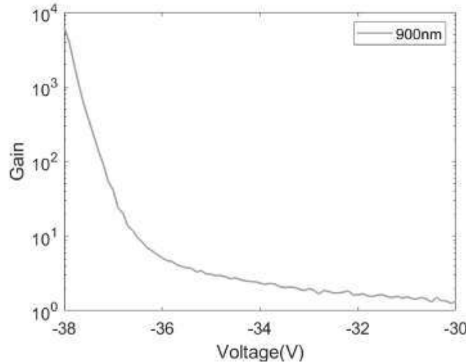


Fig. 3. Gain of a Si micro-crystal operating as APD for a wavelength of 900 nm.

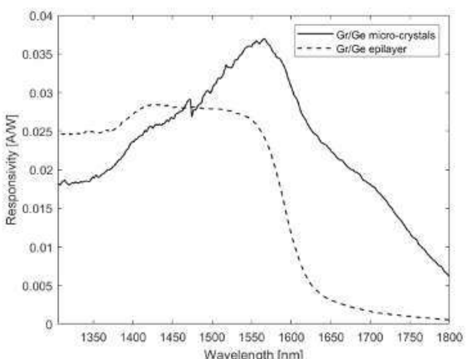


Fig. 4. Responsivity of graphene/Ge micro-crystals device and of graphene/Ge equivalent epilayer.

Acknowledgements

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Position controlled integration of InP nanoislands with CMOS compatible Si using nanoheteroepitaxy approach

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1. Introduction

Epitaxial growth of III-V semiconductors with Si has drawn huge interest due to its potential applications in the areas of optoelectronics and photonics. Amongst the III-V materials, indium phosphide (InP) is considered very promising because of its high carrier mobility, low surface recombination velocity and direct bandgap that is compatible with the optical fiber telecommunication bands, that is suitable for devices like FETs, photovoltaics and telecommunication devices[1-2].

Significant progress has been achieved for direct epitaxial growth of InP on Si, marking their up-scalability with modern semiconductor processing. However, due to the difference in the polarities of InP and Si and a lattice mismatch of ~8%, several defects like antiphase domain defects, stacking faults and microtwins can be formed. To reduce these defects for high functionality of the device, we use nanoheteroepitaxy (NHE) approach for the growth of InP on Si nanotips[3-4]. For high device functionality, a quantitative analysis of p- and n- doping levels is also required.

We show position controlled growth of undoped InP, and n-p doped InP nanoislands on CMOS compatible Si(001) nanotip wafer via gas-source molecular-beam epitaxy (GS-MBE). We further demonstrate their structural and optical properties using diverse characterization techniques like scanning electron microscopy (SEM), atomic force microscopy (AFM), Raman spectroscopy and photoluminescence (PL).

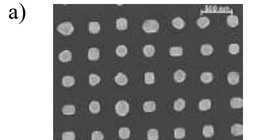
2. Fabrication and Growth of undoped and n-p doped InP nanoislands on Si nanotips

The Si nanotips were fabricated using a state-of-the-art pilot-line capable for 0.13 µm BiCMOS technology on 200 mm Si(001) wafer. The tips are around 400 nm high and arranged in a square lattice with a tip-to-tip distance of 500 nm and embedded inside SiO_2 layer. Upon dipping the 2×2 cm^2 of this wafer in a HF solution, the top layer of SiO_2 gets removed and the tips are exposed for the growth. The wafer is then baked at 750°C prior to the growth for removing native oxides present on the top of the tip. Single crystalline undoped InP nanoislands were grown selectively on these tips at 485 °C with indium growth rate of 0.1 nm/s and 4 sccm flux of phosphine.

The n-p doped InP were grown using similar conditions on n-Si(001) tips having a tip-to-tip distance of 1.4 µm. Silicon and beryllium were used as n and p dopants respectively for the growth. Firstly, a layer of n-InP was grown in direct contact with Si tips followed by a layer of p-InP of equal thickness on its top. There was no growth interruption while switching the dopants.

3. Results and Conclusions

The structural properties were characterized using SEM, AFM and Raman spectroscopy. The lateral size of the undoped InP and n-p doped InP nanoislands are 250 nm and 450 nm respectively as shown in fig. 1.

a) 

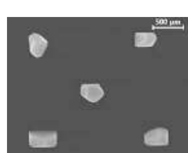
b) 

Fig. 1: Top view SEM image of a) undoped InP b) n-p doped InP nanoislands on Si nanotips.

To understand the 3-D morphology of the InP islands, AFM was performed. Fig. 2 demonstrates the AFM facet analysis depicting the preferred facet planes as (111), (513) and (401) at a facet inclination of 55°, 60° and 75° respectively. Raman measurements on the InP islands showed peak at 303 cm^{-1} and 342 cm^{-1} indicating transverse optical (TO) and longitudinal optical (LO) modes of zincblende InP crystal structure[5].

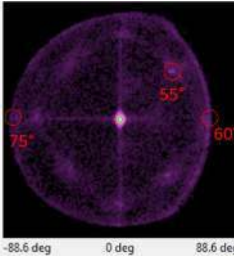


Fig.2: AFM facet analysis of undoped InP nanoislands

To understand the optical properties of the islands, PL spectroscopy was done using an excitation laser with wavelength 532 nm at 80 K. Fig. 3 shows the comparison between both samples: undoped InP and n-p doped InP islands. The undoped InP shows a peak at 1.42 eV and a shoulder at 1.39 eV. The higher energy peak is due to band-to band transition of zincblende InP, while the lower energy peak could be due to conduction band-to- acceptor recombination with an unidentified deep level acceptor present in the material[6-8]. The PL spectra of n-p doped InP nanoislands shows three distinct peaks at 1.39 eV, 1.44 eV and 1.47 eV. The lower energy peak, at 1.39 eV is expected to broaden with increase in the doping concentration due to filling of bands[7]. The origin of other two higher energy peaks need further studies. The inset in fig.3 shows PL spectra of i-InP, n-InP and p-InP, nanowires, which have different behaviour in all three samples as well[6].

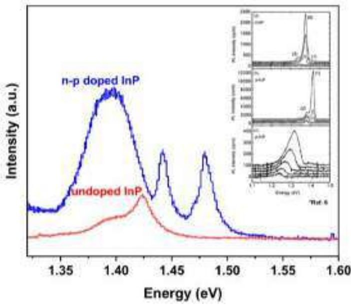


Fig. 3: PL spectra of undoped InP and n-p doped InP nanoislands

The difference in the behaviour of both the samples, as seen from the PL spectra should be investigated more in depth with other techniques, as it might have possible implications while designing the optoelectronic devices.

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Planar PIN Si:Te photodiode for room-temperature infrared detection

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1. Introduction

Silicon is the material par excellence for realizing low-loss passive optical components such as waveguides, modulators, and phase shifters due to its transparency in the telecom wavelength bands near 1310 and 1550 nm. It has a stable oxide, with which it forms high-quality interfaces with a high contrast of the refractive index [1]. This makes Si an attractive prospect for realizing cost-effective photonic integrated circuits using the same equipment and manufacturing processes as computer chips. However, the fabrication of active photonic elements at the telecom bands such as sources and detectors is largely limited by its narrow 1.1 eV optical bandgap. Telecom-wavelength photodetectors require the integration of either III-V compound semiconductors or Ge with Si [2]. Alternatively, Si doped with deep-level impurities above a certain concentration is known for its strong photoresponse in the infrared region (IR) caused by the creation of an impurity band within the Si bandgap [2-5]. Chalcogen-(S, Se, Te) hyperdoped materials exhibit a broad absorption spectrum in the infrared region due to their induced intermediate energy levels in the bandgap of Si. Photodetectors in a vertical configuration utilizing such materials and operated at room-temperature have been reported [3–6].

Recently, a conceptual planar design of an array of lateral *p-i-n* photodiodes based on hyperdoped Si was proposed [5]. In this work, we present the first experimental demonstration of a Te-hyperdoped Si planar array of a room-temperature infrared photodetector. The study of such a detector is promising for the integration with Si passive photonic components like waveguides, attenuators, and modulators. We present the characterization of these photodetectors based on dark current-voltage characteristics (IV), infrared responsivity, noise equivalent power (NEP), detectivity and frequency response.

2. Sample preparation and experimental setup

We used photolithography for the patterning of a mask for the planar PIN device to define the *p* and *n-type* regions. We used ion implantation for introducing non-equilibrium doping concentrations (above the solid solubility 10^{18} cm^{-3}) in an intrinsic Si (1 0 0) wafer for the formation of the hyperdoped Te and boron interdigitated regions. Recrystallization of both doped regions was achieved using the pulsed laser melting (PLA) method. Metal contacts were then deposited on the hyperdoped regions (fig. 1 a).

We used Raman spectroscopy for the structural analysis of the synthesized hyperdoped regions. The photoresponse measurements were performed using a monochromator and a Quartz Tungsten Halogen (QTH) lamp. We used a lock-in-amplifier along with a low-noise current amplifier for acquiring the signal mechanically chopped at the frequency of interest. The NEP measurements were performed by adapting the procedure reported in [8]

3. Results

The dark IV of the fabricated device is shown in fig. 1 (b). It has a diode behavior with a considerable rectification ratio of around 200. We observed a responsivity of $8x10^{-5}$ A/W and $1x10^{-5}$ A/W for 1300 nm and 1550 nm respectively when operated with a reverse bias of 1V, a commercial Si detector is also presented for reference (fig. 1 c). The NEP of the device is in the order of $7x10^{-7}$. We also measured the 3dB cut-off frequency (f_{3dB}) of the detector, which is above 250 kHz. This was found to be related to the large RC constant of the device, as the device dimensions are large *i.e.* 3 µm x 3 µm.

4. Conclusion

In this work, we have reported a planar PIN Te-

hyperdoped Si infrared detector operating at room temperature which has the potential to be integrated with active and passive Si photonic components. The recrystallization for both *p* and *n-type* hyperdoped regions has been achieved using pulsed laser melting. The PIN Si:Te device shows a strong rectification behavior with a room temperature responsivity of 10^{-5} A/W from 1300 nm to 1550 nm. Detectors of smaller dimensions (reduced RC constant) would provide a higher 3dB cut-off frequency.

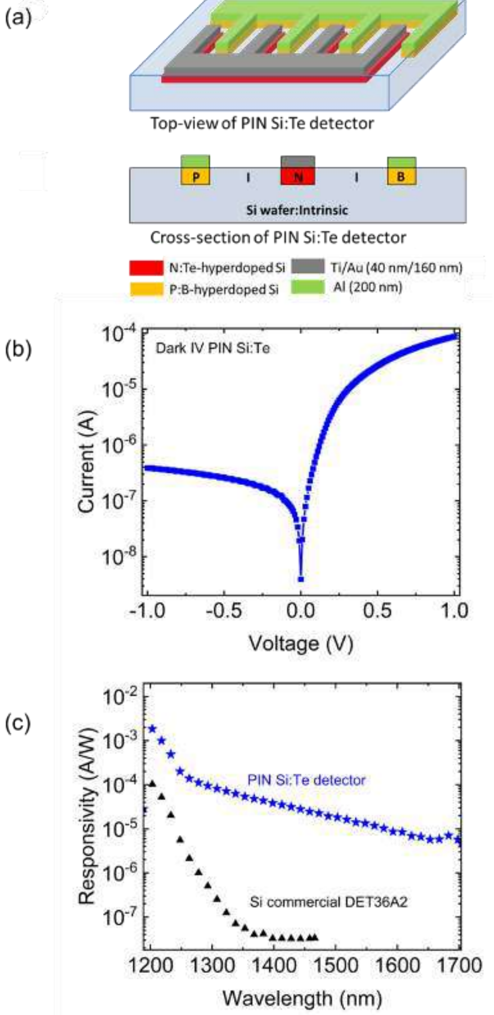

Fig. 1. a) Top view and cross-section of a proposed p-i-n photodetector with hyperdoped n region with transparent electrodes [5], b) Dark IV characteristics of PIN Si:Te detector, c) Room temperature responsivity for the detector

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Integration of electro-optic barium titanate on Si and SOI

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1. Introduction

Silicon-on-insulator (SOI) is a platform of choice for photonic applications due to the ability to fabricate waveguides with very low losses and high optical mode confinement [1-2]. To capitalize on this, active electro-optic (EO) devices need to be readily manufacturable on silicon (Si). While ferroelectric $LiNbO_3$ is well-established as an excellent material in terms of RF electro-optic gain-bandwidth, linearity, low optical loss, and overall robustness [3-4], it is not straightforward to integrate high quality material with Si [5], and it is incompatible with a standard Si fab.

$BaTiO_3$ (BTO) is a ferroelectric material that exhibits one of the largest Pockels coefficients among EO materials, with a coefficient as high as 1300 pm/V in the bulk (40 times that of $LiNbO_3$) [6]. BTO is also much easier to integrate with Si than $LiNbO_3$ [7]. Epitaxial BTO integrated on Si is a promising materials platform for building EO modulators based on the Pockels effect that can be used for fast, low-power optical switches, or even for new forms of computing including neuromorphic and quantum computing [10]. In addition, unlike $LiNbO_3$, BTO does not have any volatile components and therefore, is compatible with silicon fabrication processes.

Both, small footprint Mach-Zehnder and ring resonator hybrid modulators based on Si waveguides patterned on top of BTO grown on silicon by molecular beam epitaxy (MBE) have been recently reported [11-12]. These devices demonstrate that substantial electro-optic modulation can be achieved in Si photonics-compatible processes. In both cases, the devices utilized a portion of the r_{42} component of the BTO Pockels tensor, which is the largest component, and relies on the BTO film having its ferroelectric polarization in-plane (a-axis oriented or X-cut films). Such X-cut modulators have the benefit of being easily fabricated in a standard silicon photonics process flow without pattering the BTO. Waveguides can be made out of silicon or silicon nitride deposited and patterned on the BTO layer and electrodes deposited to form the TE-mode EO modulators [12]. Alternatively, waveguides can be fabricated in the BTO material itself, both in c-axis or a-axis oriented films. Using a c-axis oriented film, with polarization normal to the film's surface, enables fabrication of waveguides using TM-modes similar to Z-cut devices fabricated in $LiNbO_3$ [13].

We developed processes to integrate ferroelectric BTO films with both c- and a-axis orientation on Si and Si-on-insulator with thickness ranging from 0.1 to over 1 μm, using MBE and off-axis RF magnetron sputtering. Films show excellent EO characteristics and support fabrication of ultra-compact, ultra-low-power EO modulators compatible with Si photonics.

2. Integration on Si

2.1. Molecular Beam Epitaxy

MBE is a very flexible albeit slow tool to integrate BTO on both Si and SOI [6]. We start with depositing a $SrTiO_3$ (STO) buffer directly on Si (001) and proceed with either a layer-by-layer shuttered deposition or co-deposition of Ba and Ti from the metal sources in the presence of oxygen. It is a high temperature process (around 700°C) resulting in high crystalline quality BTO films. A typical 100 nm-thick BTO film is shown in Fig 1. The excellent crystal quality of MBE-grown films is evident form a narrow rocking curve peak (<0.3°). The films start out strained and c-oriented and begin transitioning to a-oriented at about 30 nm, unless strain engineering is used [14].

2.2. RF magnetron sputtering

We also grow highly crystalline, epitaxial BTO films with a-axis orientation and thickness >300 nm by off-axis RF magnetron sputtering on either Si or SOI substrates. The STO buffer still requires MBE deposition but is very thin compared to the BTO film itself.

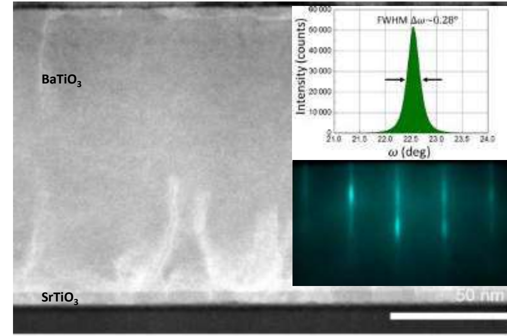

Fig. 1. Large-scale image of BTO film on Si showing no distinct grains and high epitaxy quality across the film. The insets show the rocking curve of the BTO 002/200 peak and

the RHEED in the [110] direction of the BTO surface.

The films are structurally of similar quality to those grown by MBE but can be grown more than ten times faster, enabling a path for manufacturability of rather thick films [8]. The 0.5 μm thick RF-sputtered a-oriented film is shown in Fig. 2. The dislocations seen in Fig. 2a stem from the non-optimal cooling and can be controlled. The c-oriented films can also be grown up to a thickness of 120 nm. To grow c-oriented films thicker than this, we use straining STO interlayers where we have demonstrated 0.4 μm thick c-oriented films on SOI.

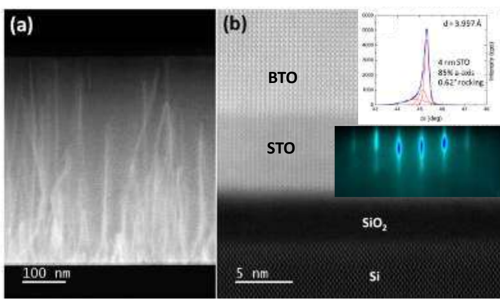

Fig. 2. ADF-STEM images of the cross section of a 500 nm BTO film grown by sputtering. (a) Low-magnification image showing the entire BTO layer. (b) Atomic resolution image of the interface region of the film. The insets show the 002/200 x-ray diffraction peak and the RHEED of the BTO surface.

2. Optical Characterization

The films have been characterized optically as unpatterned thin films and via fabricating waveguides and modulators. In view of the application in Si photonics, the most important materials properties are optical losses and the effective EO coefficient.

3.1. Losses

While the best $LiNbO_3$ devices based on bulk material demonstrate very low losses, with the hybrid devices exhibiting 0.2 dB/cm and the monolithic devices boasting as low as 0.15 dB/cm [4], BTO-based modulators at the moment show an order of magnitude higher loss. This, however, may not be intrinsic to the material, but rather arises from the lack of proper poling and non-optimized fabrication. Our slab waveguide loss measurement for the unpoled film revealed the loss in the range of 1 to 1.5 dB/cm for both TE and TM modes at 1550 nm wavelength [13]. We believe this is the upper limit and that proper poling will reduce the loss.

3.1. Electro-optic response

The EO response is the area where BTO truly shines. The bulk value of r_{42} is 1300 pm/V, and the highest reported thin film value is 900 pm/V [12]. However, more typically, an effective Pockels coefficient rather than a specific tensor component are reported for a-oriented films. For a-oriented films (active thickness around 100 nm) we measure an effective EO coefficient of 350 pm/V for MBE-grown films [14] and 182 pm/V for RF sputtered films [8]. For c-oriented films of similar thickness we measure an r_{33} component of 134 pm/v that is essentially the bulk value [13]. EO modulators fabricated on this material demonstrate V_{π}-L on the order of 0.2-0.4 V-cm, which is an order of magnitude better than that of Si-integrated devices based on $LiNbO_3$. More importantly, the BTO-based modulators are about two orders of magnitude smaller in area, which translates to significantly lower energy consumption and chip real estate.

3. Conclusions

Highly crystalline, epitaxial BTO films with either a-axis or c-axis orientation can be integrated on STO-buffered Si or SOI with thicknesses up to 1 μm. The integration can be achieved either by MBE or by RF magnetron sputtering, with the films being of similarly high quality. BTO demonstrates sufficiently low loss and high EO activity necessary for fabrication of highly efficient compact EO modulators for integrated Si photonics.

Acknowledgements

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Impact of flows, temperature and pressure on the GeSn growth kinetics with a Ge_2H_6 + $SnCl_4$ chemistry

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1. Introduction

We recently succeeded in fabricating room temperature optically pumped GeSn lasers with a Sn concentration close to 17% in the thick GeSn layers of such devices [1, 2]. They were grown at 100 Torr with a Ge_2H_6 + $SnCl_4$ chemistry on Ge Strain-Relaxed Buffers (SRBs), themselves on Si(001) substrates. The growth temperature was the main lever used to change the Sn concentration in such stacks, but not only. We for instance also reduced, at 307°C, the $SnCl_4$ flow when capping the optically active GeSn layer with lesser Sn content layers, instead of increasing the temperature [2]. The aim was then to avoid Sn surface precipitation in such stacks. In the following, we will quantify, for a fixed Ge_2H_6 flow, the impact of temperature, pressure, H_2 carrier flow and $SnCl_4$ flow on the GeSn growth kinetics. Such a know-how will be most useful to fabricate complex, high Sn content stacks for use in electrically pumped lasers, light emitting diodes and so on.

2. Results

2.1. Experimental details

Omega-2Theta scans around the (004) X-Ray Diffraction order as in **Fig. 1** were used to gain access to the thickness, in the 37 to 60 nm range, and Sn content, in the 2.3% - 14.3% range, of the pseudomorphic GeSn layers grown in the 301°C – 362°C range on Ge SRBs.

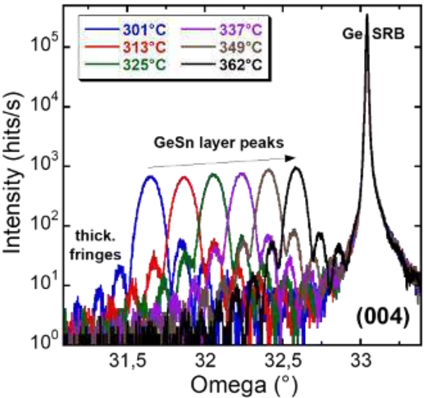

Figure 1 : XRD profiles of GeSn layers grown at 100 Torr with $F(SnCl_4)/F(H_2)_{ref.} = 4.69x10^{-5}$.

The Ge_2H_6 flow was fixed and such that the $F(Ge_2H_6)/F(H_2)_{ref.}$ Mass-Flow Ratio (MFR) was equal to $7.92x10^{-4}$. The growth pressure was either 50 or 100 Torr, the H_2 carrier flow either the reference value of a few tens of standard liters per minute or half of it and the $SnCl_4$ flow varied from $F(Ge_2H_6)/F(H_2)_{ref.} = 1.88x10^{-5}$ up to $5.62x10^{-5}$.

2.2. Impact of $SnCl_4$ flow and temperature

We have first quantified the impact of the temperature T, in the 301°C – 362°C range, and the $SnCl_4$ flow on the GeSn Growth Rate (GR) and Sn content. The resulting data are shown in **Fig. 2**.

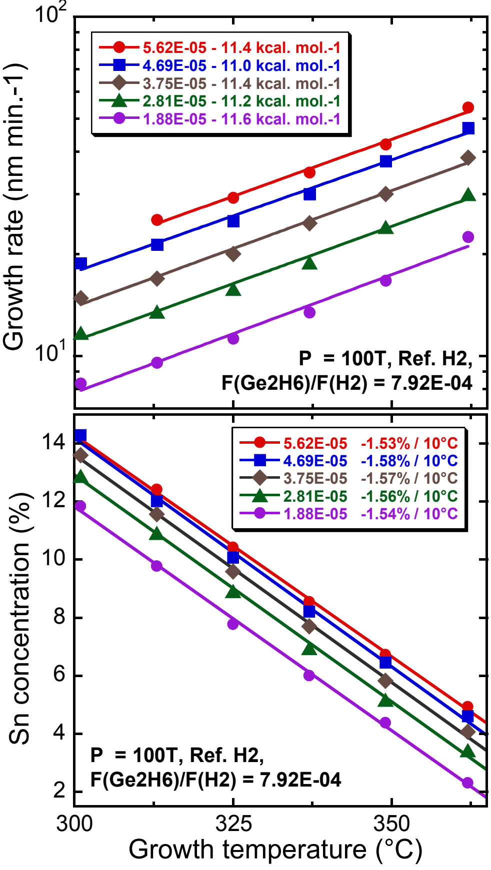

Figure 2 : growth rates and Sn contents in GeSn layers grown at 100 Torr with various $F(SnCl_4)/F(H_2)_{ref.}$ MFRs (see the inset) in the 301°C – 362°C range.

The GeSn growth rate exponentially increased with T, with very similar activation energies between 11.0 and 11.6 kcal $mol.^{-1}$ whatever the $SnCl_4$ flow. There was otherwise a linear increase of the GeSn GR with the $SnCl_4$ flow whatever the temperature, with a steeper slope at higher T.

Meanwhile, the Sn concentration linearly decreased as T increased, with very similar slopes between -1.53%/10°C and -1.58%/10°C whatever the $SnCl_4$ flow. The sub-linear increase of the Sn concentration x with the $SnCl_4$ flow was fitted with a $x^2/(1-x) = n*F(SnCl_4)/(2*F(Ge_2H_6))$ relationship. The n parameter exponentially decreased from 0.443 down to 0.085 as T increased from 301°C up to 362°C, with a -18.8 kcal. $mol.^{-1}$ slope.

Multiplying the GeSn growth rate by the Sn content x or the Ge content $1-x$ yielded Sn and Ge GR components. Plotting them as functions of T gave us hints about growth mechanisms. We had an exponential increase of the Ge GR component with T, with very similar activation energies between 12.3 et 12.8 kcal $mol.^{-1}$ whatever the $SnCl_4$ flow. The Ge GR component otherwise increased with the $SnCl_4$ flow, although the Ge_2H_6 flow was constant. This was due to a larger number of surface sites available for growth. We were thus in a surface-limited regime for Ge. Meanwhile, the Sn GR component decreased with T whatever the $SnCl_4$ flow. It otherwise increased with the $SnCl_4$ flow. We were thus in a supply-limited regime for Sn, with more and more Sn atoms sublimating from the surface as T increased.

2.3. impact of H_2 carrier flow and growth pressure

The Ge_2H_6 and $SnCl_4$ mass-flows being constant, we then evaluated the impact of the H_2 carrier flow and pressure on GeSn growth kinetics. Data are shown in **Fig. 3**.

The GeSn growth rate exponentially increased with T whatever the H_2 carrier flow and chamber pressure. Dividing by two, at 100 Torr, the H_2 flow and halving the chamber pressure (from 100 down to 50 Torr) resulted in activation energies increases from 11.0 up to 12.1 and finally 13.8 kcal. $mol.^{-1}$. GRs were otherwise higher when halving the H_2 carrier flow and the chamber pressure.

Meanwhile, the the Sn concentration linearly decreased with T whatever the H_2 carrier flow and chamber pressure. Dividing by two, at 100 Torr, the H_2 flow resulted in very similar slopes: -1.58%/10°C ⇔ -1.55%/10°C. Halving the chamber pressure (from 100 down to 50 Torr) had more of an impact: -1.55%/10°C ⇔ -1.44%/10°C. Sn concentrations were otherwise higher, at 100 Torr, when halving the H_2 carrier flow. Halving, for that reduced H_2 flow, the chamber pressure resulted in lower Sn contents.

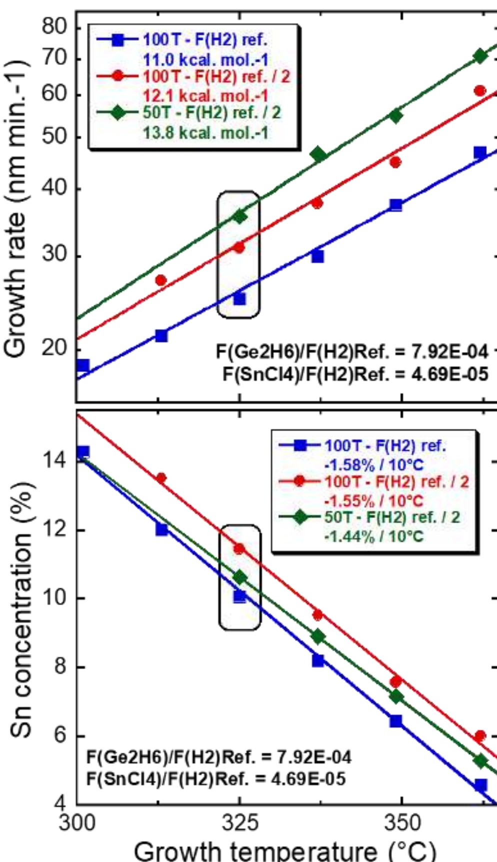

Figure 3 : growth rates and Sn contents in GeSn layers grown with various H_2 carrier flows and pressures in the 301°C – 362°C range. Fixed Ge_2H_6 and $SnCl_4$ flows.

Missing data points in Fig. 3 for reduced H_2 flows and chamber pressures were actually due to a complete lack of growth at low temperatures.

As far as layer uniformities over the wafers were concerned, the best tradeoff was at 100 Torr with the reference H_2 flow. Thickness uniformity was indeed better but Sn concentration uniformity worse when halving at 100 Torr the H_2 carrier flow. Going down to 50 Torr yielded the worst thickness uniformity and the best Sn content uniformity of all. Finally, surfaces of all layers grown in the 301°C-349°C range were, whatever the growth conditions, smooth and cross-hatched as the Ge SRBs underneath, while 362°C layers were islanded.

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Efficient in-situ p- and n-doping of strained germanium tin epilayers

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1. Introduction

Novel group IV semiconductor epitaxial structures of Silicon (Si), Germanium (Ge) and Tin (Sn) on Si or Silicon on Insulator (SOI) substrates are a natural way to improve the properties of modern state of the art Si semiconductor devices and to expand their existing functionalities. Epitaxially grown Germanium Tin ($Ge_{1-x}Sn_x$) binary alloys have recently emerged as a versatile and promising semiconductor for a wide range of applications spanning fields such as electronics[1], photonics[2,3], spintronics and quantum technologies[4-7]. These group IV materials offer the possibility to leverage strain and bandgap engineering to tune device performance and to embed optimized components into conventional Si-based circuitry. $Ge_{1-x}Sn_x$ is expected to be an essential building block to implement source/drain contacts in future high-performance field-effect transistors[8,9] and low-resistivity ohmic contacts in large variety of devices spanning from diodes, including LED, lasers, etc up to sensors. Contact engineering is thus one of the critical aspects that need to be advanced to bring $Ge_{1-x}Sn_x$ photonics a step closer to real life deployment. It is worth noting that heavily doped $Ge_{1-x}Sn_x$ alloys are also endowed with plasma frequencies in the mid- and far-infrared ranges of the electromagnetic spectrum. This is a yet-untapped feature that could lead to novel optical technologies based on plasmonic sensors with distinct advantages in diverse fields including point-of-care diagnostics and light harvesting for photovoltaics[10,11]. *Finally, tailored carrier mobilities and electrical conductivities in highly doped materials are a steppingstone in maximizing the energy conversion efficiency for waste heat recovery*. Efforts on this subject can arguably disclose the full potential of $Ge_{1-x}Sn_x$ alloys in the burgeoning field of thermoelectrics and renewable energy[11,12].

Well-controlled incorporation and efficient activation of both donor and acceptor impurities in semiconducting $Ge_{1-x}Sn_x$ is indeed crucial for all the applications where charge transport plays a central role, let alone hybrid integration schemes in which the active region is based on III-V compounds rather than group IV materials. *To this purpose, in-situ doping through epitaxy of $Ge_{1-x}Sn_x$ films above the metal-to-insulator transition can provide a facile and effective method to yield low-resistivity ohmic contacts for a large variety of modern and future devices. In particular, only strained doped $Ge_{1-x}Sn_x$ epilayers, without additional defects generation, would lead to the highest electrical activity of dopants and therefore the lowest material's electrical resistivity.* Presently, however, little is known about electronic transport in epitaxial $Ge_{1-x}Sn_x$, especially under degenerate doping conditions. The available data often focus on one specific type of impurity, providing information within restricted temperature intervals, chiefly around 300 K.

In this work we researched, both experimentally and theoretically, the p- and n-type in-situ doping of strained, and therefore defect free, $Ge_{1-x}Sn_x$ epitaxial layers and their impact on structural and electrical materials properties.

2. Results and discussion

The $Ge_{1-x}Sn_x$ layers were epitaxially grown on 100 mm diameter Si(001) wafers via a non-intentionally doped relaxed ~600 nm thick Ge buffer layer in a reduced pressure chemical vapour deposition (RP-CVD) system.[5,13] A schematic cross-section of the samples is shown in the Fig. 1a. Seven samples were grown, *at unusually very low wafer's temperature of 260 ^oC and in hydrogen (H_2) carrier gas atmosphere*, with different doping levels of the $Ge_{1-x}Sn_x$ epilayer: one undoped, as a reference sample with Sn content 11.6% ±0.1 in the $Ge_{1-x}Sn_x$ alloy epilayer, three p-type doped using an increasing amount of boron (p, p+, p++), and three n-type doped with phosphorus (n, n+, n++). The doping range was varied between $\sim 1 \cdot 10^{17}$ and over $\sim 1 \cdot 10^{20}$ cm^{-3}. Diborane and phosphine were used as precursors for p-type and n-type doping, respectively. The partial pressure of both precursors was the same for p and n, p+ and n+, and p++ and n++

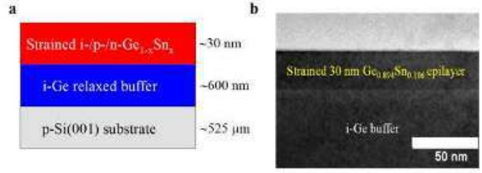

Fig. 1. (a) Schematics cross-section of the strained $Ge_{1-x}Sn_x$/Ge/Si(001) heterostructures grown by CVD. (b) High magnification XTEM image of the surface region of the p+ 30 nm thick strained $Ge_{1-x}Sn_x$ sample is shown.

samples. In contrast to most reported results, which stress the need of much more expensive and unstable Digermane precursor to grow epitaxial $Ge_{1-x}Sn_x$ thin films using Chemical Vapour Deposition, we used a standard Germane precursor for Ge. Also, in contrast to published results epitaxy takes place in a hydrogen atmosphere, without nitrogen present.

All epilayers thicknesses of $Ge_{1-x}Sn_x$/Ge/Si(001) heterostructures were obtained via analysis of XTEM images. Fig. 1b shows a typical high magnification XTEM image of the surface region of one of the samples, with p+ 30 nm thick strained $Ge_{1-x}Sn_x$ epilayer and top region of very high quality relaxed Ge buffer. The defect free $Ge_{1-x}Sn_x$ epilayer with very smooth surface and abrupt interface between $Ge_{1-x}Sn_x$ epilayer and Ge buffer is clearly visible. Surface roughness, measured by AFM, of all samples is ~1 nm root mean square surface roughness (RMS) and does not change by either n- or p-type doping of the $Ge_{1-x}Sn_x$ epilayer. Compressive strain and Sn content in each $Ge_{1-x}Sn_x$ epilayer were obtained by analysing of HR-XRD data.

Hall-bar devices for subsequent electrical characterization of the samples using resistivity and Hall effect measurements over 15 – 300 K temperature range, were microfabricated using optical lithography, etching and contacts formation techniques. Insert in Fig. 2 shows a plan view optical image of a typical fabricated Hall bar device. Fig. 2 demonstrates effect of both p- and n-type doping on the formation of the $Ge_{1-x}Sn_x$ solid solution. The same growth conditions were maintained for all the samples, including partial pressure of precursors. No changes in Sn content are observed between the undoped $Ge_{1-x}Sn_x$ and both lightly p- and n-doped, up to relatively low values of 10^{17} cm^{-3}, samples. N-type doping with Phosphine leads to slight increase in Sn content from ~11.6%, for undoped reference sample and low doped n (1×10^{17} cm^{-3}), up to 11.9% for n+ (5×10^{19} cm^{-3}) and additionally to 12.2% for n++ (7×10^{19} cm^{-3}) samples. In contrast to it, doping with diborane leads to pronounced changes in Sn content manifested itself via reduction of Sn content down to 10.6% for p+ (3×10^{19} cm^{-3}) and 9.5% for p++ (4×10^{20} cm^{-3}) samples. Explanation for the observed phenomena will be presented at the conference.

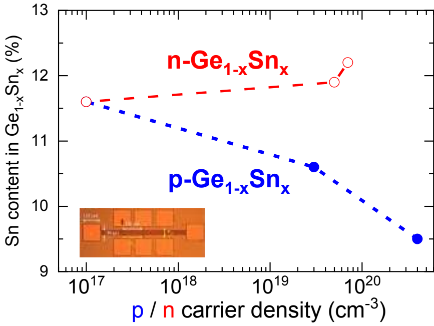

Fig. 2. Sn content in $Ge_{1-x}Sn_x$ epilayer for both p-type and n-type doped sample as a function of the Hall carrier density measured at 15K. Insert shows Hall-bar device used to measure transport properties of the materials.

3. Conclusions

In conclusion, in-situ doping of compressively strained $Ge_{1-x}Sn_x$ epilayers, grown by CVD, at very low substrate temperature of 260 ºC, reveals unusual impact of dopants manifesting via pronounced reduction of Sn content in the epilayer accompanied with enhancement of growth rate, due to increasing p-type doping concentration and opposite behaviour for n-type doping, but resulting in less pronounced increase of Sn concentration and no effect on growth rate. Very high carrier density of holes up to ~4×10^{20} cm^{-3} is obtained in p-type doped $Ge_{1-x}Sn_x$ epilayer resulting in the lowest resistivity of 0.15 mΩcm among all in-situ doped epitaxially and strained group-IV semiconductors. In contrast to p-type doping, n-type doping using Phosphorus in strained $Ge_{1-x}Sn_x$ epilayer is limited to much lower values, i.e. 7×10^{19} cm^{-3}.

In addition, we find the metal-to-insulator transition in $Ge_{1-x}Sn_x$ to start at doping densities as low as 1×10^{17} cm^{-3}, substantially lower than any group-IV semiconductor.

Efficient p- and n-type doping $Ge_{1-x}Sn_x$ epilayers in the range between ~10^{17} and ~4×10^{20} cm^{-3} is demonstrated. Our findings can contribute to the development of efficient current injection in future electronic devices, thus facilitating the transition of technologies and heterostructures based on $Ge_{1-x}Sn_x$ from research labs to the industrial production.

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In-Situ Strain Control of Silicon Carbide for 3D MEMS Applications

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1. Introduction

Three-dimensional (3D) micro-electro-mechanical systems (MEMS) have allowed for evolutionary transition from the conventional integrated circuits technology and planar methodology. Bulk micromachining, LiGA (fabrication technology to create of high aspect ratio microstructures), and surface micromachining [1] have had significant contribution to the design and development of 3D structures such as resonators, accelerometers, pressure sensors, flow control devices (e.g. micropumps) and flow sensors.

Bulk micromachining is limited to Si [2] substrate but its etchants are highly toxic or explosive at concentrations suitable for batch fabrication [3]. LiGA welcomes a wider range of suitable materials [4] but lacks lateral resolution and uniformity [5]. Conventional LiGA uses high energy X-ray (X-ray LiGA) for lithography that is complex and expensive. The alternative, UV LiGA, although cheap and accessible, suffers from lack of adhesion and uniformity [6]. Surface micromachining is not bound to a specific substrate material and is affordable. However, its prominent issues such as unwanted buckling of released structures, etch selectivity, and stiction continue to exist.

Efforts have been made to offer solutions that combine surface micromachining with other, generally, nonconventional techniques to create elevated structures attached to planar fixtures for out of plane motion and sensing. These processes require additional assembly and micromanipulation, complex fabrication involving several steps, appealing to intricate deposition methods and uncommon techniques such as electric or magnetic field [7 – 12].

This work presents, for the first time, a fabrication method through which cubic silicon carbide (3C-SiC) microbeams with in-situ, via epitaxy only, controlled out-of-plane curvature have been suspended from Si substrates, see Fig. 1. This novel technique not only simplifies 3D microfabrication, but also resolves the ever-existing obstacle in surface micromachining of unwanted buckling of microstructures upon suspension, due to difference in thermal expansion coefficient and/or mismatch of lattice parameters.

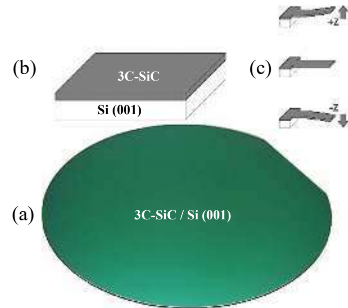

Fig. 1. a) 100 mm diameter 3C-SiC on Si(001) epiwafer, b) schematic cross section of the 3C-SiC/Si(001) heterostructure and c) 3C-SiC cantilevers with positive, neutral and negative microbeam deflection.

2. Method of approach

2.1. Epitaxial growth

Sub-micron thick 3C-SiC films with different carbon to Si (C/Si) ratios were grown on 100 mm diameter Si (001) wafers using an industry standard 'cold-wall' reduced pressure chemical vapor deposition (RP-CVD) at relatively low temperature of~ 1000 °C, see Fig. 1 (a) and (b). Variation in C/Si ratio was achieved by varying partial pressure of carbon precursor.

2.2. Microbeam microfabrication

Microbeams with fixed width (5 μm) and variable lengths (10 to 100 μm) were produced using a simple lithography process and all dry fabrication process. An oxide mask layer was deposited onto the wafer at low temperature in a plasma-enhanced CVD (PECVD). Patterns were transfer using deep reactive ion etching (DRIE) onto oxide and then carbide layer. Finally devices were released by isotropic dry etching of Si. Simulations performed used COMSOL Multiphysics, to optimize the geometry and the extent of undercut.

2.3. Characterization

A handful of technique were utilized to characterize 3C-SiC/Si epiwafers and microbeams in terms of

crystal quality, surface roughness, static and dynamic mechanical properties; namely X-ray diffractometry (XRD), atomic force microscopy (AFM), white light interferometry, laser doppler vibrometry (LDV) and scanning electron microscopy (SEM).

3. Results and discussions

X-ray measurements, including high resolution XRD (HR-XRD), X-ray reflectivity (XRR), rocking curve (RC), were performed to analyze crystal orientation, thickness, composition, and lattice strain for all samples, confirming monocrystalline quality of 3C-SiC growth on Si(001). These results were confirmed by surface roughness analysis using AFM, proving very smooth surfaces.

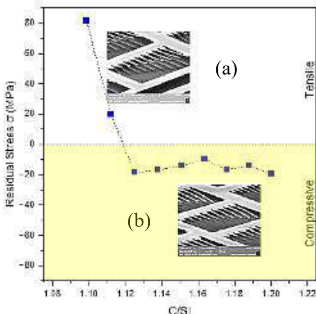

Fig. 2. 3C-SiC microbeam's residual stress as a function of C/Si ratio. Insets (a) and (b) show curvature profiles corresponding to tensile and compressive stresses, respectively.

Microbeams were characterized in terms of their static and dynamic mechanical behaviour. Static deflection parameters of the microbeams, Z deflection and radius of curvature, were measured using white light interferometry; and they were used to calculate the residual stress in the epilayers, see Fig. 2. The increase in the C/Si resulted in a declining trend in thin film stress, effectively switching the signage from positive to negative; also known as tensile to compressive, respectively. SEM imaging shows microbeams with curvature profiles changing from concave up (Fig. 2, inset (a)) to concave down (Fig. 2, inset (b)), qualitatively confirming static measurements and stress calculations. A transient drop throughout the Si-rich region followed by a steady state flattening towards the C-rich, of residual stress values shows a nonlinear (almost an exponential decay) trend. It also indicates that the stress values are highly sensitive to C/Si quantities between 1.09 and 1.13, and almost undisturbed for amounts 1.14 and larger.

For microresonator applications in particular, it is not only the static, but also the dynamic response that is of strong interest. Frequency response of the microbeams characterized above has been analyzed using the vibrometer, normalized to the beam thickness, and compared against both the values extracted from simulations and also the average of measured values. The results have shown to be within the experimental error of the characteristic resonance frequency obtained theoretically.

4. Conclusions

Microbeams were fabricated from low temperature grown 3C-SiC/Si epilayers, with different degrees of curvature defined by epitaxial growth conditions. Fabrication method involved direct-write lithography and all-dry processing. The ratio of carbon to silicon precursors partial pressure in the reactor, during the heteroepitaxy, proved to be the defining parameter for the amount residual stress in the films and as a result the sign and magnitude of curvature in the beams. All dry processing proved advantageous in terms of both selective etching and stiction prevention. Implications of strain control are two-fold: suitability of 3C-SiC/Si systems as device layer for 3D fabrication and as virtual substrate for subsequent material growth.

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Local epitaxial growth of GaAs islands for monolithic integration on Si

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1. Introduction

An epitaxial growth technology for monolithic integration of III-V semiconductors on silicon substrates is presented designed to avoid overheating of delicate electronic components. The method relies on local substrate heating using focused laser radiation and pyrolithic decomposition of metalorganic precursors. Thereby, local metalorganic vapor phase epitaxy of circular islands is enabled with diameters ranging from 50 µm up 3000 µm. Successful homoepitaxial growth of GaAs islands on GaAs(001) substrates was recently demonstrated [1]. We discuss important steps towards growth control and present first results on doped GaAs layers.

2. Experimental

2.1. Motivation

Two major, well-known issues have delayed monolithic integration of III-V materials on Si. One is the lattice-constant mismatch between zincblende structure of III-V compounds and the diamond structure of Si and the other is mismatch between thermal lattice expansion as well as for optimum growth temperature. For the former, many tools have been developed to reduce defects such as dislocations and anti-phase boundaries. In the past decade, growth approaches using local nucleation enabled tremendous progress [2-4]. For the latter, a possible solution is to restrict heating to local areas of the substrate. Such local areas could serve as growth spots kept at optimum temperature for III-V growth while adjacent areas will only be moderately heated. If the resulting island exhibits reduced dimensions the total amount of incorporated mechanical stress might be reduced as well. Local heating can be readily obtained by high-power laser radiation if the laser wavelength is above the absorption edge of the substrate material. As chemical vapor deposition rates are controlled by substrate temperature due to the pyrolithic nature of the precursor decomposition it is favorable to design a reactor for laser-assisted metalorganic chemical vapor epitaxy to obtain device-quality epitaxial layer structures. Using several laser sources simultaneously a parallelization of local island growth can be envisioned, also. Here we present a reactor concept for laser-assisted metalorganic vapor phase epitaxy (LA-MOVPE) together with experimental data on GaAs growth.

2.2. Reactor setup

The design of the reactor follows general concepts as established for full-wafer MOVPE growth featuring separate units for gas mixing, reactor, control electronics, and exhaust treatment. The system is leak-tight down to $1\cdot10^{-9}$ l/m^{3}s and can operate at pressures between 10-1000 mbar at total flows of 5 slpm. Except the reactor chamber, laser heater and susceptor all parts are considered standard to vapor phase reaction systems. Recipe-based control of the epitaxial process is implemented into the programmable control electronics.

The reactor accepts 2 inch wafers which can be loaded/unloaded by opening the reactor lid into the inert atmosphere of a glovebox. Three xyz-translation stages allow to move the susceptor about 20 mm in x- and y- direction and about 5000 mm in z-direction.

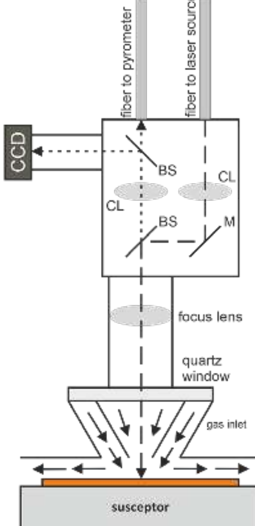

Fig. 1 Schematic of reactor including optics. BS - beam splitter; M - mirror; CL - collimating lens; CCD - camera

For heating, a commercial high-power laser module operating at 980 nm wavelength with up to 60 W output power is fiber-connected to an optics module.

Within the optics module, the viewport of a CCD camera, the optical path of a pyrometer sensor, and the laser are aligned together and fed into the reactor via an objective lens.

The pyrometer sensor is part of the laser module and provides the necessary feedback to control to laser power for a given temperature within a range of 260°C - ~2000°C. The lower limit is set by the pyrometer dark current which is of the order of 2-3 nA. A pilot laser can be used to locate the laser spot on the surface of the substrate.

Active substrate cooling is provided through the body of the susceptor by chilled water.

2.3. Temperature calibration

Temperature distribution is crucial in order to get control over crystalline quality, morphology, and composition of grown layers. As the laser provides a non-homogeneous temperature profile with a central peak pyrometric temperature measurements will yield only an average temperature which can be largely exceeded at the laser spot center depending on the spot size. Finite-element calculations of the temperature profile as due to a Gaussian laser intensity profile are used to correlate the average temperatures of the pyrometer to peak temperatures.

2.4. GaAs island growth

GaAs island growth is performed on GaAs(001) substrates using triethylgallium (TEGa) and tertiarybutylarsine (TBA) and hydrogen as carrier gas. Surface deoxidation by wet-chemcial treatment prior to loading or about 2 min in-situ thermal annealing at around 600°C under TBA is mandatory to obtain flat surface morphologies. By adjusting the z-position of the substrate surface, the island diameter can be controlled between 50-3000 µm. For diameters larger than about 300 µm, slip lines occur upon island growth within the heated area. For a given diameter of the laser spot size, the vertical island growth rate is a linear function of the input molar flow of TEGa which is mandatory for composition control. For diameters <1000 µm, the surface on a µm-scale appears smooth but featureless whereas step-terrace morphology appears for larger diameters. Auto-doping with zinc atoms from the substrates is found in micro-photoluminescence experiments. Both a vertically and radially decaying gradient of the Zn concentration can be deduced.

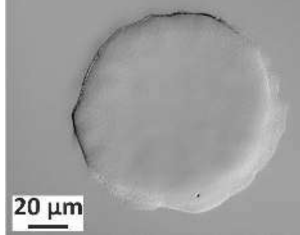

Fig. 2 Microscope image of GaAs island

Extrinsic doping is performed using a tetracarbonbromide (CBr_4) source for p-type doping and hydrogen-diluted silane (100 ppm SiH_4/H_2). For a qualitative analysis, vertical IV-measurements from the top of the island via the p-doped GaAs substrate are used. Increasingly ohmic behavior with increasing p-doping from 4 to 80 pMol/min is noticed but almost no effect upon doping with Si. The latter might be due to an underestimation of the required silane concentration in the input stream. Further growth experiments on ternary AlGaAs materials and growth on Si are being carried out.

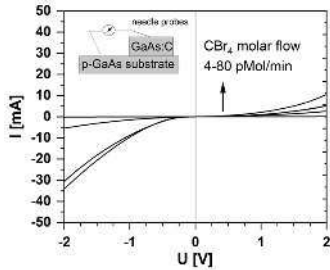

Fig. 3 IV curves for carbon-doped GaAs islands on top of p-doped GaAs substrates. Needle probes on the island and substrate surface are used.

3. Conclusions

Local epitaxy of III-V heterostructures is targeted by laser-assisted metalorganic vapor phase epitaxy. Using GaAs growth as a model system, controlled island growth with smooth surface morphologies are demonstrated. Island size is variable between 50 – 3000 µm diameter depending on laser spot size and available laser power. Doping with a carbon source yields promising ohmic IV characteristics.

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Untwinned Si (111) on Al_2O_3 (0001) Grown by Thermal Laser Epitaxy

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1. Introduction

The silicon-on-sapphire (SOS) technology is based on the epitaxial growth of a thin silicon layer (generally < 0.6 μm) on a sapphire substrate. The outstanding properties of sapphire substrates, such as their excellent electrical insulation, high thermal stability, high strength, and high radiation resistance [1], in addition to superb crystal quality and availability in large areas at economical prices lead to great attention for SOS as a promising material for CMOS technology [2]. The suitability of sapphire as a substrate for carbides, nitrides and oxides offers the prospect of using sapphire as a universal substrate, on which, starting from the highest process temperatures, mutlilayer stacks of diverse materials can be integrated for a very large spectrum of device functionalities.

The silicon layer can be deposited by a variety of film growth techniques. Pure Si source flux and oxygen-free environments are advantageous for optimizing the quality of the grown Si films. Thermal laser epitaxy (TLE) is a novel film deposition technique that uses continuous-wave lasers to thermally vaporize pure elemental sources and to heat substrates [3]. Owing to laser-induced heating, TLE enables high-temperature film growth with ultrapure source flux in a well-controlled environment.

In this study, we demonstrate the growth of Si films on *c*-plane sapphire substrates by TLE. The formation of Si (220) or of Si (111) films is found to be controllable by the substrate temperature. Remarkably, we succeeded in growing epitaxial, *untwinned* Si (111) films on *c*-plane sapphire substrates.

2. Experiment

Figure 1 shows a schematic of the TLE chamber. A focused 1070 nm fiber laser beam irradiates the top surface of a cylindrically-shaped Si source. Its evaporation rate is controlled by the power of the incident laser beam. A sapphire substrate is placed 60 mm above the Si source and is heated by a 10-μm CO_2 laser beam. The heater provides energy-efficient access to the entire stability range of the sapphire substrate from room temperature to its melting point at 2040 °C. During deposition, the chamber base pressure is $< 2\times10^{-8}$ hPa.

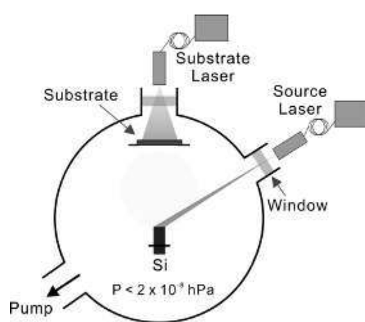

Fig. 1. Sketch of the TLE chamber

3. Results and Discussion

2.1. Thermal laser evaporation of Si

Figure 2 shows a photograph of the Si source during evaporation with a 300 W laser beam. The cylindrical solid Si source (12 mm in diameter and 8 mm in height) is locally molten by laser heating, providing an effective and ultraclean evaporation source. The rest of the source remains solid and acts as a crucible for the molten part of the Si source. Owing to the local melting and self-support, which prevents possible impurity incorporation into the source from the surrounding, the source generates an ultra-pure flux of adatoms. Further, the absence of thermal expansion mismatch of the source with a second material allows the source to be heated and cooled extremely rapidly, offering high throughput and very agile flux modulation.

Fig. 2. Photograph of a cylindrical Si source (12 mm in diameter and 8 mm in height) during evaporation.

2.2. Si thin films on c-plane sapphire substrates

We have grown Si films on c-plane sapphire substrates at substrate temperatures of 400–1200 °C. X-ray diffraction (XRD) ω-2θ patterns of the Si films are presented in Fig. 3. Up to 400 °C, the Si films are amorphous. With increasing substrate temperature, crystallized Si films begin to form. The Si (220) epitaxial orientation is dominantly observed from films grown ~ 600 °C. At higher temperatures, the Si (111) epitaxial orientation appears and becomes the dominant crystal plane in the film. At 1000 °C Si {111} planes are found exclusively. XRD φ scans confirm the fully epitaxial growth of a Si (111) film, which will be discussed later. When the temperature further increases to > 1200 °C, the Si does not remain on the substrate.

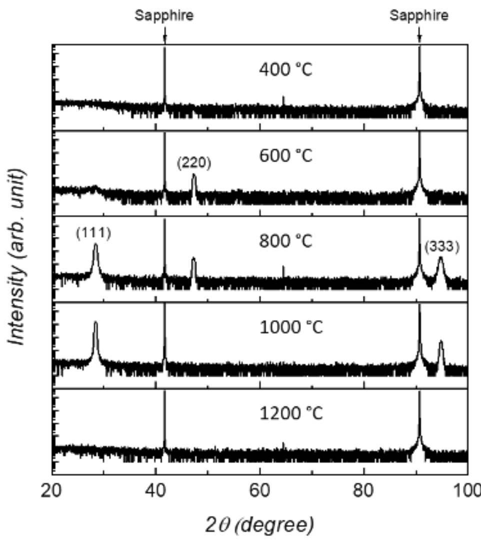

Fig. 3. XRD *ω-2θ* patterns of Si thin films grown on *c*-plane sapphire substrates at several substrate temperatures.

2.3. Untwinned Si (111) films

Fig. 4 shows the XRD *φ* scans for the Si (220) and Al_2O_3 (104) Bragg reflections of the film grown at 1000 °C, confirming the in-plane single orientation epitaxial growth of Si (111) films on the *c*-plane sapphire substrate. The (220) plane of the diamond cubic structure has a threefold symmetry, which agrees with the observed three peaks separated by 120° from each other. This confirms the absence of twinned domains in the Si film. We conclude that the high-temperature growth process of TLE leads to the untwined Si (111) growth, similar to the growth of highly (111)-oriented SiGe films on *c*-plane sapphire substrates [4], and the untwined Cu (111) films on *c*-plane sapphire substrates by high-temperature post-annealing [5] .

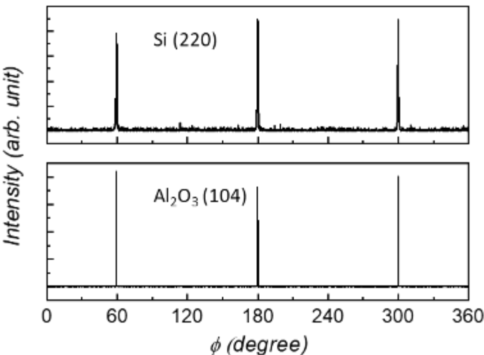

Fig. 4. XRD *φ* scan for the Si (220) and Al_2O_3 (104) Bragg reflections.

3. Conclusions

We have demonstrated the growth of Si thin films on c-plane sapphire substrates by TLE. TLE provides an ultrapure Si flux. By varying the substrate temperature, TLE enables the deposition of Si to yield amorphous, polycrystalline and epitaxial growth to even complete desorption. High-temperature TLE growth allows the growth of the untwinned Si (111) films on the c-plane sapphire substrates. Our results demonstrate the potential of TLE for the silicon and the silicon-on-sapphire technologies.

Since TLE in principle allows the co-deposition of any combination of elements of the periodic table in an extremely wide range of process conditions including, e.g., the entire range of CVD and MOCVD, we expect this method to much enhance the possibilities of Si hetero-integration.

Acknowledgements

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Si CVD Fundamentals Revisited

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1. Introduction

Si Chemical Vapor Deposition took off in the early 60s. And the first Arrhenius plot for Si deposition via silane was published exactly sixty years ago in the Journal of the Electrochemical Society, Fig. 1, [1].

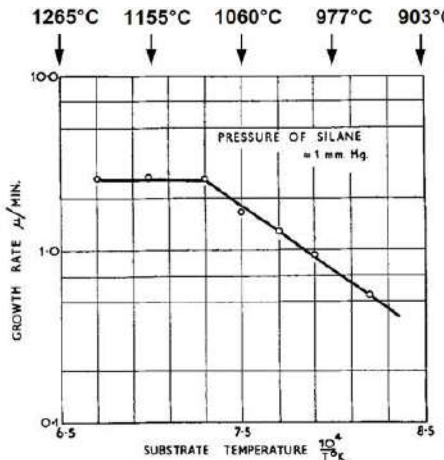

Fig. 1: Joyce and Bradley Arrhenius plot (GR vs. 1/T) for Si deposition via silane, published in 1963 in the J. Electrochem. Soc. [1]. E = 37 kcal/mol.

Since the mid-sixties, the Arrhenius plot of Si GR is still interpreted with the Deal–Grove model. In a nutshell, the GR plateau at high temperature is assigned to a growth limited by the precursor mass-transfer. And the Si GR $\propto e^{-E/RT}$ is assigned to a growth limited by chemical kinetics. The limiting reaction is the desorption of molecular hydrogen.

Transistor fabrication is the focal point of considerable materials science due to the highly competitive and profitable industry. But out of pragmatism, the industry approach to Si CVD is mostly a sensible black box approach with, at best, structured empirical strategies such as design of experiments, or trial and error problem solving.

Since the early days of CVD, a substantial chemical knowledge has accumulated across many disciplines. And to some extent, Si CVD chemistry is in a dire need of a consolidation.

An in-depth understanding of a deposition mechanism asks for the discerning review a few fundamentals, [2]. The first one is the adsorption of molecular hydrogen on crystallogens, or carbon group elements. The second one is the Thermal Decomposition of molecular precursors. The third and last is, as expected, Si CVD kinetics.

2. Chemical Review

2.1. Molecular hydrogen adsorption on crystallogens

Molecular hydrogen chemisorption on silicon is negligibly small. For all intent and purposes, $H_2(g)$ chemisorption doesn't happen. $H_2(g)$ chemisorption on Ge appears as well negligible. There are also hints chemisorption is not happening on diamond and a few group III and group V elements. Most likely, the lack of $H_2(g)$ chemisorption is a shared chemical property of p-block elements. An awareness of this chemical property is exceedingly important for the deployment of the thermochemical analysis. And it appears to have been overlooked since the inception of Si CVD.

2.2. Thermal Decomposition of Group IV hydrides

A first order reaction mechanism is shared by carbon group hydrides TD. It's demonstrated from C to Sn. Ge stands apart with an additional 0th reaction order, Fig. 2.

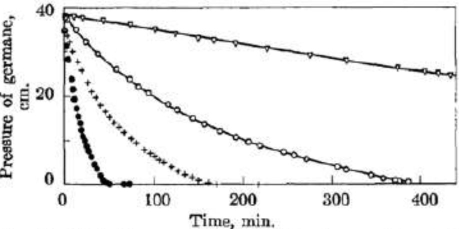

Fig. 2: Tamaru's investigation of $GeH_4(g)$ thermal decomposition. Two mechanisms are apparent with a 1st order conceding to a 0th order mechanism.

The review of the activation energy is of particular interest, Fig. 3. E(TD,Si,1) and E(TD,Ge,1) appear aligned at about 52 kcal/mol. E(TD,Ge,0) shows up about 10 kcal/mol below E(TD,Ge,1). Finally, E(TD,Sn,1) appears at about 10 kcal/mol.

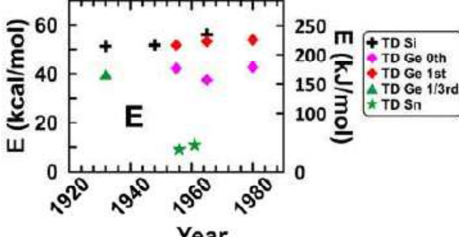

Fig. 3: Si and Ge E vs determination year.

2.3. Kinetics of crystallogen CVD

Si CVD GR is proportional to (p^n), i.e., GR $\propto p^n$; p precursor partial pressure, n reaction order. The Si industry is very familiar with the sublinear GR (n < 1) of Si depositions via $SiH_{1-x}Cl_x$, Routine Si CVD via SiH_4 appear more often than not linear, n = 1. But a sublinear GR is demonstrated in more esoteric parameter spaces. What's less emphasized is the sublinear GR n = ½, Fig. 4. The reaction order appears by no means unique. Chiang's experiments suggest repeated occurrences, Fig. 5.

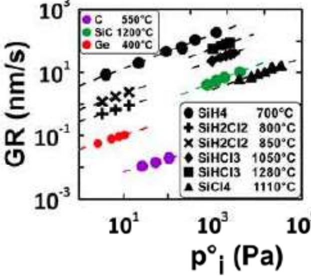

Fig. 4: Crystallogen GR vs monomeric precursor partial pressure. A reaction order n = ½ is shared by elemental crystallogen, including hexagonal SiC.

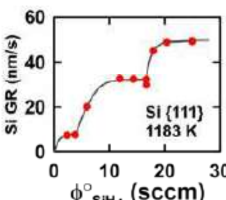

Fig. 5: Chiang's Si GR via SiH_4 with He(g) carrier gas. Repeated GR plateaus are observed.

Si CVD E(CVD, Si) is notoriously all over the place, Fig. 6. Nevertheless, a few striking features are apparent. There seem to be a double distribution with a few kcal/mol separation. Ge is most often reported about 10 kcal/mol below Si, but it's occasionally aligned with Si. E(Si,CVD) is looked at in more detail in Fig. 7. Three E(CVD, Si) are apparent in Fig. 7. The last pieces of evidence are i) Beer's report of two E(TD/CVD, αSi), ii) E(TD/CVD, αSi) ≈ 55 kcal/mol.

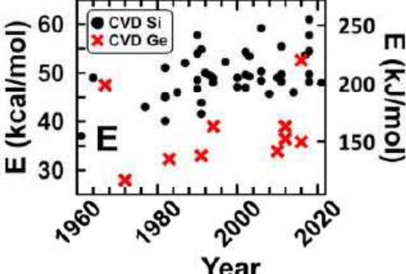

Fig. 6: E(CVD, X), X= Si, Ge.

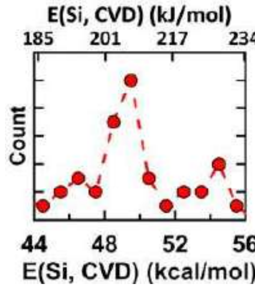

Fig. 7: Energy distribution of E(CVD,Si). 3 subgroups are apparent for E(CVD,Si), 46.5,50, 54.5 kcal/mol.

3. Conclusions

A careful consideration of the experimental facts exposed above seen through a thermodynamics lens leads to the following statements:

- Si CVD is an equilibrium deposition method
- Growth is controlled by the surface energy
- 3 reactions mechanisms are apparent (Fig. 5)
    1. Deposition under X-H bond energy control
    2. Deposition under H-H bond energy control
    3. Deposition of αSi

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Growth and Optical Characterization of SiGe QDs on Si Nano-tips

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1. Introduction

In recent years, quantum dot (QDs) devices have been widely studied due to their unique optical properties. Among several different fields of applications for QD-based lasers, light-emitting diodes, single-photon emitters, solar cells, and sensors were particularly in research focus.

However, the main challenge to improve the QDs manufacturing processes remains, which is mandatory to implement them into the next generation of CMOS-compatible devices [1]. Therefore, in our work, we performed a growth study of SiGe QDs grown on Si(001) nano-tips (NT) patterned substrates. We used the Nanoheteroepitaxy (NHE) approach to improve the quality of the grown QDs, which has the advantage of small interfaces between QDs and Si NT, reducing intermixing during growth and annealing. This concept is based on the compliance effect, strain participation between QD material and Si NT to overcome the large lattice mismatch. Further, the here present deterministic site-control of QDs significantly improved their accessibility and feasibility for future integrated technologies. Additionally, this approach allows for an efficient decoupling of strain and SiGe composition in the QDs, differently from conventional Stranski-Krastanow quantum dots.

The nanostructures were characterized using transmission electron microscopy (TEM) and micro-photoluminescence (μ-PL) spectroscopy.

2. Sample fabrication and morphology

In this investigation, we have manufactured NT-patterned Si(001) substrates using a state-of-art 0.13 μm BiCMOS technology pilot line for 200 mm wafers [2]. As the last production steps, free-standing 800 nm high Si NTs were first covered in silicon dioxide (SiO_2) using low-pressure chemical vapor deposition (LPCVD), and hereafter, the surface was polished using chemical mechanical planarization (CMP), defining in this way the Si NT´s top opening diameter of 50 nm.

The deposition of SiGe QDs on top of the Si NTs was performed by molecular beam epitaxy (MBE). Before SiGe QD growth, the pieces (1 cm x 1 cm) of Si NT substrate were wet-chemically cleaned using a combination of Piranha etch and RCA cleaning with a hydrofluoric acid dip of 10s at the end to remove native surface oxide. After loading into the MBE, the sample pieces were degassed and pre-annealed for 20 min at 790°C for degassing. The SiGe QDs growth temperature was set at 850°C. In total, four samples of homogenous almost spherical SiGe QDs with different Ge content were grown, exhibiting no visible defects in TEM (Fig.1). The average diameter of QDs is 10 nm.

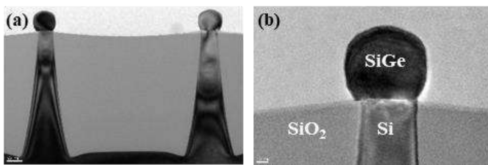

Fig. 1. A cross-sectional view of TEM image of SiGe QDs on Si NTs. The pitch size between the NTs is 0.5 μm.

3. Photoluminescence (PL)

3.1. Experimental methods

μ-PL measurements were performed with a HORIBA iHR 320 spectrometer equipped with a Synapse/Symphony InGaAs II detector, 50x objective with 1 μm spot size. In this experiment, the grating was 600 grooves/mm, which allows wavelengths from 1000 to 2000 nm to be measured. With a green laser of 532 nm wavelength, we studied the temperature and power dependence of the grown SiGe QDs on Si NT substrate. The temperature dependence was determined by using a LN2 cryostat with a power of 11.3 mW.

3.2. Results

The μ-PL spectra at 80 K for the SiGe QDs with different Ge composition is shown in Fig.2.

The energy position, intermediate between Si and Ge, suggest its origin from the SiGe QDs; no signal was observed in a bare substrate (only Si nanotips). The signal is narrowest and highest in $Si_{50}Ge_{50}$ QDs.

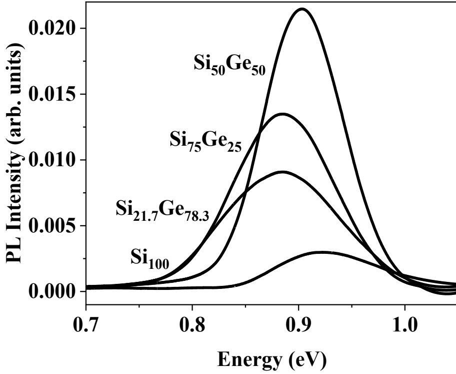

Fig. 2. µ-PL spectra of SiGe QDs different chemical composition measured at 80 K.

PL spectra were fitted with one peak using a Gaussian function. According to the fitting, we find that with increasing Ge content, the peak position shifts to the lower emission energy (Fig. 3). As for $Si_{75}Ge_{25}$ the peak position does not perfectly follow a linear composition dependence; this could be due to the lower crystalline quality of dots.

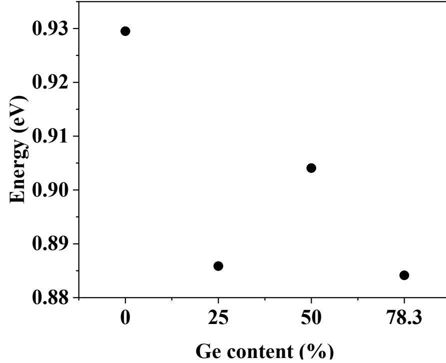

Fig. 3. µ-PL spectra of SiGe QDs different chemical composition measured at 80 K.

Temperature-dependent PL measurements were also performed for Si and SiGe QDs. We observe a clear redshift and the PL spectra becomes broader as the temperature is increased with a decrease in intensity; however, it does not follow the Varshni rule observed in Ge [3].

Furthermore, we observed a blueshift in power-dependent PL experiments (Fig. 4). The integrated PL intensity as a function of power follows a power-law relationship $I_{PL} \propto P^m$ [4]. Based on experimental data, the best-fitted values for power exponent m are in the range of 1 to 1.5, which suggests an exciton-like transition [5].

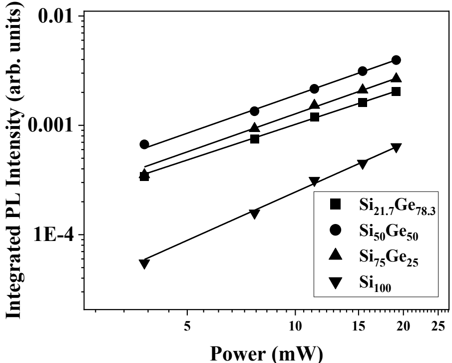

Fig. 4. PL intensity as a function of the power for Si and SiGe QDs

4. Conclusions

In summary, by the NHE approach, we have successfully fabricated SiGe QDs on Si NT. Our results demonstrate that we can use the patterned substrate to control the growth dynamics beyond the interplay of composition and size that occur in standard epitaxial growth on unpatterned substrates. These QD have excellent optical properties in terms of photoluminescence, where we also control the emission energy of a transition associated with excitons by changing the composition.

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Deposition of Sn rich islands by Molecular Beam Epitaxy

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1. Introduction

In recent years, extensive research has been carried out on the development of $Ge_{1-y}Sn_y$ hetero- and nanostructures with an aim of obtaining direct bandgap materials, which are compatible with Si/Ge technology. However, the growth of bulk $Ge_{1-y}Sn_y$ alloys can be quite challenging due to a large lattice mismatch between Ge and α-Sn (approx. 14.7%). Here, we investigate the use of molecular beam epitaxy (MBE) for the growth of Sn-rich quantum islands on Ge [1, 2]. We discuss the morphologies of islands resulting from the deposition of few monolayers (ML) of Sn on a thin Ge virtual substrate (VS) grown on a Si wafer using MBE. Our Sn-rich nanoislands have potential applications in GeSn-based optoelectronics (photodetectors and light emitters) and electronics (MOSFETs and TFETs) [3].

2. Results

The Ge virtual substrates (VS) on top of a p-doped Si (001) wafer were grown by first depositing a 50 nm Si buffer layer followed by an 80 nm Ge layer deposited at a substrate temperature of 250 °C and subjected to a subsequent annealing step. The thickness of the VS was chosen so as to facilitate future process integration for the Sn-rich dots. Transmission Electron Microscopy (TEM) images also validate the formation of a high-quality Ge-VS. The growth of Sn-rich islands was then achieved by depositing thin layers of Sn (with a deposition time of 270 s for Sample A and 380 s for Sample B) on the Ge-VS at a substrate temperature of 100 °C. The morphology of the Sn dots was obtained from AFM measurements acquired on the uncapped samples (Fig. 2).

For both samples, the deposition of Sn on the Ge surface resulted in the formation of self-assembled quantum islands. Analogously to the growth of few MLs of Ge on Si, the deposition of few MLs of pure Sn on Ge first leads to the formation of a continuous wetting layer (WL). For Sn layer thicknesses exceeding a critical thickness, a strain of the Sn layer is relaxed via the formation of three-dimensional islands (Stranski-Krastanov growth). Indeed, our AFM results show the appearance of spherical-shaped dots on top of both samples (Fig. 2). However, the different thicknesses of the deposited Sn layers result in different dot densities. For Sample A, we can see 1845 dots/μm^2 that are, on average, only 2 nm in height. On the contrary, Sample B's surface features 1274 dots/μm^2 having larger volumes. This is in agreement with previous studies carried out on the Ge/Si system, where the dot density was characterized by a reduction of the density of the dots, and increased dot size as the deposited material increased [4]. This can be quantified by plotting the diameters and the heights of the islands for the two different samples (Fig. 2).

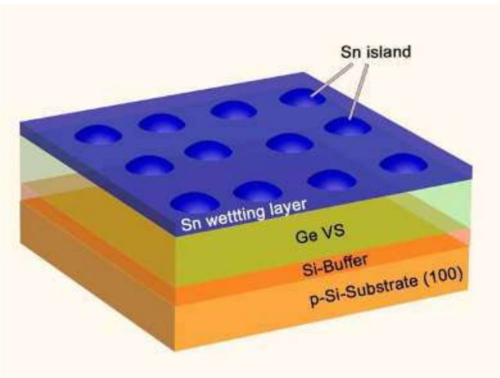

Fig. 1. Schematic view of uncapped Sn-rich islands grown on a Ge virtual substrate by molecular beam epitaxy.

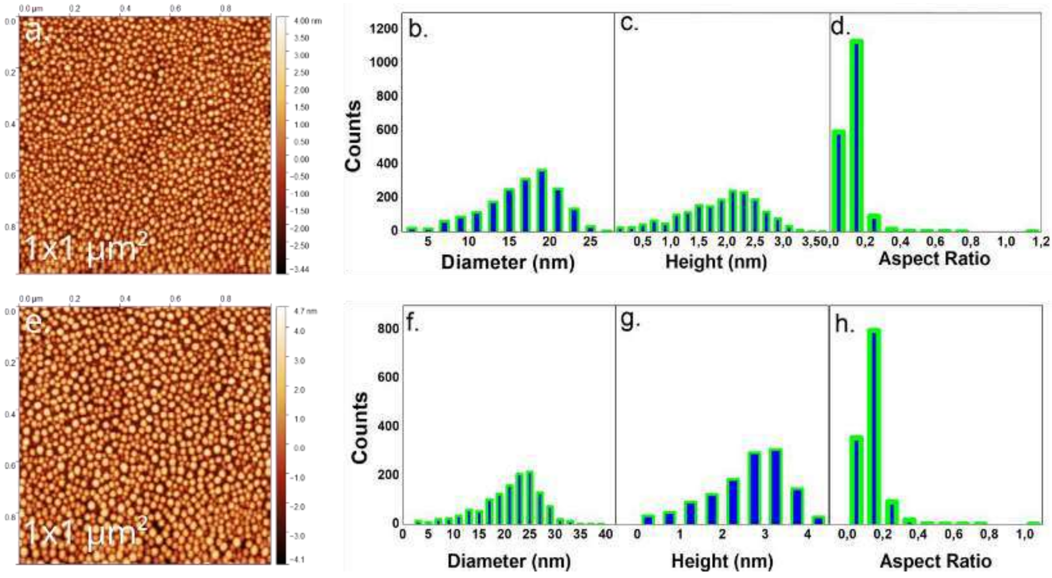

Figure 2. a) AFM image of Sample A after the formation of Sn-rich islands as can be seen from the histograms of b) diameters, c) heights, and d) aspect ratios of the dots. The AFM image e) of Sample B shows the presence of much larger dots, with histograms of f) diameters, g) heights and h) aspect ratios.

3. Conclusions

We report on the growth and characterization of Sn-rich islands on Ge virtual substrates on Si using MBE. The deposition of thin layers of Sn on Ge leads to the formation of self-assembled islands as a consequence of Stranski-Krastanov growth. We discuss strategies to utilize such structures for device applications.

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Gallium phosphide nanowires grown on SiO_2 by gas-source molecular beam epitaxy

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1. Introduction

III-V semiconductor nanowires (NWs) have drawn much attention in areas of next-generation electronics and photonics. Especially, in contrast to relaxed bulk crystals or epilayers, III-V NWs offer a better control to realize either the zincblende (ZB) or the wurtzite (WZ) crystal structures by changing the growth conditions [1]. Therefore, by reducing the dimensionality of the semiconductor material into NWs, the electronic structure can be engineered. Among III-V semiconductors, GaP has the smallest lattice mismatch with silicon and is a promising material for optical applications. However, the indirect band gap of GaP in the zinc-blende crystal structure severely limits its applications, particularly as light-emitter. Nevertheless, band structure calculations [2, 3] predicted that GaP under pressure or when grown as nanowires can have WZ structure with direct band gap. In this work, self-catalyzed GaP nanowires were grown on SiO_2 using gas-source molecular beam epitaxy (GS-MBE). The morphology of the samples was investigated using scanning electron microscopy (SEM). The structural and optical properties were characterized using micro-Raman spectroscopy, and photoluminescence (PL). Our results show that the GaP NWS grown on SiO_2 are the polytype WZ/ZB/WZ nanowires.

2. General Instructions

2.1. Experiment

GaP NWs were grown on SiO_2 substrates in a Riber 32 molecular beam epitaxy system, using thermally cracked phosphine (PH_3) as gas source and solid gallium (Ga) source.

2.2. Results and discussion

Fig. 1 is the plan-view SEM image of a sample after 2 hours growth of GaP. The randomly distributed nanocrystals on the SiO_2 surface are GaP particles. Nanowires with a length up to 20 µm are distributed irregularly with large spacings between them.

One can scan a single NW to identify the structural information and phase purity. Fig. 2(a) displays Raman spectra along a representative GaP nanowire with a length of 7 µm. The inset in Fig. 2(a) shows the optical image of this nanowire. According to the Raman spectra the E and E_2^H modes (78.1 cm^{-1} and 355.8 cm^{-1}), associated with the WZ phase, appear at the beginning and the end of the NW. The data indicate that the lower part of the NW is in WZ phase, transforming later into ZB phase, and finally ending the growth in the WZ phase. Fig. 2(b) is a typical Raman spectrum of WZ GaP, taken from the bottom of the NW. The Raman results are a clear indicator of the existence of WZ phase in the single GaP nanowires.

For exploring the optical emission of the GaP nanowires, PL measurements were carried out. Fig. 3(a) shows the PL spectrum of an ensemble of GaP nanowires on the SiO_2 substrate, measured at 9 K and excited by a 458 nm laser with a power density of 100 W/cm^2. Trap-bound excitons can explain the observed peak at 2.14 eV. The emission energy of this peak, E_{PL} is related directly to Eg, the WZ band gap (Γ_{9v}-Γ_{8c}) energy, E_{PL}= Eg-ΔE, where ΔE is the sum of the free exciton energy and the binding energy of the free excitons to the trap centers [4]. The peak at 2.31 eV is, on the other hand, a direct observation for the indirect band gap from Γ to X-minimum at 9 K ZB GaP, showing that the ZB GaP phase is definitely present in the ensemble of nanostructures, too.

Photoluminescence measurements in the temperature range between 10 K and 300 K were performed shown in Fig. 3(b). According to the temperature-dependent bandgap equation due to electron- phonon coupling (Eq. 1) [5], with increasing temperature, the band gap becomes narrow. Eq. 1 describes this model,

$$\mathrm{Eg}(T) = \mathrm{E0} - \mathrm{S}\langle\hbar\omega\rangle\left(coth\left(\frac{\langle\hbar\omega\rangle}{2kBT}\right) - 1\right)$$

where Eg(T) is the bandgap at temperature T, S is a dimensionless material constant which is a measure of strength of electron-phonon coupling, k_B is the Boltzmann constant, and <ħω> is average phonon energy. Since the binding energy of excitons and the trap energy are not temperature dependent, we can use this model (Eq. 1) to fit the temperature dependence of the PL peak at 2.14 eV as shown in Fig. 3(c). The equation leads to an excellent fit with values of S= 2.66, <ħω> = 17.24 meV, and E_0 = 2.143 eV.

The exciton binding energy △E can be investigated by temperature dependence of the light output associated with the trap-bound exciton system. We apply the Arrhenius model to estimate the activation energy [6]. The integrated PL intensity of the energy peak at 2.14 eV as a function of temperature can be described by (Eq. 2):

$$I = \frac{I_0}{1 + A\exp(-E_a/k_B T)}$$

where A is the non-radiative recombination process coefficient, k_B is again the Boltzmann constant, and Ea is the activation energy for thermal dissociation of the bound excitons. Fig. 3(d) shows the integrated PL intensity as a function of $1/k_BT$ and the fitting curve using the Arrhenius equation, which results in a thermal activation energy of 31±3 meV for trap-bound excitons in wurtzite GaP nanowires. We approximately considered it as the exciton binding energy, leading to an estimated band gap energy of about 2.174±0.003 eV at 0 K.

3. Conclusion

In summary, GaP nanowires were successfully grown on SiO_2 substrates by GSMBE. The Raman study on individual nanowires showed that one type of NWs is WZ-base/ZB main-body/WZ-end. At 10 K, the estimated direct band gap energy for the WZ phase is about 2.171 eV and the indirect band gap energy of the ZB phase is about 2.31 eV.

Acknowledgments

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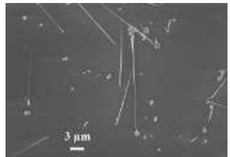

Fig. 1 SEM image of GaP Nanowires grown on SiO_2.

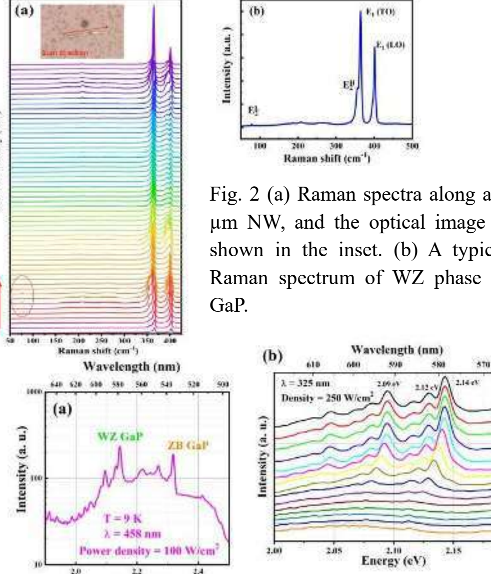

Fig. 2 (a) Raman spectra along a 7 μm NW, and the optical image is shown in the inset. (b) A typical Raman spectrum of WZ phase of GaP.

Fig. 3 (a) PL spectrum at 9 K. (b) Temperature-dependent PL spectra. (c) Emission energy at 2.14 eV and corresponding curve fitted with Eq. 1. (d) Integrated PL intensity of the emission peaked at 2.14 eV as a function of $1/k_BT$ and fitting curve according to Eq. 2.

Heteroepitaxial Growth of High Substitutional Sn-content $Ge_{1-x}Sn_x$ Layer Lattice-matched on InP Substrate

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1. Introduction

$Ge_{1-x}Sn_x$ with a high Sn content over 10% has been attracted as a direct-transition group-IV semiconductor for electronic, optoelectronic, and thermoelectric applications [1, 2]. In addition, increasing the Sn content as high as 20-30% extends the potential for infrared optoelectronic applications with shrinking the energy bandgap by a few 0.1 eV. However, it is not so easy to realize such a high substitutional Sn content due to the limitation of the thermal-equilibrium solid solubility of Sn in bulk Ge, which is as low as 1%.

One of the key factors for increasing the substitutional Sn content in $Ge_{1-x}Sn_x$ is reducing the strain in a $Ge_{1-x}Sn_x$ heteroepitaxial layer grown on a substrate [3]. The reduction of the strain energy in a $Ge_{1-x}Sn_x$ epitaxial layer enhances the substitutional Sn content extensively over the thermal-equilibrium limit. Practically, we previously achieved the heteroepitaxy of a $Ge_{1-x}Sn_x$ layer with a substitutional Sn content as high as 26% on a InP substrate having a large lattice constant of 0.58686 nm that is lattice-matching to that of unstrained $Ge_{1-x}Sn_x$ with the Sn content [4].

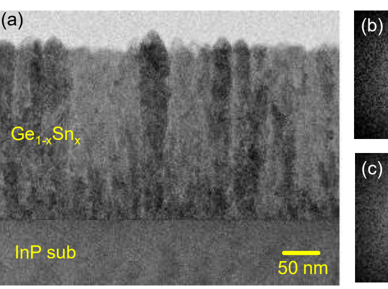
On the other hand, in our previous report, the crystalline quality of the $Ge_{1-x}Sn_x$ layers is not so high as twin growth with a high dislocation density is observed in the layers. It is necessary to understand the epitaxial growth behavior and establish the heteroepitaxial growth technology of a very-high-Sn-content $Ge_{1-x}Sn_x$ layer on a large-lattice-constant substrate for practical applications. In this study, we investigated the influence of the surface condition, growth temperature, and layer thickness on the crystalline structure and morphology of $Ge_{1-x}Sn_x$ layers on InP substrates.

2. Sample preparation

InP(001) wafer was used as substrate. After chemical cleaning of the substrate using diluted H_2SO_4 solution and deionized water, the wafer was annealed at 340 or 380 °C in an ultra-high vacuum (UHV) chamber for surface cleaning. Then, a $Ge_{1-x}Sn_x$ layer was deposited at a substrate temperature from 50 to 100 °C using molecular beam epitaxy (MBE) method. Ge and Sn were deposited with individual Knudsen cells. The target Sn content was as high as 26%. The thicknesses of $Ge_{1-x}Sn_x$ layers were ranging from 100 to 200 nm.

3. Results and discussion

First, we investigated the influence of the surface cleaning temperature of InP on the growth of $Ge_{1-x}Sn_x$ layer. The $Ge_{1-x}Sn_x$ layer grown at 100 °C on the InP substrate cleaned at 340 °C shows the domain growth with the twin and polycrystalline structures as shown with transmission electron microscopy (TEM) observation (Figs. 1(a)-(c)), while the surface morphology looks uniform with suppressing the Sn precipitation. In contrast, the $Ge_{1-x}Sn_x$ layer grown at 100 °C on InP cleaned at a higher temperature of 380 °C exhibits better epitaxial



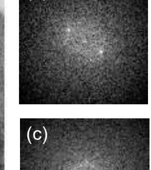


Fig. 1 (a) The cross-sectional TEM image of $Ge_{1-x}Sn_x$ layer grown on InP thermally cleaned at 340 °C. Fast Fourier transform patterns of $Ge_{1-x}Sn_x$ regions (b) near the surface and (c) interface.

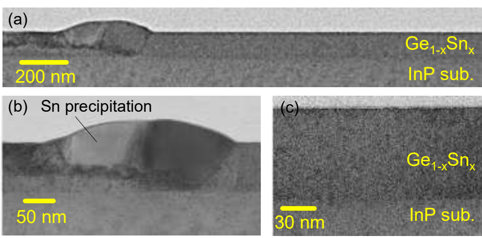


Fig. 2 (a) Cross-sectional TEM images of $Ge_{1-x}Sn_x$ layer grown on InP thermally cleaned at 380 °C. Enlarged images of (b) Sn precipitation and (c) uniform epitaxial growth regions.

growth regions with a substitutional Sn content as high as 25%, although we can find regions where the low-Sn-content $Ge_{1-x}Sn_x$ growth with significant Sn precipitation takes place (Figs. 2 (a)-(c)).

Our observation using microscopic Raman scattering spectroscopy and energy dispersive X-ray spectroscopy analyses revealed that a higher temperature cleaning at 380 °C for InP substrate realizes a clean surface preferential for the uniformly epitaxial growth of a $Ge_{0.75}Sn_{0.25}$ layer (*not shown*). However, dot-like In precipitations were also simultaneously formed with the UHV annealing probably due to the desorption of P atoms from the InP surface with annealing and those enhances significant Sn precipitation during the $Ge_{1-x}Sn_x$ growth.

Thus, we examined lowering the growth temperature from 100 to 50 °C. Figures 3 and 4 show the X-ray diffraction two-dimensional reciprocal space mapping (XRD-2DRSM) and $2\theta/\omega$ profile results, respectively, for the $Ge_{1-x}Sn_x$/InP sample with a growth temperature as low as 70 °C. We can clearly observe the diffraction peak of the epitaxial $Ge_{0.73}Sn_{0.27}$ layer near that of InP substrate. This layer is pseudomorphicaly grown on the substrate with a small in-plane compressive strain. Thickness fringes are also clearly observed in the $2\theta/\omega$ profile (Fig. 4), indicating that an atomically flat and uniform inter-

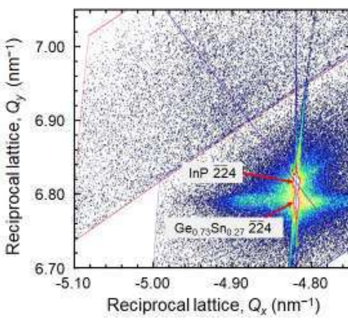


Fig. 3 The XRD-2DRSM result of the $\bar{2}\bar{2}4$ Bragg reflection for the $Ge_{1-x}Sn_x$/InP sample with a growth temperature of 70 °C.

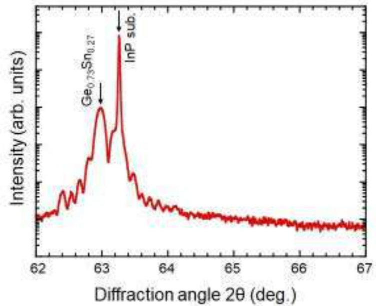


Fig. 4 The XRD $2\theta/\omega$ profile for the $Ge_{1-x}Sn_x$/InP sample with a growth temperature of 70 °C.

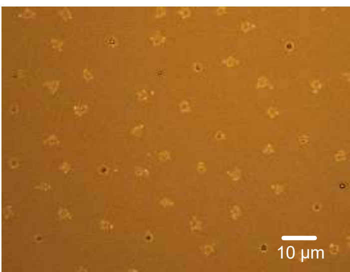


Fig. 5 The optical microscope image of the $Ge_{1-x}Sn_x$/InP sample with a growth temperature of 70 °C.

face should be formed between the $Ge_{0.73}Sn_{0.27}$ layer and InP substrate.

Figure 5 shows the optical microscope image of the $Ge_{0.73}Sn_{0.27}$/InP sample. We can observe the formation of a uniform and flat $Ge_{0.73}Sn_{0.27}$ epitaxial layer on the almost wide region with a few 10 μm size, although precipitations consisting of Sn and In due to the surface cleaning mentioned before.

4. Conclusions

We investigated the heteroepitaxial growth of $Ge_{1-x}Sn_x$ layer with a Sn content higher than 25% on InP(001) substrate. The lattice-matching growth of $Ge_{1-x}Sn_x$ heteroepitaxial layer on InP substrate is achieved without twin or polycrystalline growth on a properly cleaned substrate. The present result indicates that a homogeneous high-Sn-content $Ge_{1-x}Sn_x$ epitaxial layer should be obtained using an completely uniform InP surface without In precipitation. The lattice-constant engineering for $Ge_{1-x}Sn_x$ epitaxy opens up the potential technology for a novel nanomaterial of $Ge_{1-x}Sn_x$ beyond the thermal-equilibrium limitation.

Acknowledgements

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SiGe Fabrication on Si by Al induced liquid phase epitaxy using screen-printing Al-Ge paste

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1. Introduction

The integration of III-V semiconductors and multi-junction solar cells on silicon (Si) substrate is a challenging task due to multiple problems. The top on the list is the significant difference in lattice constants between the III-V semiconductors such as Gallium Arsenide (GaAs) and Indium Phosphide (InP) and lattice constant of Si. This mismatch causes strain in the grown III-V layers leading to multiple defects at the interface causing significant degradation in the grown III-V's electronic properties [1].

For high efficiency multi-junction solar cells fabrication on Si, many researchers have been working to overcome these problems and developed methods for integrating III-V semiconductors on silicon substrates such as wafer bonding [2], lift-off [3], SiGe/Ge thick sacrificial buffer layer growth [4] and SiGe bottom cells on Si with buffer layers [5] are some of the approaches that have been introduced.

In this context, SiGe buffer layers are one of the most suitable approaches to relax the lattice mismatch between Si and III-V solar cell layers, and their fabrication methods have been intensively studied by various groups using molecular beam epitaxy (MBE), chemical vapor deposition (CVD) and liquid phase epitaxy (LPE) methods [6]. However, obtaining good crystallinity of SiGe with these conventional processes requires the use of expensive gases, large furnaces and special vacuum equipment. Therefore, there is a need for another SiGe fabrication method that utilizes a low-cost, simple, and fast processing. We investigated the liquid-phase growth of SiGe layers on Si substrates mediated by an alloying process using aluminum-germanium (Al-Ge) mixed paste. This method is a simple process using a conventional screen-printer and a furnace [6], and it has been confirmed that, uniform SiGe layers with a thickness of more than 20 μm can be formed in a short processing time [7].

In this study, we will investigate the effect of gas ambient during annealing on the growth of SiGe layers and monitor the crystal state changes taking place during the formation process by measuring the crystal transformation during annealing by in situ XRD-2D measurements.

2. Effect of gas ambient during annealing on the growth of SiGe layers

The Al-Ge paste was screen-printed onto the n-type Si (111) substrate at an areal density of 0.1 mg/mm^2 and dried at 100 °C to form a thick paste matrix. The annealing temperature was ramped up to 1000 °C at 5 °C/s and then cooled naturally. The ambient gases used during annealing were air, oxygen (O_2), nitrogen (N_2), argon (Ar) and atmosphere containing 0.05 % to 1.0 % oxygen mixed with Ar. The oxygen concentration in the annealing furnace was measured with an oxygen analyzer connected to the exhaust port from the chamber. The SiGe layers formed on samples annealed under each condition were observed by cross-sectional scanning electron microscopy (SEM) and analyzed by energy dispersive X-ray spectroscopy (EDX). The SEM cross-section images of printed samples with Al-Ge paste and annealed under air, O_2, N_2 and Ar ambient are shown in Fig. 1. Al particles normally have a native oxide film, and as the temperature rises, cracks appear in the native oxide film due to thermal expansion. When Al cracks are in contact with Si and Ge, they partially form a liquid phase of alloying and a path for atomic transfer. In an oxygen-containing ambient, the contact points between Al and Ge and Si are reduced and the atom transfer paths are restricted by oxidation. In the samples annealed in air and O_2 ambient, Al and Ge powder shapes remain in all paste matrix layers. This suggests that the oxide film thickness was increased suppressing the reaction with Si and Ge. And consequently resulting in thin and non-uniform SiGe layer. Since the nitrogen also reacts with Al at high temperatures, but with slower rate than that of oxygen, the SiGe layer of more than 20 μm was formed, although it was not uniform, and there were areas where the Al powder shape remained at the top of the Al-Ge paste matrix. In an Ar ambient, the cracks due to thermal expansion are not oxidized, and the contact points between Al, Ge, and Si are increased, which is assumed to promote the formation of the Al-Ge-Si alloy liquid phase.

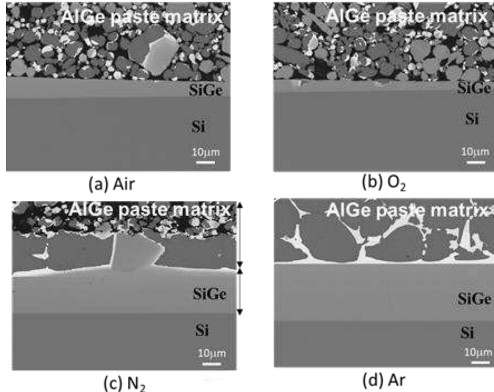

Fig.1 The formed SiGe thickness vs gas ambient

3. In-situ X-ray diffraction analysis of liquid phase of SiGe grown on Si

Two types of Al-Ge pastes were screen-printed on Si (111) wafers. The first one was made by adding Al and Ge powders to a vehicle devised for screen-printing. The second paste was made by adding an Al-Ge alloy powder. Figure 2 shows the XRD intensity extracted from measured 2D maps center. In the case of the sample fabricated using the paste mixed of Al and Ge powders, crystal peaks other than Si (111) and Si (333) on the substrate disappear between 530°C to 540°C as can be seen in Figure 2(a), indicating that both Al and Ge are indeed in the liquid phase up to the peak temperature of 900°C. The XRD spectrum at 800°C after cooling down from 900°C, shows that the SiGe peak appears, followed by the reappearance of the Ge (111) and Ge (333) peaks at 430°C. In the case of the sample fabricated with the Al-Ge paste formed using the Al-Ge alloy powder in Figure 2(b), the XRD peaks of Al and Ge at the paste matrix are small, because the powder was already alloyed in the initial state. Furthermore, the Al and Ge peaks appear as the Al and Ge crystal structure might be altered in the Al-Ge alloy powder as the local Ge crystals form larger inclusions inside the powder when heating to 420°C. From 420°C to 430°C, the Al and Ge peaks of the paste matrix disappeared and the Al-Ge alloy turned into liquid phase. The change in the peak of SiGe growth during cooling from 900°C is similar to Figure 2(a), with the SiGe peak and the Ge peak appearing at 430°C. It is noted that the intensity of the SiGe and Ge peaks are stronger for the samples prepared with Al-Ge alloy paste. This is considered to be due to the fact that the Al-Ge alloy powders are in the liquid phase at lower temperature, which creates more contact points between the Al and Ge inside the alloy powder and, consequently, the Si substrate, increasing the interaction paths of the elements and making the SiGe epitaxial growth easier.

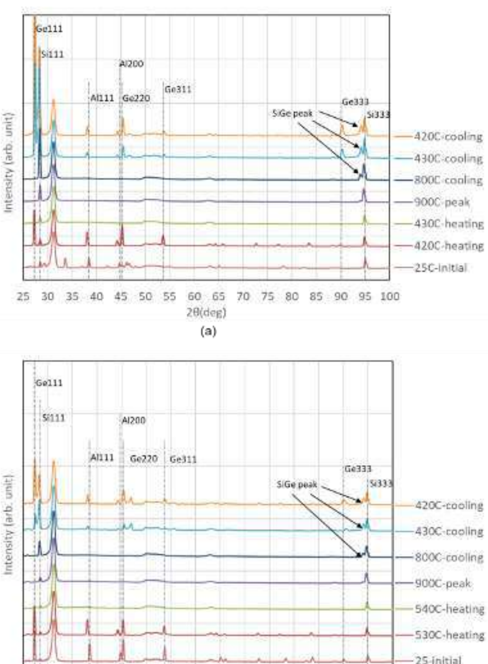

Fig.2 In-situ XRD measurement results extracted from the 2D map center of the samples fabricated using Al-Ge paste with Al and Ge powder (a) and Al-Ge alloy powder (b).

4. Conclusions

Liquid-phase growth of SiGe epitaxial layers were formed on Si substrates by screen-printing Al-Ge paste and high-temperature annealing. Oxidation of the Al particle surface restricted the contact points for alloying Al, Ge and Si. From the In-situ X-ray diffraction analysis we found that the liquid phase began to form at lower temperatures when the Al-Ge alloy powder was used, which is expected to improve the uniformity of the composition in the liquid phase.

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Fabrication of crack-free strained SiGe/Ge multiple quantum wells on Ge-on-Si(111) by the patterning method

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1. Introduction

Recently, Ge-based light emitters have been attracting increased attention toward the realization of on-chip optical interconnection, Although Ge is an indirect-band-gap semiconductor like Si, it is expected that strong direct-transition luminescence can be obtained from tensile-strain induced Ge-on-Si. We have previously reported highly efficient room temperature EL emission from strained Ge-on-Si p-i-n diodes[1]. Further increase in luminescence intensity and control of emission wavelengths are expected to be made possible by introducing quantum well structures in the active layer, where fabrication of high-quality strained SiGe layers on Ge is essential. However, critical thickness limits the total growth thickness and numbers of strained layers, which hinders various applications of the SiGe/Ge quantum wells. We have succeeded in fabricating a strained SiGe layer that is much thicker than the critical thickness by means of a patterning method[2]. In this study, we report on the fabrication of strained SiGe/Ge multiple quantum wells on Ge-on-Si(111) by the patterning method and demonstrate improved crystallinities and optical properties.

2. Experiments

Sample structures fabricated in this study are shown in Fig. 1. The crystal growth of $Si_{0.1}Ge_{0.9}$/Ge multi quantum wells (MQWs) on Ge-on-Si was carried out with solid source molecular beam epitaxy (MBE). The Ge-on-Si was fabricated using the so-called two-step growth method. First, a low-temperature (LT) Ge layer of 40 nm was grown on a p-type Si(111) substrate at 400°C. Subsequently, a high-temperature (HT) Ge layer of 500 nm was grown at 700°C, followed by annealing at 800°C for 10 min. Mesa patterns were formed on the fabricated Ge-on-Si (111) substrates by photolithography. After patterning, 50 nm thick Ge buffer layer ware grown on a Ge-on-Si(111), and P-doped MQW layers consisting of 6 nm $Si_{0.1}Ge_{0.9}$ barrier and 10 or 12 nm Ge well layers were grown with 15 cycles at 350°C.

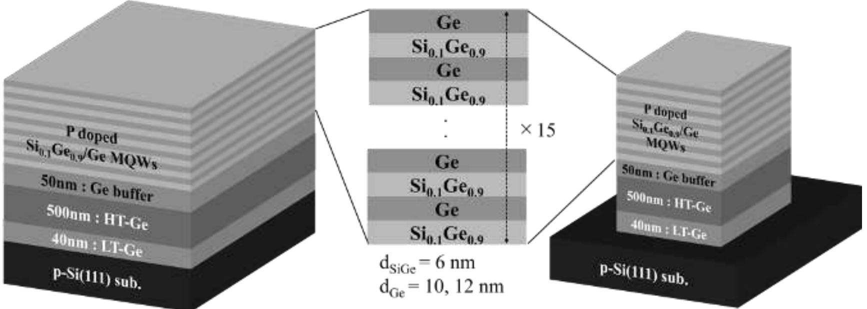

Fig. 1 $Si_{0.1}Ge_{0.9}$/Ge MQWs grown on Ge-on-Si (111) with and without patterning.

3. Results and discussion

Figures 2 show laser microscope images of the fabricated $Si_{0.1}Ge_{0.9}$/Ge MQWs on Ge-on-Si(111) samples. Several cracks were clearly observed on the sample without patterning. On the other hand, cracks were absent on the sample with patterning. We consider that crack generation and propagation can be highly suppressed by the mesa patterning [2].

Figure 3 shows results of X-ray-diffraction ω-2θ scans for $Si_{0.1}Ge_{0.9}$/Ge MQW on Ge-on-Si(111). We can see periodic peaks originated from the MQWs, which indicates that the multi layers have high crystallinity and abrupt interfaces. Peak shifts were observed between the two samples. For the un-patterned sample, the relaxation ratio was estimated to be 12%. Additionally, for the patterned sample, small peaks are seen around the left side of the strong MQWs peaks. These are considered to come from MQW layers grown outside of the mesa.

Figure 4 shows the photoluminescence (PL) spectra of $Si_{0.1}Ge_{0.9}$/Ge MQWs on Ge-on-Si(111) at room temperature. Strong PL peaks owing to quantum confinements are observed, and an increase in the PL intensity and peak red-shift with increasing Ge well layer thickness are clearly obtained. Figure 5 shows comparisons of PL intensity and peak energies between the samples with and without patterning. The patterned MQWs exhibits a larger peak intensity and lower peak energy than un-patterned MQWs, which is attributable to the strain relaxation due to the crack generation.

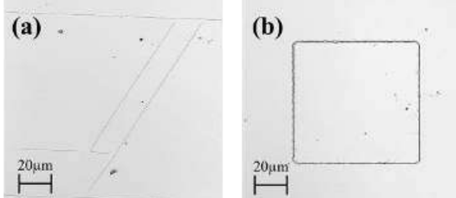

Fig. 2 Laser microscope images of the fabricated $Si_{0.1}Ge_{0.9}$/Ge MQWs on Ge-on-Si(111) (a) without and (b) with patterning.

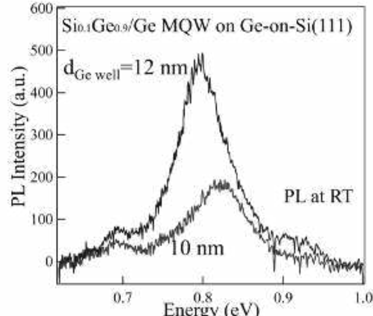

Fig. 4 Photoluminescence (PL) spectra of $Si_{0.1}Ge_{0.9}$/Ge MQWs on Ge-on-Si(111) at room temperature.

4. Conclusions

We fabricated strained $Si_{0.1}Ge_{0.9}$/Ge MQWs structures on Ge-on-Si(111) by the patterning method. As a result, it was demonstrated the patterning can suppress crack formation in the MQWs. It was confirmed from XRD measurements that high-quality $Si_{0.1}Ge_{0.9}$/Ge MQWs were fabricated with the patterning, and strong PL was obtained at room temperature, indicating that the suppression of crack formation by the patterning method is very useful toward SiGe/Ge MQW embedded light-emitting device applications.

Acknowledgements

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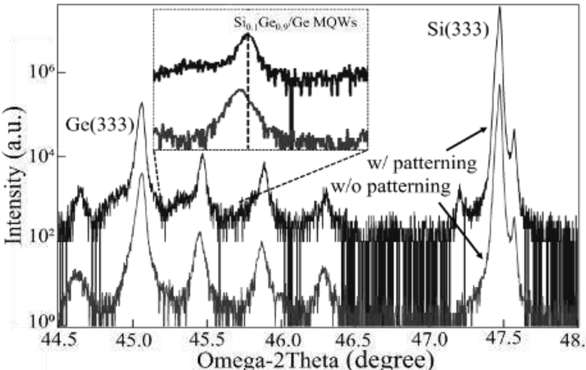

Fig. 3 Measurement of X-ray-diffraction ω-2θ scans for $Si_{0.1}Ge_{0.9}$/Ge MQW on Ge-on-Si(111) with and without patterning.

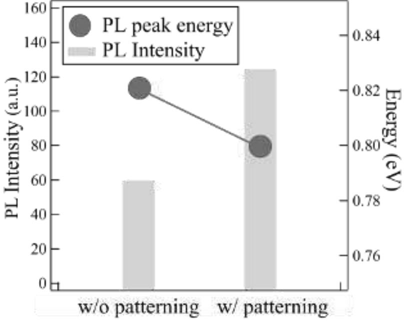

Fig. 5 PL intensity and peak energies between the samples with and without patterning.

Van der Waals heteroepitaxy of Xene 2D materials on graphene/6H-SiC

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KEYWORDS: 2D materials, Silicene, Graphene, Van der Waals heterostructure, Molecular Beam Epitaxy, nucleation and growth, kinetic Monte-Carlo

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1. Introduction

Homogeneous and heterogeneous dewetting processes of Silicon (Si), Germanium (Ge) and SiGe when deposited on SiO2, has been investigated for various applications in silicon photonics and microelectronics, and in particular for the fabrication of resonators. The developed approach allowed the fabrication of self-organised arrays of defect-free and faceted islands that are much smaller than the initial nominal resolution. In addition, appropriate substrate nanostructuring has enabled the scattering properties of the objects created as well as the structural colouration and contrast between the scattering maxima and minima of individual resonant antennas. The results have great interest for photonic applications, while using fully dielectric photonic devices. In parallel, we have invesigated in recent years the fabrication of Van der Waals heterostructures with the development of silicene and germanene on graphene (Gr).

2 Results

In this study, we have developed a new process combining dewetting and 2D materials (silicene and germanene) on graphene. We have also investigated the growth of Gr on Germanium (and on Ge on insulator) substrate for heterogeneous integration of 2D materials in Si-based microelectronic systems. The silicene, germanene and graphene layers are deposited on Ge by molecular beam epitaxy (MBE). Results on the characterisation of the 2D layers (silicene, germanene and graphene) obtained by MBE will be presented. We will also present the dewetting of Si and Ge layers on Gr as a function of the deposition/annealing temperature and the thickness of the deposited layers. The dewetting can be controlled by nanostructuring the surface either before or after Si (Ge) deposition. This study is of fundamental importance for various applications, including the optical manipulation of droplet arrays and/or single droplets. The aim is to determine the wetting dynamics on graphene surfaces in order to control the wetting/dewetting states and to quantify the wettability of the Gr as a function of its thickness, the underlying substrate, and the experimental deposition conditions. With this study, we bring new results on the wettability of Gr which is so far misunderstood with a large debate on the origin of the contact angle differences, since most studies show that, due to the atomic thickness of graphene, the underlying substrate has a critical effect on the apparent wettability of graphene. On the other hand, different external factors can alter its surface state: 1) fundamental substrate effects and 2) environmental effects. Fundamental substrate effects include the effects of polarity and substrate doping, but they are often altered by environmental effects (polycrystalline graphene with domains of different sizes and orientation, contaminations, etc.).

3. Conclusions

We will give some insights on the structural and morphological evolution of Si (Ge) droplets (SiGe) by TEM, EDX, and GPA. In addition the optical properties of droplets as a function of their size and morphology will be described. In parallel, simulations of the dewetting process of Si (and Ge) on Gr give a

better understanding of the morphological evolution. The optoelectronic characteristics of the Si (Ge) droplet arrays obtained by substrate nanostructuring are very promising for several applications .

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From Plastic to Elastic Relaxation in SiGe Microcrystals

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1. Introduction

The epitaxial growth of germanium on silicon is a key technological step in electronics and photonics. However, the mismatch in lattice parameter and thermal expansion coefficients results in defective epitaxial layers and reduced device performance.

A novel approach, named vertical heteroepitaxy (VHE), has been recently demonstrated to address these issues [1]. VHE employs deep patterning of Si pillars of micrometric lateral size to obtain the vertical growth of a self-assembled array of Ge micro-crystals by Low-Energy Plasma-Enhanced CVD (LEPECVD). Such crystals have been demonstrated to be fully relaxed and have a high crystalline quality, while featuring the complete expulsion of threading dislocations.

It has also been predicted that, for suitable values of the lateral size of silicon pillars, fully relaxed dislocation-free microcrystals may be achieved [2]. However, this effect has only been experimentally demonstrated for 27 μm tall composition-graded SiGe microcrystals grown on 2 μm wide silicon pillars [3].

In this work we report the dislocation-free growth of fully relaxed SiGe microcrystals with a constant 10% Ge content and a much smaller thickness of 5 μm on silicon pillars with a sub-micrometric lateral size.

2. Epitaxial deposition and dislocation analysis

2.1. Substrate fabrication and growth

Standard silicon wafers have been patterned by e-beam lithography followed by ICP-RIE. The Si pillars have a lateral size ranging from 250 nm to 2 μm and are separated by trenches 2.7 μm deep and with a width ranging from 500 nm to 2 μm. The sidewalls of the Si pillars are oriented along the (110) direction.

The substrates have been cleaned following the standard RCA process and the native oxide has been removed by an HF dip before the epitaxial deposition. The growth of a 200 nm Si buffer followed by 5 μm of SiGe 10% has then been carried out in a LEPECVD reactor at a substrate temperature of 650°C and a growth rate of ~5 nm/s.

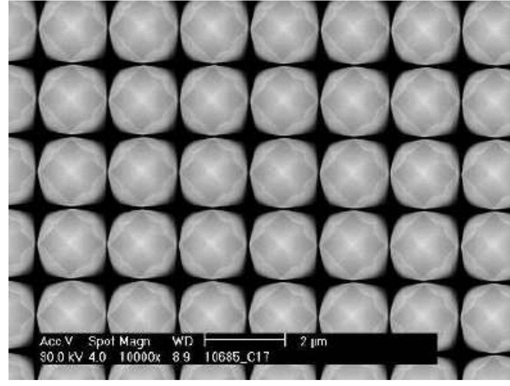

Figure 1 SEM top views of 5 um SiGe 10% microcrystals grown on 250 nm wide silicon pillars separated by 1.5 um wide trenches.

2.2. TEM analysis

Samples grown on three different substrates have been selected for further analysis to probe three different relaxation regimes: full elastic relaxation (Si pillars 250 nm wide separated by a gap of 1.5 μm), partial plastic relaxation with few dislocations (Si pillars 2 μm wide separated by 2 μm gap) and fully plastic relaxation (standard flat Si substrate).

SEM images of the TEM lamellae are shown in Fig. 2, together with TEM dark-field images taken at the (004) reflection. The results are in clear agreement with the theoretical predictions: no dislocations can be observed in the sample with the smallest pillar size, larger pillars show a few dislocations. In the flat sample an array of dislocations can be noticed, whose period is in agreement with the plastic relaxation theory.

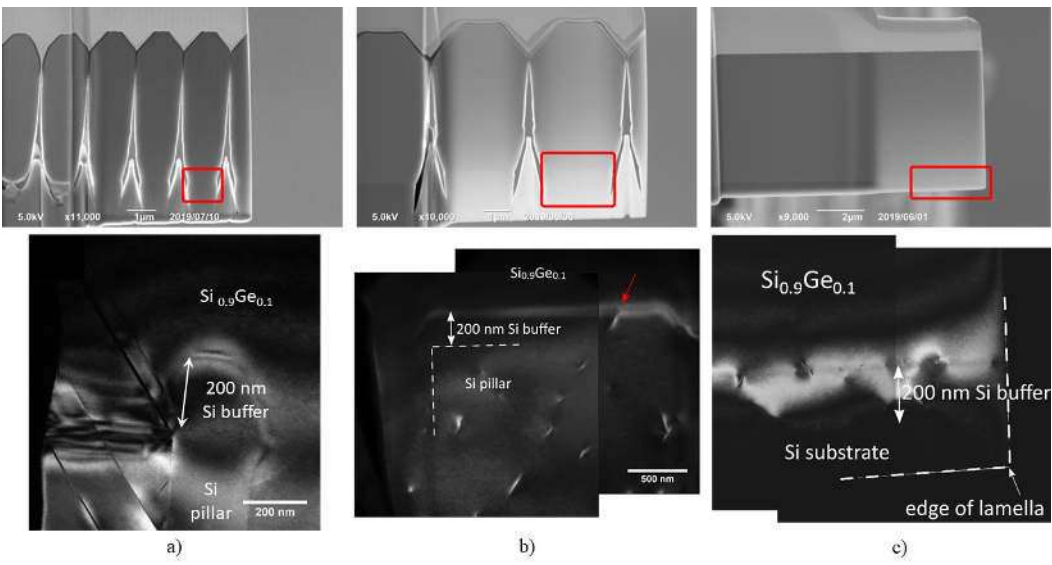

Figure 2 SEM image of TEM lamellae and DF TEM images taken at the (004) reflection of 5 um SiGe 10% grown on a 200 nm Si buffer on a) Si pillars with a lateral size of 250 nm separated by 1.5 um wide trenches, b) 2 um Si pillars separated by 2 um trenches and c) a flat Si substrate.

2.3. Photoluminescence measurement

The presence of dislocations has also been investigated by continuous-wave photoluminescence measurements performed at 5K with a 1064 nm excitation at a power density of 325 W/cm^{-2}. The PL spectra of the three samples are compared in Fig. 3.

The feature of interest are the D1-5 peaks, which are related to dislocations in the SiGe system. It can be clearly observed that the intensity of the peaks is quite large in the flat region of the sample, small for the larger pillars and almost completely disappear in the case of sub-micrometric pillars. The small features which can still be seen can be possibly due to the signal collected from the material grown in the trenches between the Si pillars.

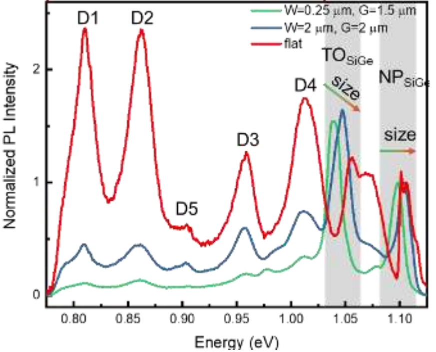

Figure 3 Photoluminescence spectra acquired at 5K with 1064 nm CW excitation showing decreasing dislocation-related peaks as the size of the Si pillars decreases.

3. Conclusions

Theoretical predictions of fully elastic relaxation in SiGe grown on patterned silicon substrates have been investigated and confirmed by TEM dark-field cross-sections and photoluminescence spectra, paving the way to the integration of dislocation-free SiGe alloys on CMOS-compatible Si substrates fabricated with industry-standard techniques.

Acknowledgements

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Effects of Phosphorous Doping Density on Thin Ge Layers Grown on Si(001)

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1. Abstract

Reduction of threading dislocation density (TDD) in thin-film Ge grown on Si is considered critical for realising Si photonics integration. Employing n-type dopants such as Sb and As during Ge growth has demonstrated success in suppressing threading dislocation and smoothening film surfaces. [1, 2] Phosphorous, being another n-type dopant, its effect on Ge epilayer quality has not been reported. In this study, we optimise the effect of phosphorous doping density on defect density of 500 nm Ge layers with P concentration ranging from 1×10^{18} to 5×10^{19} cm^{-2} grown on Si by molecular beam epitaxy. To obtain a full spectrum of n-type doping, the optimum doping density for Sb is also determined from a series of Ge samples with doping density ranging from 1×10^{18} to 7×10^{18} cm^{-2}. Then, a novel co-doping technique is developed by introducing P and Sb simultaneously to the low-temperature Ge seed layer, which reduces the TDD to mid-10^{7} cm^{-2} for a 500-nm-thick Ge film. This thin Ge layer with low TDD provides a high-quality platform for high-performance Si-based semiconductor devices.

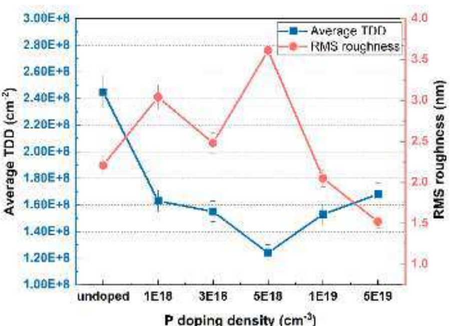


Fig.1. Summarising plot of TDD and root-mean-square (rms) roughness of samples with phosphorus doping density of 0, 1E18, 3E18, 5E18, 1E19 and 5E19 cm^{-3}, indicating an optimum P concentration of 5E18 cm^{-2}.

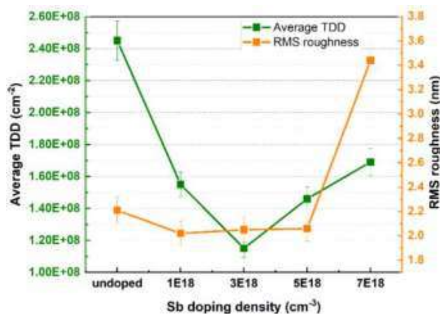
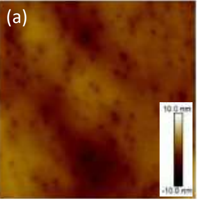


Fig.2. Summarising plot of TDD and rms roughness of samples with antimony doping density of 0, 1E18, 3E18, 5E18 and 7E18 cm^{-3}, indicating an optimum Sb concentration of 3E18 cm^{-2}.



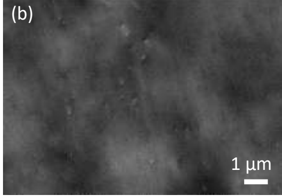


Fig.3. Characterisation of the 500-nm sample doped with 1E18 cm^{-3} P and 3E18 cm^{-3} Sb. (a) 5µm × 5µm AFM scan showing the surface topography of the co-doped sample with RMS roughness of 1.51 nm. (b) ECCI scan of the co-doped sample with a TDD of 7.8×107 cm^{-2}.

Acknowledgements

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Uniform CVD of graphene on 2” SiC wafer.

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1. Introduction

Propane/hydrogen CVD growth of graphene on SiC, studied since 2010 [1], consists simply to grow graphene from propane in a hydrogen/argon atmosphere. The presence of hydrogen in the gas phase promotes Si excess on the surface, hence making impossible graphene growth without propane flow [2]. This makes propane/hydrogen CVD very different from silicon sublimation where graphene grows from a carbon excess on SiC. The presence of hydrogen during growth, beyond strongly changing the chemistry during growth, allows to tune graphene properties from p-type multilayer to n-type monolayer. The quality of graphene monolayers prepared by hydrogen CVD is appealing for electronics applications, such as electrical metrology [3]. Graphene is also seen as a surface of choice for van der Waals epitaxy of nitrides [4] or 2D materials. For both applications, the growth of uniform high quality graphene films remains a crucial issue. This contribution focusses on the growth of graphene on 2" SiC wafers using propane/hydrogen CVD.

2. Experiments

Graphene films were prepared on the Si-face of 2" SiC wafers in a horizontal hot-wall CVD reactor with a rotating substrate holder under the same growth conditions: a 9% H_2 / 91% Ar growth atmosphere under 800 mbar, plus 0.1% C_3H_8 during a 15’ plateau at 1550°C for graphene growth. All graphene films are characterized using atomic force microscopy (AFM), and some are additionally studied using Raman spectroscopy and X-ray photoemission (XPS). Overall, the properties and the quality of the graphene films depend on the SiC polytype and on the wafer residual offcut. Representative XPS spectra from four samples grown on 6H-SiC are shown in Fig. 1.

The two spectra from graphene grown on two wafers from the same series appear almost superimposed (gray curves), while graphene grown on other series presents only small differences (black curves). Best graphene films are obtained on 6H-SiC wafers with a residual offcut of the order of 0.1 to 0.2°. For these optimized graphene films, morphology appears very uniform at the wafer scale, as shown by two representative images in the center and 200 mm away (Fig. 2).

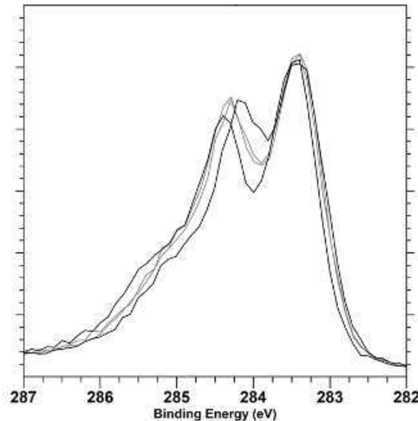
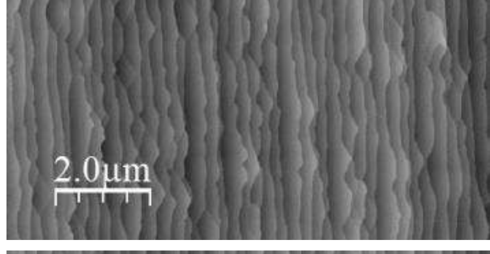


Fig. 1. C1s XPS spectra on four different 2” 6H-SiC wafer covered by graphene.



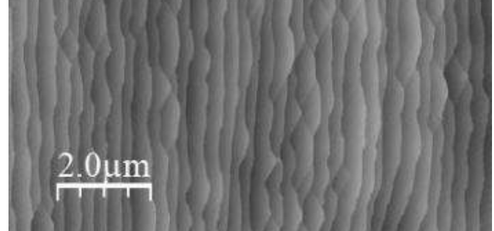


Fig. 2 AFM images of graphene film in the center of a 2” 6H-SiC wafer and 20 mm away.

3. Conclusions

Best graphene films are obtained on 6H-SiC wafers with a residual offcut of the order of 0.1 to 0.2°, which exhibit very uniform morphology even at the wafer scale. Our contribution will present these results with further characterizations (XPS and Raman mapping) and will discuss the key parameters to obtain uniform films at the wafer scale.

Acknowledgements

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InGaN Growth by PAMBE in the Intermediate Composition Regime on Silicon

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1. Introduction

InGaN is a semiconductor with an energy gap that ranges from from 0.7 eV (InN) to 3.4 eV (GaN) depending on its alloy composition [1]. The possibility to cover all the visible spectrum makes InGaN a very interesting material for photovoltaic [2] and optoelectronic applications, such as light emitters and detectors [3]. Moreover, due to its exceptional chemical stability, InGaN can be used for photoelectrochemical applications and biosensing [4], [5]. InGaN layers can be grown directly on Si substrates allowing for the direct integration of III–N technology with the existing Si technology, as well as advanced device designs [2], [5]. Despite the high interest in this material, the growth of InGaN in the entire composition range is still extremely challenging. These difficulties arise from the different thermal stability of In-N and Ga-N bonds as well as the large lattice mismatch of InN and GaN that can cause material segregation and fluctuations of the In content in the epilayer [6].

In this work we present an investigation of the growth of InGaN/Si(111) layers via plasma-assisted molecular beam epitaxy (PAMBE). Our analysis is focused on the effects of the growth conditions, in particular substrate temperature T_{sub} and N flux on the In incorporation into the epitaxial InGaN layer, as well as its morphology.

2. Material and Methods

All the samples in this study were obtained on single side polished undoped Si(111) wafers by PA-MBE equipped with a radio frequency (RF) plasma source. The native Si oxide was desorbed in situ by heating the substrates at 850°C for 10 minutes. Prior to the InGaN growth, the clean Si substrates were nitridized by exposing them to an active nitrogen flux to form an amorphous SiN layer which is known to improve the quality of the epitaxial InGaN layers [7]. InGaN growth was performed at a substrate temperature of 450°C (sample A and D), 500°C (sample B and E) and 550°C (sample C and F). The Ga and In fluxes were kept constant at 3.6×10^{14} and 2.8×10^{14} atoms/cm^2 s respectively. The molecular N_2 flux was varied from 1 sccm (sample A, B and C) to 2 sccm (sample D, E and F) with a constant RF power of 200 W. The growth time of all InGaN layers was 90 minutes. The different samples growth conditions are summarized in Table 1. The cleaning and growth processes were monitored in situ by Reflective high energy electron diffraction (RHEED). After the growth, all samples were analyzed *ex situ* by atomic force microscopy (AFM), scanning electron microscopy (SEM) and X-Ray diffraction (XRD).

Table I. Growth conditions and average In content of the samples in this study.

Sample	T_{sub} [°C]	N_2 flux [sccm]	In content [%]
A	450°C	1	43
B	500°C	1	40
C	550°C	1	23
D	450°C	2	48
E	500°C	2	45
F	550°C	2	24

3. Results

Sample A was grown with a T_{sub} = 450°C, well below the InN decomposition temperature, in a slightly N-rich condition. Sample A exhibited an epitaxial layer composed by dense and partially coalesced nanocolumns perpendicular to the surface (Fig. 1A). The average In content of the epilayer measured by XRD was 43%. Increasing T_{sub} caused a further coalescence of the nanocolumns into a network of nanowalls at 500°C (sample B, Fig. 1B) and into a rough compact layer at 550°C (sample C, Fig. 1C). The coalescence of the InGaN layer was accompanied by the appearance of large pits and In metal droplet on the surface and the subsequent reduction of In content to 40% and 23% in sample B and sample C respectively. The presence of droplets on the surface of both sample B and C suggests that the T_{sub} used were both above the InN decomposition temperature.

In order to avoid the formation of metal droplet on

the surface, the N flux was increased to reach a largely N-rich condition. Sample D was grown in a complete condensation regime and exhibited a dense array of uniform-sized flat-top columns perpendicular to the surface (Fig. 1D and Fig. 2). The average In content of the epilayer measured by XRD was 43%. Increasing T_{sub} above the InN decomposition temperature caused a random coalescence of the nanocolumns into larger hexagonal pillars characterized by an average In content of 45% (sample E, Fig. 1E).

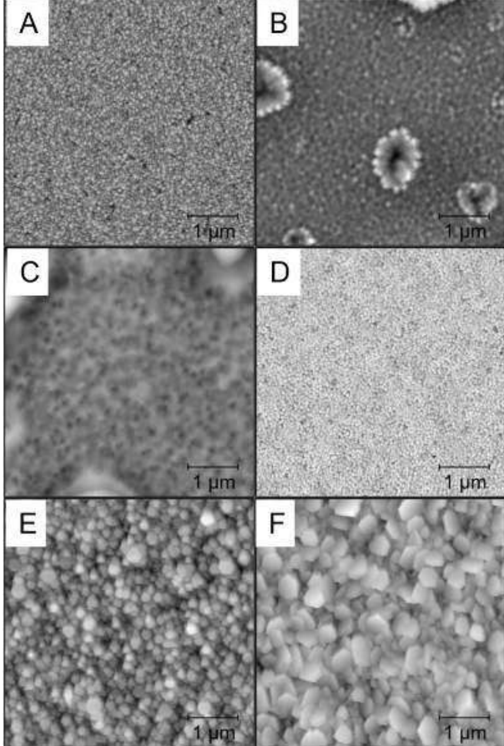

Fig. 1. 5 µm × 5 µm AFM micrographs obtained on sample A (A), B (B), C (C), D (D), E (E) and F (F).

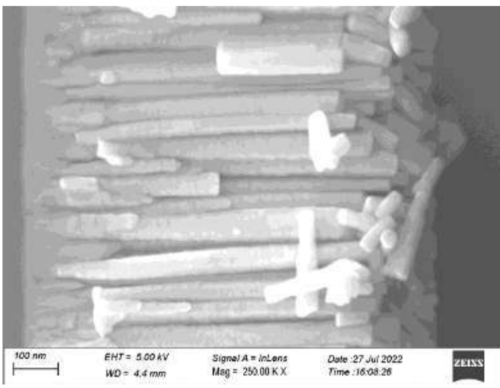

Fig. 2. SEM image measured on the cross section of sample D.

A further increment of T_{sub} to 550°C (sample F, Fig. 1F) resulted in the formation of a layer composed by network of flakes randomly oriented on the surface. XRD analysis of sample F revealed an average In content of 24% and the complete loss of epitaxial relation between the InGaN layer and the Si(111) plane.

3. Conclusions

In this work we observed that increasing the substrate temperature during the InGaN growth to values that exceed the InN decomposition temperature drastically damage the resulting epitaxial layer. An increment of 100°C in the T_{sub} from the complete condensation regime reduces the In incorporation by 50%. For low N fluxes the InN decomposition causes the unwanted formation of metal droplet on the InGaN surfaces and promotes the growth of a rough compact layer. Increasing the N flux can prevent the formation of surface droplets but enhances the uncontrolled 3D growth of the InGaN epilayer and reduces the epitaxial relation with the substrate. We also identified the ideal conditions to obtain high quality InGaN columnar layers directly on Si(111) substrates. The high uniformity and average In content of such layers make them ideal candidates for photoelectrochemical and optoelectronic applications.

Acknowledgements

The authors acknowledge support by BONES project in collaboration with Istituto Nazionale di Fisica Nucleare (INFN).

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Ge/Si Vertical Separate Absorption Charge Multiplication (VSACM) Avalanche Photo Diodes (APDs): Epitaxial Growth and Impact of Post-Epi Anneal on Excess Carrier Lifetime

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1. Introduction

Owing to its compatibility with mainstream Si technologies and remarkable physical properties, Ge has become a key enabler of modern semiconductor devices. The element has been introduced in various application areas including integrated photonics such as near-to-mid-infrared photodetectors and modulators [1-3]. In comparison to the Ge/Si Lateral Separate Absorption Charge Multiplication (LSACM) Avalanche Photo Diodes (APDs), the vertical device concept aims for a better control of the electric field in the multiplication and absorption regions. For the Vertical Separate Absorption Charge Multiplication (VSACM) APD device, light absorption is achieved in Ge, the charge region shields the absorption region from high reverse bias electric field, and multiplication is achieved in Si (Fig. 1).

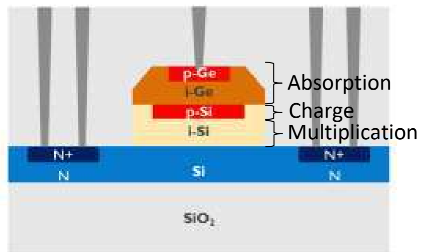

Fig. 1. Vertical Separate Absorption Charge Multiplication (VSACM) Ge Avalanche Photo Diode (APD).

Thin films of Ge can be epitaxially grown on low-cost Si substrates, with an impact on material quality due to the large lattice and thermal expansion mismatches between the Si substrate and the active part of the device [4]. The epitaxial growth is followed by a post-epi thermal treatment, to reduce the threading dislocation density (TDD), and, eventually, chemical mechanical polishing (CMP) to level the Ge surface with the surrounding masking material [4]. A concern is the Si diffusion into the Ge layer during the thermal treatment for defect reduction. It might increase the electrical band gap of the photodetector and reduces the excess carrier lifetime [5,6].

The current contribution first discusses the epitaxial growth of Ge-cap/Si bilayers required for VSACM Ge APD devices. Next, the impact of the thermal budget during the post-epi anneal of Ge will be re-addressed. It will be discussed how the post-Ge epi annealing step affects material properties like the surface roughness, TDD, the Si diffusion into the Ge, and, as a result, the excess carrier lifetime.

2. Experimental

Standard low temperature GeH_4-based epitaxial Ge growth processes in an ASM-Epsilon® 2000 system (200 mm wafers) or in an ASM Intrepid® RP-CVD cluster tool (300 mm wafers) were used to deposit Ge/Si bilayers on blanket or device patterned Si wafers [4-6]. Before layer deposition, the Si(001) wafer surface received a conventional wet-chemical clean. The native oxide has been removed either by an HF treatment and an *in-situ* thermal treatment at 800-850°C (patterned wafers) or solely by an *in-situ* thermal treatment at a sufficiently high temperature (>1000°C) (unpatterned wafers). The epitaxial growth of Ge, with thicknesses ranging from 200 to 1000 nm, was eventually followed by an *in-situ* post epi anneal for 3 minutes to reduce the TDD in the Ge layers.

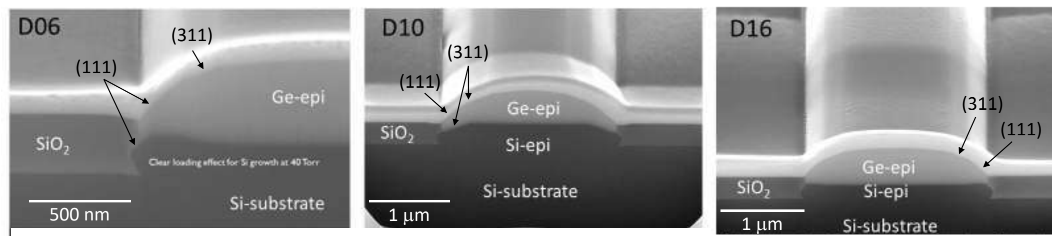

Fig. 2. Tilted SEM images of selectively grown Ge-cap/Si-epi//Si-substrate layers showing the impact of Si growth conditions on facet formation. D06: Si grown at medium pressure, D10: Si grown at low pressure, and D16: Si grown at optimized pressure. During Si-growth (111) facets might appear, depending on the steepness of the oxide side wall. Ge was always grown at lower temperature and atmospheric pressure.

Different post-epi annealing temperatures with a maximum of 850°C have been tested. This treatment is known to provide fully relaxed Ge layers, which contain a low amount of biaxial tensile strain due to the mismatch in coefficient of thermal expansion between Ge and the underlying Si substrate [5,6].

3. Results and Discussion

3.1. Selective Growth of Ge-cap/Si Bilayers

To obtain a high process throughput, Si selective epitaxial growth (SEG) was done at the highest possible growth temperature, just low enough to maintain flat (001) surfaces and to avoid surface rounding in the middle of the open windows. Near the window edges, Si facets might appear. The facet formation depends strongly on the growth pressure. At low growth pressures, (311) facets are formed (Fig. 2, D10). These (311) facets are more pronounced at a lower Si-growth pressure and for thicker layers. For higher growth pressures, facet-free Si-growth is possible but the process might suffer from chemical loading effects. Indeed, Si layers grown at 40 Torr are free of (311) facets but a slight layer thickening near the edge of the windows is observed (Fig. 2, D06). The appearance of (111) facets is linked with the shape of the sidewall of the oxide mask. Careful optimization of the process conditions, including the pre-epi wet chemical treatments, allows facet-free Si growth without layer thickening near the window edge (Fig. 2, D16). For the growth of the Ge-cap layer, facet formation cannot be suppressed without compromising material quality [4]. Figure 3 demonstrates the capability to deposit the APD Ge/Si stack in two separate steps, combined with a B-implant in between.

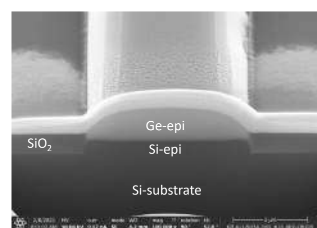

Fig. 3. Ge/Si-epi stack grown in two separate steps after applying a modified HF treatment and using optimized process conditions.

3.2. Impact of Post-Epi Anneal on TDD and Excess Carrier Lifetime

The excess carrier lifetime of epitaxial Ge, grown on bulk Si is affected both by the presence of misfit and threading dislocations and in-diffused Si (Fig. 4). With increasing Ge thickness, most of the carriers are no longer confined close to the unpassivated top Ge surface and the defective Ge/Si interface. This results in an increased carrier lifetime. Growing thicker Ge layers and polishing the stack down to the target value has a positive impact on material defectivity (Fig. 4a). However, the approach has only a limited or no effect on the carrier lifetime, with trendlines overlapping with those obtained with epi only (Fig. 4b). A reduction of the Si in-diffusion into the Ge layer by decreasing the post-epi annealing temperature has indeed a positive impact on lifetime (Fig. 4b) despite the higher remaining TDD (Fig. 4a).

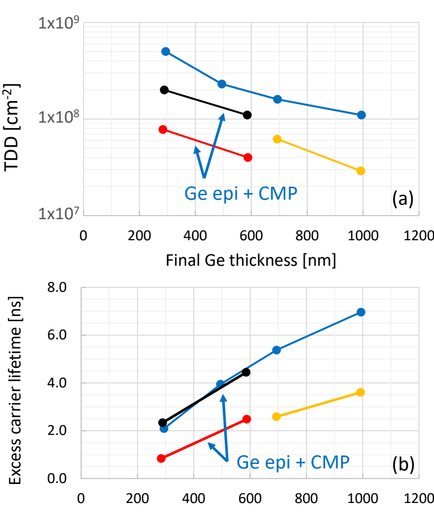

Fig. 4. a) TDD values obtained from electron channeling contrast imaging (ECCI) on Ge/Si stacks with different Ge thicknesses and annealed in different conditions (T2<T3), without and with CMP. The post epi anneals applied on the samples of the black and red data points were identical to those of the blue and yellow data points, respectively. b) Excess carrier lifetimes obtained from time resolved photoluminescence (TR-PL) from the same stacks.

4. Conclusions

The epitaxial growth of Ge-cap/Si bilayers, required for VSACM Ge APD devices has been demonstrated. The post-epi anneal reduces the dislocation density, but also leads to an unwanted Si diffusion from the Si substrate into the epitaxial Ge. Both phenomena have an opposite effect on the excess carrier lifetime.

Acknowledgements

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Influence of Ga concentration on the local atomic structure and material properties of Ga-doped $Si_{0.36}Ge_{0.64}$ epitaxial layers

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1. Introduction

Gallium is a potential dopant for source/drain (S/D) layers of pMOS devices. It enables interesting contact properties both in Ge and SiGe [1–4], making it an appealing alternative or complement to boron doping. However, the use of Ga in SiGe is not without challenges as its strong tendency to segregate at the layer surface due to its limited solid solubility in SiGe is difficult to control [5,6]. This can affect the structural properties of the material and degrade the final electrical and contact properties. In addition, the literature lacks a fundamental knowledge on the behavior of Ga impurities in $Si_{1-x}Ge_x$ lattice.

We showed previously that $Si_{1-x}Ge_x$:Ga epitaxial layers with box-like shaped Ga profiles could be produced efficiently by *in situ* doping using reduced growth temperature and higher-order Si and Ge precursors. [7] In the same reference, a first study of extended X-ray absorption fine structure (EXAFS) on uniformly doped SiGe:Ga was reported. The material showed interesting properties, with indications for a higher-than-expected Ge concentration in the average first-neighbor atomic shell around Ga atoms. However, the quality of the data did not allow to reach a definitive conclusion about this observation.

The current abstract extends this study to a larger set of Ga concentrations ($[Ga]_{chem}$), aiming for a better understanding of the preferential local atomic structure of Ga in the $Si_{1-x}Ge_x$ host matrix. EXAFS measurements at the Ge K-edge allow to compare the local structures and chemical environments around both Ge and Ga atoms.

2. Methodology

SiGe:Ga epilayers were grown using an ASM Intrepid® 300 mm-compatible reduced-pressure chemical vapor deposition (RP-CVD) reactor. The growth was performed at an extremely low temperature (320°C) using digermane, disilane and tri-tertbutylgallium (TTBGa) as Ge, Si and Ga precursors, respectively. X-ray diffraction (XRD) was used to study the structural properties of the epilayers. ω-2θ scans and reciprocal space maps (RSM) were acquired around the Si(004) and Si(113) Bragg reflections. The chemical composition was determined using secondary ion mass spectrometry (SIMS). The sheet resistance was measured using the micro-four-point probes (m4pp) method while the active doping concentration was characterized using micro-Hall effect (MHE) measurements. EXAFS analysis was carried out at the LISA beamline European Synchrotron Radiation Facility (ESRF) in Grenoble, France. Measurements in fluorescence mode, at a grazing incidence, allowed to maximize the absorbing volume within the epilayers. All the spectra were acquired at the Ga K-edge (10368 eV) for all the samples, and also, for one selected sample, at the Ge K-edge (11104 eV).

3. Results

This study examines how the Ga concentration affects the $Si_{1-x}Ge_x$ growth characteristics and the epitaxial material properties. The process conditions were optimized to obtain uniform Ga concentrations throughout the layer (Figure 1). The different $Si_{1-x}Ge_x$ layers have a similar Ge concentration of 64 ± 1% and $[Ga]_{chem}$ ranging from 6×10^{19} cm^{-3} (sample F5) to 1.7×10^{20} cm^{-3} (sample F40), where the number in the sample label corresponds to the flow of TTBGa used (a.u.).

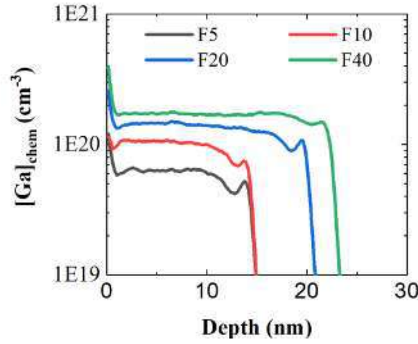

Figure 1. Ga concentration profiles as measured by SIMS, for samples grown with different TTBGa flows

Increasing the TTBGa partial pressure during growth induces strain relaxation in the epilayer, as confirmed by XRD-RSM. This might be caused by an increased amount of segregated Ga atoms acting as surfactants

during the growth. The segregation is not visible in Figure 1 due to the samples being cleaned with HCl to suppress superficial Ga in excess before SIMS analysis. On the other hand, the hole concentration increases with increasing $[Ga]_{chem}$, confirming that the process conditions are effective in incorporating electrically active dopants.

Figure 2 shows the best fits of the Fourier transform of the k^2-weighted EXAFS acquired at the Ga and Ge K-edges of sample F20 up 4 Å before phase correction. In SiGe, the first peak is well defined while the higher distance peaks are significantly smeared out due to the high static disorder of SiGe. This is indicated by a higher Debye-Waller factor (σ^2) which is a measure of the mean-square displacement of atoms in the lattice. Fitting parameters extracted for the first peak are provided in Table I.

The first peak is composed of two contributions of Ge and Si atoms. At the initial stage of the fitting procedure, the total number of atoms in the first coordination shell (main peak) was constrained to four, as expected in a diamond cubic crystal structure. In more refined fittings, the constraint was removed to accurately determine the error bars on the extracted parameters.

The average Ge coordination number around Ga dopants is higher than the concentration determined via SIMS, with the first coordination shell of Ga having Ge concentrations of ~ 75%, *i.e.*, 10% higher than the alloy's stoichiometry. Conversely, [Ge]% in the first shell of Ge for sample F20 amounts to 65%, which is in line with the composition of the host alloy. This indicates that Ge atoms are preferentially incorporated as Ga nearest-neighbors during the epitaxy process. No clear trend emerged when varying the [Ga]chem, despite sample F5 having a remarkably high [Ge]% in the first coordination shell.

3. Conclusions

The study examined the effects of varying the Ga concentration in $Si_{0.36}Ge_{0.64}$:Ga thin films on the properties and local atomic environment of Ga and Ge atoms. The EXAFS data confirmed a higher Ge/Si ratio in the first coordination shell of Ga compared to the SiGe alloy composition, suggesting that Ge atoms are preferentially incorporated as nearest-neighbors of Ga during the epitaxy process. Furthermore, the Ge fraction in excess was quantified to be ~10%. Additionally, electrical characterization confirmed that the process conditions were effective in incorporating electrically active dopants, while structural analysis revealed an increase in strain-relaxation with the TBBGa flow used.

Acknowledgements

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Table I Summary of EXAFS fitting results for the 1st coordination shell of $Si_{0.36}Ge_{0.64}$:Ga samples.

Sample (abs. atom)	Atom-shell.	R (Å)	N	σ^2
F5	Si-1st	2.37±0.04	0.7 ± 0.3	0.003
(Ga)	Ge-1st	2.42±0.01	3.3 ± 0.3	0.003
F10	Si-1st	2.37±0.02	1.0 ± 0.2	0.003
(Ga)	Ge-1st	2.40±0.01	3.1 ± 0.5	0.003
F20	Si-1st	2.36±0.03	1.0 ± 0.3	0.003
(Ga)	Ge-1st	2.40±0.01	2.9 ± 0.5	0.003
F20	Si-1st	2.40±0.01	1.7 ± 0.2	0.005
(Ge)	Ge-1st	2.43±0.01	3.2 ± 0.4	0.005
F40	Si-1st	2.37±0.02	1.2 ± 0.2	0.005
(Ga)	Ge-1st	2.40±0.01	3.7 ± 0.3	0.004

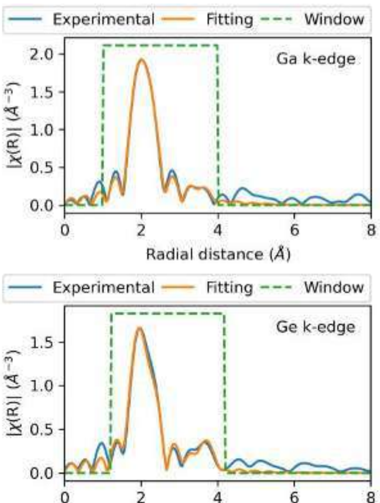

Figure 2: Fourier transforms of the k2-weighted EXAFS signals acquired at the Ga (top) and Ge (bottom) K-edges of a SiGe:Ga (sample F20).

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Modeling of optical absorption in SiGe QCSE modulators including excitonic effects

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1. Introduction

Electroabsorption modulators (EAM), which are based on the quantum-confined Stark effect (QCSE), are promising devices for numerous electrooptic applications, including emerging photonic integrated circuit (PIC) applications for fiber-optic communications. A SiGe quantum well design, which was first demonstrated in Ref. [1], has the advantage of being compatible with CMOS technology. The growth and characterization of such devices are challenging. Therefore, modeling of these structures is required to optimize device parameters and benchmark their extracted characteristics.

In this work, we present improvements of the nextnano software which we have developed for modeling QCSE structures within the EU project SiPho-G. nextnano is a TCAD tool for the simulation of electronic and optoelectronic semiconductor nanodevices with various geometries, materials, biases, etc. We address the following challenges when simulating the SiGe QCSE: Modeling of single particle electron and hole states near the Γ point; calculation of imaginary and real parts of the complex refractive index from computed states; adding the excitonic corrections to the optical properties.

2. Details of the modeling

2.1. 8-band k·p simulations

Most of the multiple quantum well QCSE designs [2, 3] use wide barriers where the overlap of electron wavefunctions from neighboring wells is insignificant, therefore this work focuses on modeling single quantum well structures. When thinner barriers are used, the interaction between the wells can be taken into account by expanding the simulation region to two or more quantum wells. Furthermore, doped buffer regions can be placed on both sides of the quantum well structures to compute realistic electrostatic potential profiles and currents in the system.

The 8-band k·p Hamiltonian is used to calculate single-particle states in the valence and conduction bands. This approach includes the degenerate perturbation theory around the Γ point between conduction and valence bands through Kane parameters [4], which is a significant improvement compared to single-band and 6-band k·p models, especially in the case of small bandgap materials. The strain correction is included in our 8-band Hamiltonian. The Poisson equation is solved self-consistently together with the Schrödinger equation.

2.2. Refractive index calculations

This calculation aims to study the optical properties of the device composed of a stack of modeled quantum wells. The physical properties of interest are the absorption coefficient and the complex refractive index. The dependence of both quantities on the photon energy can be calculated from the complex permittivity,

$$\varepsilon(\omega) = \varepsilon_1(\omega) + i\varepsilon_2(\omega). \quad (1)$$

The imaginary part of the permittivity, ε_2, can be calculated directly from the computed wavefunctions and eigenenergies [5],

$$\varepsilon_2 = \frac{2\pi e^2}{V m_0^2 \omega^2 A^2} \sum_k \left|\vec{A}\cdot\vec{P}_{ba}\right|^2 \delta(E_{ba} - \hbar\omega)(f_a - f_b), \quad (2)$$

where a and b are eigenstate indexes involved in transitions, e – electron charge, m_0 – electron mass, ω - photon frequency, A – polarization, E_{ba} – difference between eigenstate energies, f – Fermi factor, P – momentum matrix element computed using Hellmann–Feynman theorem.

The real part of the permittivity, ε_1, can be calculated using the Kramers–Kronig relation between the real and imaginary parts of the analytic complex function,

$$\varepsilon_1(\omega) = 1 + \frac{1}{\pi} P \int_{-\infty}^{+\infty} d\omega' \frac{\varepsilon_2(\omega\prime)}{\omega' - \omega}. \quad (3)$$

The Kramers–Kronig relation is nonlocal, therefore the result of the integration in Eq. (3) is governed by ε_1 at all photon energies. The 8-band k·p model only gives the information about ε_2 of order 10^{-2} eV around the absorption edge. Thus, a way to estimate the impact from optical transitions at higher photon energies is needed. The authors of [2, 3] used the constant real refractive index approximation to avoid using Kramers–Kronig equation [2], while nextnano is able to reproduce local variation of the real refractive index.

2.3. Excitonic correction

The QCSE absorption modulators operate at photon energies close to the absorption edge. In this region, the impact of the excitonic correction on optical properties is significant. An exciton is a quantum state formed by an electron and a hole interacting via the Coulomb potential. These states are found for each electron and hole pair at the Γ point using a variational approach, cf. Ref. [2]. The method was adapted to be compatible with the 8-band k·p Hamiltonian, by converting 8-band parameters to corresponding single-band ones and accounting for a strong mixing between hole states and a weaker mixing between hole and electron states.

The exciton correction to absorption consists of two contributions. (1) The electron and hole at the Γ point form a bound exciton state, which results in a distinct peak in ε_2 few meV below the absorption edge. (2) To account for the formation of excitons at nonzero electron and hole wavevector, the rest of ε_2 is modified by the Coulomb enhancement factor [6].

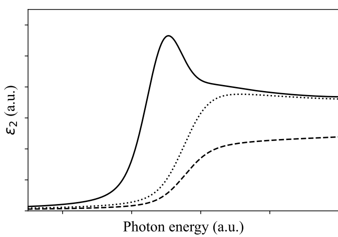

Fig. 1. Excitonic correction to optical properties. The single-particle ε_2, computed from Eq. (2) (dashed line) is modified by the Coulomb enhancement factor (dotted line). Then, the exciton peak from the bound state is added (solid line).

3. Results

Our simulation framework has been tested on a 9 nm Ge well with a 12 nm $Si_{0.4}Ge_{0.6}$ barrier grown on $Si_{0.3}Ge_{0.7}$. Such a structure has been studied in Ref. [1]. The resulting band edges and wavefunctions at the Γ point are shown in Fig. 1. We have used the analytic profile of the Ge content in the structure as suggested in Ref. [2], to take into account interdiffusion between the barrier and the well.

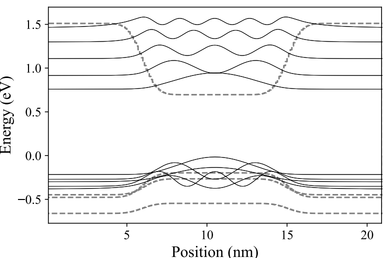

Fig. 2. Conduction and valence band edges (dashed lines) with electron and hole eigenstates (solid lines).

According to Ref. [2], a characteristic diffusion length of 1 nm provides the closest result to the experiment, therefore this value is used in this work. The k·p parameters were taken from Ref. [2].

The effective optical absorption of the quantum well for two different biases is shown in Fig. 3. The absorption spectrum has a red shift at nonzero bias, allowing for absorption modulation at photon energies in the range of 0.95–0.96 eV. With a further increase of bias, the absorption shifts to lower energies, while the intensity of the exciton peak decreases.

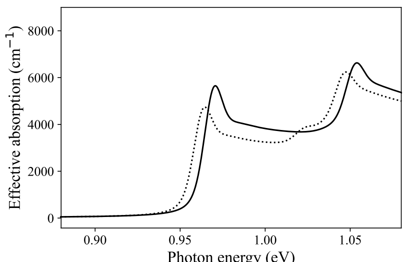

Fig. 3. The effective absorption inside the quantum well at zero electric field (solid line) and 90 kV/cm field inside the well (dotted line).

4. Conclusions

We have reviewed the application of the nextnano software for simulations of QCSE devices. The optical properties are calculated within the 8-band k·p model, which considers the nonparabolicity of the conduction band and the mixing between electron and hole states. Besides, the exciton correction to absorption was taken into account to improve the optical properties calculation at photon energies close to the absorption edge. In the next steps, we will adapt this approach to full Brillouin zone models such as the 30-band k·p Hamiltonian. This will allow us to compute transitions at higher photon energies, improving the accuracy of the model for the real part of the refractive index.

Acknowledgements

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Electrical Characterization of Sputtered Monocrystalline GeSn Thin Films for Photodetection Applications

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1. Introduction

With global resources of Indium rapidly depleting, GeSn is a promising, more abundant alternative to InGaAs for short-wave infrared (SWIR) photodetectors [1]. The introduction of a low percentage (<10%) of Sn produces an indirect-to-direct band gap transition in Ge, with the resulting GeSn direct band gap shifted deeper into the SWIR region [2,3]. The band gap can be tuned via the fraction of Sn introduced, making GeSn an ideal material for SWIR photodetector applications such as telecommunications and Light Detection and Ranging (LiDAR) technologies [1].

Methods of GeSn fabrication include molecular beam epitaxy (MBE), chemical vapor deposition (CVD) and sputtering [2]. Several challenges arise in the growth of GeSn alloys, including the high (>4.2%) lattice mismatch between GeSn and Si substrates and the low solubility of Sn in Ge [2,3]. Here, we focus on sputtering as a GeSn growth method because it is cost effective and scalable for industry applications [1].

We present an investigation of the electrical properties of monocrystalline GeSn thin films grown by sputtering in order to evaluate the suitability of sputtered films for SWIR photodetection applications. Using Hall measurements in the Van der Pauw geometry [4], we aim to evaluate the electrical properties of our sputtered samples.

2. Methods

Si(001) substrates are cleaned with a 1% HF solution for 90 seconds. The substrates are loaded in a magnetron sputtering machine in confocal configuration. GeSn films are grown at 300°C in Ar+4%H_2 gas, controlling their composition by fixing independently the plasma powers applied to the Ge and Sn targets. A STEM HAADF image of a representative monocrystalline GeSn thin film grown using this method is shown in Fig. 1. We use Hall measurements in Van der Pauw geometry to evaluate the unintentional doping concentration and Hall mobility of our GeSn films.

The clean room facilities at EPFL are used to prepare sputtered GeSn samples for measurements in the Van der Pauw geometry. Laser lithography, deposition of Al/Ti layers by electron beam evaporator and lift-off are used to create four electrical contacts in the sample corners.

Van der Pauw measurements are taken between 150K and 300K, in steps of 25K. At each step, a magnetic field sweep between -5T and +5T is performed. Two channels are used to check the sample is symmetric.

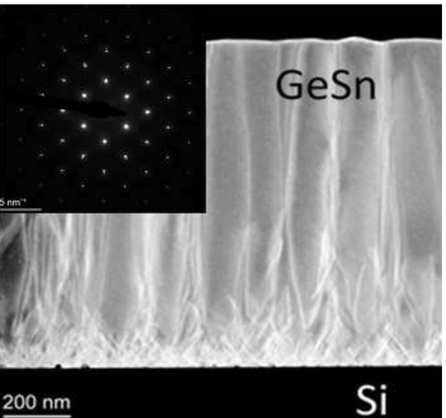
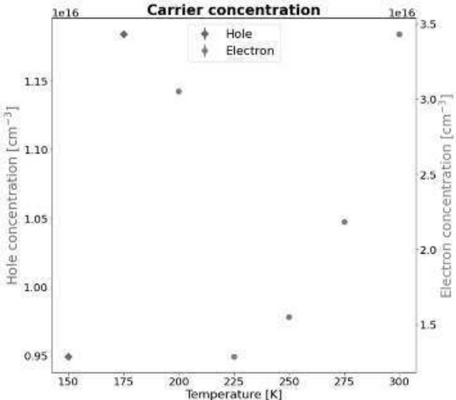


Figure 1: STEM HAADF image of a representative GeSn thin film deposited on an Si substrate by sputtering. The TEM diffractogram shown in the inset was taken so that the selected area includes both the GeSn film and the Si substrate.

3. Results

Our preliminary results were obtained for a 400nm film of GeSn with 4.5% Sn composition, grown by sputtering on an Si substrate. From Fig. 2, we see that the majority carrier changes from p-type to n-type at a temperature of about 200K. N-type unintentional doping is unexpected for GeSn, so we believe that this result is due to metallic contamination from the sputtering machine. We are in the process of replacing this machine with a new, uncontaminated one. When this new machine is ready, we aim to repeat our measurements and verify our findings at temperatures above 200K.

The 150K data point in Fig. 2 may indicate that, without unexpected n-type doping, unintentional p-type carrier concentration in our sputtered GeSn



may be as low as 10^{16} cm^{-3}. If verified using samples

Figure 2: Carrier concentration as a function of temperature for a sputtered GeSn on Si sample. The majority carrier transisitons from p-type to n-type at 200K.

from the uncontaminated machine, this result could be very promising, as low levels of unintentional doping are desired for high performance NIR photodetectors.

The Hall mobility values are shown in Fig. 3. The hole mobility measured at 150K is below 60 cm^2/Vs, a very low value. We again expect this is due to contamination of the film during growth.

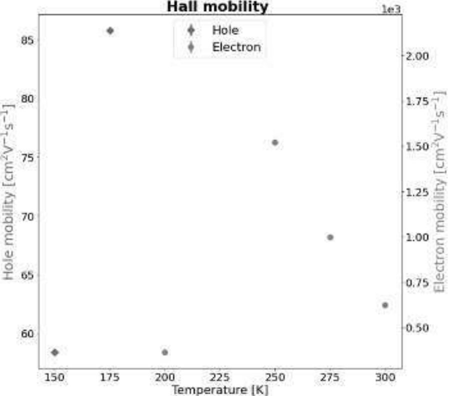


Figure 3: Hall mobility as a function of temperature for sputtered GeSn on Si sample.

4. Conclusions

Ahead of the ICSI/ISTDM, we aim to carry out the same Hall measurements using samples grown in the new sputtering machine, in the hope of verifying the low unintentional doping concentration in sputtered GeSn films on both Si and Ge substrates. We will present the results of this study at the conference.

Acknowledgements

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Plasmonic TiN nanohole arrays for on-chip refractive index sensors

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1. Introduction

Refractive index (RI) sensing based on plasmonic excitations has attracted interest in the field of bio-sensing. Integrated biosensors have the potential to be used in applications ranging from agricultural monitoring to point-of-care healthcare solutions. State of the art plasmonic biosensors typically require external instruments such as microscopes and spectrometers for readout which limits the possibility of miniaturization. Fully integrated on-chip biosensors based on plasmonic structures, in which the sensor output is available as an electrical signal, require the use of complementary metal-oxide-semiconductor (CMOS) material for fabrication on the cost-effective Silicon platform. However, CMOS fabrication processes place restrictions in particular on the metals that can be used, which precludes the utilization of commonly used noble metals such as Au. The optical properties of plasmonic nanohole arrays (NHAs) are highly sensitive to changes in the RI in the vicinity of the structures and the combination of an Al NHA with a Ge photodiode has previously been shown to enable the development of integrated RI sensors [1]. Here, we focus on the CMOS compatible transition metal nitride Titanium Nitride (TiN) as a plasmonic material that is also biocompatible.

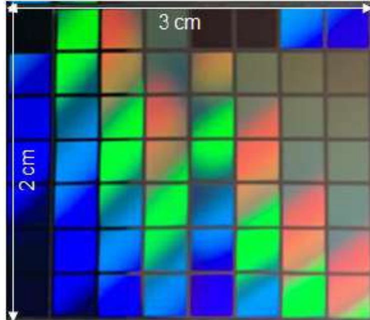

Fig. 1. *Fabricated chip with different TiN NHAs*

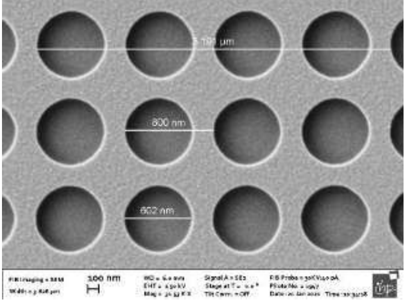

Fig. 2. *SEM image of TiN NHA*

2. Results and discussion

We present and discuss optical characterization results for TiN nanohole arrays fabricated using industrial fabrication processes [2] (Fig. 1 and Fig. 2) for possible applications in CMOS-compatible on-chip RI sensors with a large degree of miniaturization [3, 4]. Furthermore, we compare our experimental results with FDTD simulations based on the measured TiN permittivity. Both measured and simulated reflectance spectra show pronounced Fano-shaped resonances (Fig. 3) that shift as a result of changes in the dielectric environment.

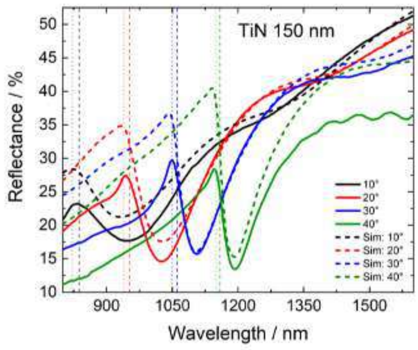

Fig. 3. *Measured and simulated reflectance spectra of TiN NHA under different angles of incidence and p-polarization*

The Fano resonances become more pronounced at increasing angle of incidence as well as increasing TiN layer thickness. This opens up the possibility to fine-tune TiN layers for good sensing performance even though optical losses in the material are large compared to e.g. Au and Ag. We discuss metrics that evaluate the expected performance for refractive index sensing and compare to selected measurement results.

3. Conclusions

TiN is a CMOS compatible and biocompatible transition metal nitride with large thermal stability, which could make it interesting for applications in on-chip sensing. Our optical characterization of the fabricated structures based on reflectance spectra shows the appearance of Fano resonances at specific wavelengths related to the array geometry as well as the superstrate RI. We find that our structures can give sufficient sensitivity for detection of solvents in water.

Acknowledgements

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Extended short-wave infrared GeSn photodetector realized by ion implantation and flash lamp annealing

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1. Introduction

Nowadays, most of photodetectors (PDs) for short wavelength infrared (SWIR) photodetection are based on III-V group materials which are not compatible with complementary metal oxide semiconductor (CMOS) for integrated Si-based optoelectrical platform application. Alternatively, full-IV-group GeSn alloy is considered as a promising choice for 2 μm to mid-infrared application [1] due to its highly tunable bandgap and benefit from the success of the integration of Ge alloys with Si-based technology [2].

Incorporating Sn into Ge is limited by low equilibrium solid solubility of Sn in Ge, which is typically lower than 1% [3] and a large lattice mismatch of around 14.7% between Ge and Sn [4]. Until now, most of the GeSn fabrication highly relies on expensive growth methods like chemical vapor deposition (CVD) [5][6][7] or molecular beam epitaxy (MBE) [8][9][10]. Alternatively, ion implantation is a fully CMOS-compatible technology, which advantages of low-temperature ex-situ doping and local doping through photolithographically patterned masks.

In this work, we demonstrate a room-temperature p-n photodetector fabricated with a CMOS-compatible process based on ion implantation and flash-lamp annealing. The photodetectors exhibit an extended responsivity up to 2 μm. This result provides a new approach for realizing CMOS-compatible optoelectrical integration near 2 μm.

2. Fabrication and characterization of GeSn photodetectors

We implant Sn and P into p-type Ge wafer to achieve non-equilibrium alloying of 3% Sn and pn junction of photodetectors. Then, we use flash lamp annealing (FLA) for 3 ms to recovery crystal damage and active P doping in pn junction region. UV photolithography and metal deposition are used to fabricate metal contacts for the GeSn vertical pn photodetector. After metal depositions, samples were annealed by FLA for 3 ms with the lower energy density, which is sufficient to activate electrical contacts but not leads to Sn segregation.

We investigated the photodetector responsivity by illuminating the device with a calibrated halogen lamp dispersed by a monochromator. The photocurrent of GeSn PD was obtained through a Lock-in amplifier coupled to a low-noise current amplifier.

3. Result and discussion

The spectral responsivity of 3% GeSn devices under -1V reverse bias is measured from 1200 nm to 2000 nm and compared with a commercial Ge PD FDG03-CAL from Thorlabs Inc..

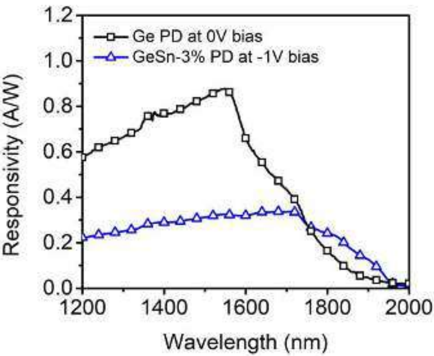

Fig. 1 Responsivity comparison between commercial Ge and our GeSn PDs.

As the responsivity shows in Fig.1, Sn incorporation into the Ge lattice shrinks the bandgap and leads to an extended responsivity to a longer

wavelength than Ge PDs. The 3% GeSn shows an extended responsivity peaking at 1680 nm. The peak responsivity of our GeSn PDs under -1V reverse bias is found to reach 0.34 A/W which is comparable with Ge PDs, indicating a high-quality GeSn material after implantation and FLA. The responsivity of the 3% GeSn PD extends up to 1950 nm with a maximum external quantum efficiency (EQE) of 25% @-1V.

4. Conclusions

We have demonstrated a room-temperature GeSn p-n photodetector fabricated by CMOS-compatible ion implantation and flash-lamp annealing process. The peak responsivity under -1V reverse bias has been demonstrated to be 0.34 A/W@1680 nm with 3% Sn concentration. Our work provides a clear pathway for realizing CMOS-compatible GeSn photodetectors with the potential for 2 µm Si-based integration application.

Acknowledgments

Support from the Ion Beam Center (IBC) and the clean room facility at Helmholtz-Zentrum Dresden-Rossendorf (HZDR) is gratefully acknowledged. This work was partially supported by the National Science Center, Poland, under the Grant No. 2016/23/B/ST7/03451 and the Bundesministerium für Bildung und Forschung (BMBF) under the project "ForMikro": Group IV heterostructures for high performance nanoelectronic devices (SiGeSn NanoFETs) (Project-ID: 16ES1075).

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TiN nanotriangle arrays in a CMOS-compatible fabrication process for open plasmonic cavities

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1. Introduction

We present optical characterization results and theoretical analysis of titanium nitride nanotriangle arrays fabricated in a CMOS-compatible process. Here, the optical properties are determined by the interaction of the localized surface plasmon resonance modes of the individual triangles and the lattice resonances of the array itself. Non-trivial nanoparticle arrays- such as the ones investigated here can feature various optical phenomena. The honeycomb lattice, very similar to the one shown here, exhibits optical Dirac points and resonances with very narrow resonances, which can, among other properties, serve as open optical cavities with high quality factors to induce and enhance lasing [1].

We study such arrays by angle-dependent reflection spectroscopy, in order to obtain the lattice dispersion. Comparing this to full-wave simulations, as well as analytical computation of the high-symmetry directions, can provide an understanding of the interaction of light and matter in such lattices.

2. Results and Discussion

2.2. Optical Characterization

The nanostructures were created by plasma-enhanced chemical vapor deposition of 150 nm of SiO_2 on Si, followed by sputtering of 50 nm of TiN. The sample was then patterned via deep-ultraviolet (248 nm) photolithography and reactive ion etching. More details on the fabrication process and its ongoing integration into a commercial SiGe process flow are given elsewhere [2].

Compared to structuring them directly, fabrication of the nanotriangle arrays is far easier through fabrication of arrays of nanoholes with large diameter, which connect to each other. This leads to an array of nanotriangle islands (Fig. 1) on two interpenetrating hexagonal lattices, which belong to the same wallpaper group *p6m* as the infinite honeycomb lattice.

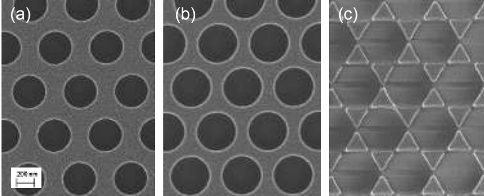

Fig. 1. The nanotriangle arrays are fabricated by etching a hexagonal nanohole array (a-b) with excessive hole diameter (c), making the holes touch and creating triangular islands.

2.2. Optical Characterization

When measuring the reflection spectra under vertical incidence, one can identify how the nanohole and nanotriangle arrays exhibit very distinct reflection spectra (Fig. 2). The position of maxima and minima is almost reversed. The effects of this transition are known from nanosphere lithography.[3]

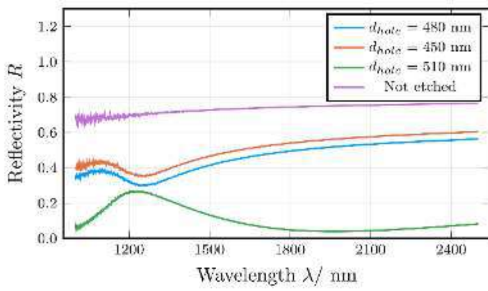

Fig. 2. Reflectivity (measured under vertical incidence) for hexagonal nanohole arrays etched with a hole pitch of 600 nm and various hole diameters. For 510 nanometer hole diameter, the structure transitioned to a nanotriangle array (Fig. 1c).

We also studied the lattice dispersion by reflection spectroscopy under grazing incidence. The impinging wave was TE polarized, and the azimuth was oriented towards the M and K points of the lattice, respectively. We recorded spectra for incidence angles between 5 and 50 degrees, in increments of 5 degrees. The results were then interpolated, in order to obtain a distribution

of reflection values over the photon energy $E_{phot} = hc/\lambda$ and in-plane momentum $k_{||} = 2\pi/\lambda \sin(\theta)$, where h is Planck's constant, c is the speed of light in vacuum, and θ is the angle of incidence. The results for incidence in the lattice direction of the K point are shown in Fig. 3, on the right side of the plot. In the heatmap, one can observe boundaries of relatively sharp transition in the reflectivity. These correspond to the conditions of momentum matching between incident light and vectors of the reciprocal lattice, and can be found analytically by solving

$$\frac{2\pi E_{ph}}{hc} = |\vec{k}| = \left|\begin{pmatrix} k_{||} \\ 0 \end{pmatrix} + \vec{G}_{i,j}\right|, \quad (1)$$

where $\vec{G}_{i,j}$ is any linear combination of the reciprocal lattice vectors. The solutions of (1), plotted as white lines, match the transitions in the reflection heatmap (Fig. 3).

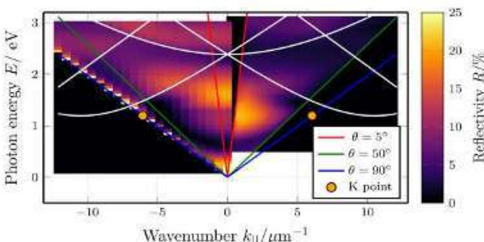

Fig. 3. Simulated (left) and measured (right) lattice dispersion of the nanotriangle lattice in air. The white lines show the points where the momentum matching condition is fulfilled.

2.3. Full-wave Simulation

While we are able to produce nanotriangle arrays with great accuracy, we are limited by the maximum practical angle of incidence of the instrument (50 degrees) and to the samples produced. In order to study more cases, we set up simulations using the rigorous coupled-wave analysis (RCWA)[4]. We model the array with a simple stack of 50 nm TiN, structured into the array, on top of 150 nm SiO_2 on a Si substrate. The simulations (left half of Fig. 3) match the momentum matching lines and agree qualitatively with measured reflectivities. With simulation, we could also obtain results for near-vertical incidence and extend the cone towards 90 degrees. The results obtained around 90 degrees may suffer of numerical instability.

The interesting sharp transitions in reflectivity occur for photon energies in excess of 1.5 eV, in the visible spectrum. However, plasmon resonance in TiN rather occurs within the near and short-wave infrared range, as the optical properties become metallic.[5] In addition, it is worth to note that working in near infrared would ensure compatibility with other silicon photonics technology. To tune the lattice to lower photon energies, one can either scale up its size, or modify the speed of light by immersing the sample in a refractive liquid (Fig. 4). Simulations predict sharp transitions in reflectivity around the lowest-energy momentum matching line, which could be harnessed in applications of these structures as open cavities.

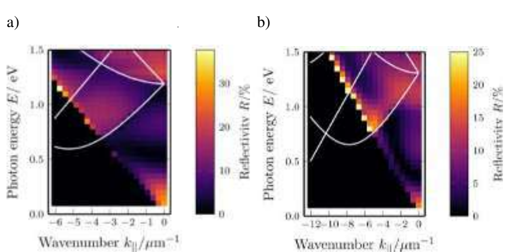

Fig. 4. Simulated reflection of a) the structure scaled by a factor of 2 b) the structure immersed in acetone (n=1.35).

3. Conclusions

We fabricated TiN nanotriangle arrays in a honeycomb-like lattice and studied their optical properties. The lattice dispersion matches numerical results. Simulations of larger lattices show how future experiments can be conducted with enhanced structures in the near and short-wave infrared region.

Acknowledgement

We thank the 4th Physical Institute of the University of Stuttgart for permission to use and guidance with their Fourier-transform infrared spectrometer.

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Spin pumping in GeSn alloys

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1. Introduction

The development of fast and energy efficient electronic devices is demanding to face the challenges of the future information and communication technology.[1] Spintronic devices are a promising strategy to overcome the "more than Moore" scenario, exploiting the spin degree of freedom of electrons to engineer new functionalities. The mutual interconversion between spin and charge currents represents a very hot topic in the field of condensed matter physics. In particular, when high spin-orbit coupling (SOC) materials (i.e. heavy metals (HM)) are coupled with ferromagnets (FMs), it is possible to manipulate the FM magnetization through the so-called spin Hall effect (SHE). Here, a charge current flowing inside the HM is converted into a pure spin current in the bulk of the material, and subsequently injected into the adjacent FM. The SHE is directly connected to the strength of the SOC present in a material, thus the higher is the SOC, the higher is the generated spin current.[2] Recently, studies on spin-to-charge conversion (SCC) have been conducted also in semiconductors belonging to the group IV, such as Si and Ge, with the aim to exploit both their CMOS compatibility and high spin diffusion length.[3]
In this contribution, we investigate the spin pumping (SP) mechanisms in novel group IV alloys. Specifically, we study GeSn/(Au/)Co/Au heterostructures by means of room temperature (RT) broadband ferromagnetic resonance (BFMR) and SP-FMR experiments, where the strength of the SOC in the SHE material is varied by controlling the Sn molar fraction in the binary alloy. The different Sn concentration allows the tuning of the band structure of the GeSn alloy from an indirect (low Sn concentration) to a direct (high Sn concentration) band gap configuration. This offers the possibility to explore the mutual influence between the SOC and the band structure in the GeSn alloy on the generated SCC efficiency.

2. Materials and Methods

GeSn samples with a thickness of about 400 nm were deposited on Ge virtual substrates (Ge-VS) on Si(100) wafers through reduced pressure chemical vapor deposition using an AIXTRON TRICENT reactor. Digermane (Ge_2H_6) and tin tetrachloride ($SnCl_4$) were used as precursors for elementary Ge and Sn, respectively.[4,5]
The Co(10 nm)/Au(5 nm) bilayers and Au(5)/Co(10 nm)/Au(5 nm) trilayers were deposited on top of the GeSn substrates via e-beam evaporation at RT.
The BFMR and SP-FMR experiments were conducted using a home-made setup, where the sample is positioned between the polar extensions of a Bruker ER-200 electromagnet, maintaining its surface parallel to the external magnetic field (H_{ext}) in the so-called "flip-chip" configuration for in-plane (IP) measurements. To induce an oscillating magnetic field in the FM layer, the sample is fixed to a coplanar waveguide connected to a broadband (1 - 40 GHz) RF-source. The FMR signal for a fixed RF frequency is performed by measuring the derivative of the absorption power downstream of the electrical transmission line as a function of H_{ext} through a lock-in amplifier.

3. Results and discussion

In Figure 1(a) the evolution of the Kittel curves acquired in the IP geometry is presented for the GeSn/Au/Co/Au studied samples, and the dataset is fitted according to Equation 1 (solid lines in Fig.1 (a)).

$$f_{res}=2\pi/\gamma \sqrt{[H_{res}(H_{res} + 4\pi M_{eff})]} \qquad (1)$$

where γ is the gyromagnetic ratio, and M_{eff} the effective magnetization. γ is maintained constant in the fit, being the Co layers simultaneously deposited on the different substrates. M_{eff} is related to the surface anisotropy of the Co film, which turns out to be the same for all the samples, with an average value of 1102 ± 5 emu/cm^3.

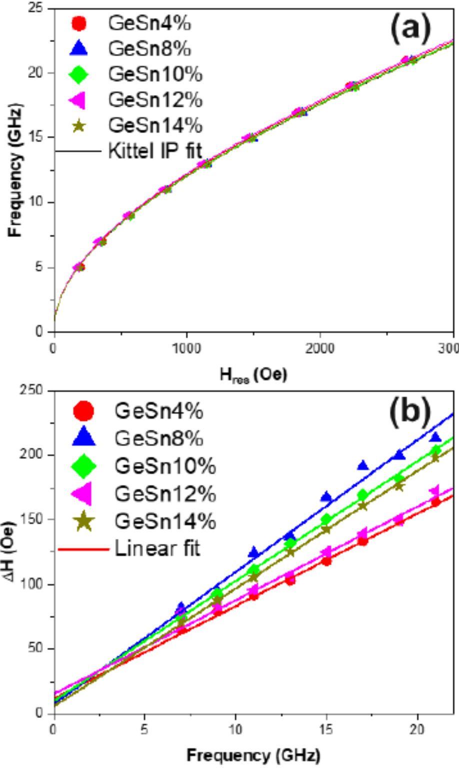

Fig. 1. Dataset extracted from the BFMR measurements conducted on each GeSn sample as a function of the Sn concentration. (a) Kittel curves acquired in the in-plane geometry (scattered symbols) fitted with equation 1 (solid lines). (b) $\Delta H(f_{res})$ curves fitted with equation 2.

Figure 1 shows the linewidth of the BFMR signal (ΔH) as a function of the resonant frequency (f_{res}) for each GeSn/Au/Co/Au sample with a different Sn concentration (scatter plots). The solid lines in Fig. 1 indicate the fit of the collected data with Equation 2.

$$\Delta H = \Delta H_0 + 4\pi/\gamma \ \alpha \ f_{res} \qquad (2)$$

where ΔH_0 represents the inhomogeneous broadening, and α the damping constant.
According to the spin pumping theory, α is directly proportional to the spin current density (J_S) generated in the system due to the SHE. Thus, the higher the slope of the $\Delta H(f_{res})$ curve, the larger is J_S. From Figure 1, the correlation between the slope and the Sn content in the GeSn alloy suggests a non-trivial interplay between the SOC present in the material and the positioning of the energy bands.

4. Conclusion

In this contribution the SCC mechanisms in GeSn alloys with different Sn concentration are investigated, and a non-trivial correlation between the Sn concentration and the generated spin current density in the systems is observed. Our results are the first steps in the investigation of the relationship between the SOC and the GeSn band structure changes through the variation of the Sn molar fraction, opening a path towards the optimization of GeSn-based spintronic systems as spin-charge interconverters.

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Investigation of the Schottky barrier height in germanium-aluminum heterostructure devices

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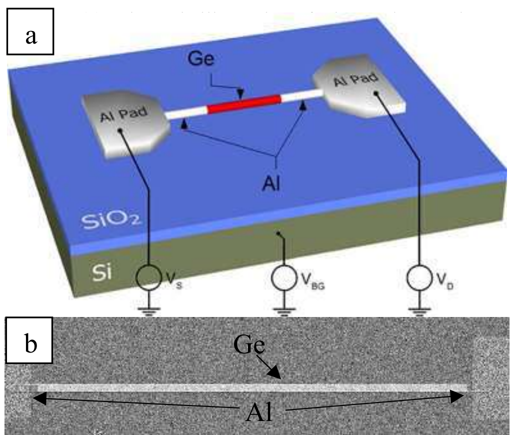
1. Introduction

Germanium can be used to fabricate low-dimensional devices that are promising for optoelectronic because of their compatibility with the CMOS technology. Currently, Ge-based devices are under investigation to better understand their transport and optical properties for the development of transistor, optoelectronic, and spintronic devices. In particular, Ge nanowires (NWs) are interesting because their growth can be precisely controlled, thereby customizing their shape, geometry, composition, and orientation. Ge heterostructures and metallic contacts can be combined and used as integrated contacts and interconnection solutions for nanometer-scale electronic. The identification of a



metal that can be used to form a good contact with Ge via a thermally induced exchange reaction is complex and still the subject of research. Aluminum is one of the best materials for this scope, and Al/Ge devices are very promising also for superconductor-semiconductor hybrid devices.

In this work, we analyzed the Schottky barrier height of Al/Ge nanosheets fabricated via a thermally induced Al-Ge exchange reaction. This mechanism allows one to obtain abrupt interfaces between Ge and Al [1,2]. After the lithography of Germanium-on-insulator (GeOI), 76 nm thick Ge stripes are obtained. Al contacts are fabricated with sputter deposition, and the formation of Al/Ge heterostructure is achieved via a thermal annealing process. The structure of these devices and the scanning electron microscopy images are shown in Figs. 1. Fig. 1b shows one device after processing. The darker segments emerging from the Al pads are due to the Al exchanged with the Ge during the annealing procedure. The brighter segment is the Ge segment, whose length depends on the temperature and duration of the annealing process and on the width of Ge sheet and Al pads. The samples analyzed in this work have Ge segment lengths ranging from 60 nm to 100 µm.

The Al-Ge-Al nanosheets on top of the oxide and handle wafer of the GeOI resembles a back-gated transistor, hence the conductance of the device can be tuned by controlling the back-gate voltage (V_{BG}). At large negative V_{BG} the majority carriers in the channel are holes, so there is a p-type behavior, while at positive V_{BG} the majority carriers are electrons, so the device is n-type.

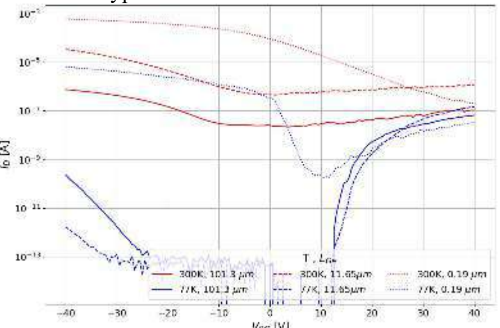


Fig 2 Transfer characteristics for Al-Ge-Al heterostructure devices with various Ge channel length as a function of the gate voltage (V_G)

The analysis of transfer characteristic measured as a function of temperature, reported in Fig. 2, shows an interesting behavior at V_G=+40 V. The current flowing through the channel reaches the same value at every temperature and for every NW length. We can conclude that the physical effect contributing to the current in the n-type regime does not depend on temperature and length. We believe that in this regime, carriers diffuse by tunneling through the barriers. Conversely, at V_G=-40 V the transfer

characteristics give the expected result, namely at room temperature, the current is dependent on the length of the Ge NW, being dictated by the resistance of the channel. Whereas at 77 K, ballistic transport becomes evident also for devices longer than the ballistic transport range at room temperature (>100 nm).

To better understand these findings, we performed a dedicated investigation of the Schottky barrier height. The measurements were performed by using a cryostat under dark conditions [3]. The transfer characteristics were acquired for all the analyzed devices at different temperatures and at different voltages between source and drain (V_{DS}).

We want to obtain an effective Schottky barrier plot at V_{DS}=0 V ($\varphi_{0,eff}$) as a function of the V_G. In order to have this the thermionic theory can be used to calculate the current flowing through the channel. For each V_G and V_{DS} considered, the logarithmic plot of I_D*T^{-2} as a function of 1/T (Richardson plot) can be used to extrapolate the voltage-dependent Schottky

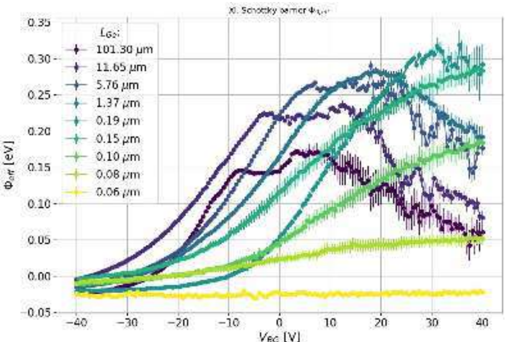


Fig 3 Schottky barrier for Al-Ge-Al heterostructure devices with various Ge channel length as a function of the gate voltage (V_G).

barrier. $\varphi_{0,eff}$ is obtained by a linear fit of φ as a function of V_{DS}: the intercept of the linear fit is $\varphi_{0,eff}$ at fixed V_G. In Fig. 3 we report the curves for $\varphi_{0,eff}$ as a function of V_G for samples with different channel length. The figure shows a trend on the Schottky barrier height for different Ge NW lengths. First, the height of the barrier depends on the length of the Ge NW and on the applied V_G. The Schottky barrier is larger for shorter devices and the maximum is shifted to higher V_G, excepted for ultra-short devices (devices shorter than 200nm). At V_G=-40 V the barrier is small, in good agreement with the well-known Al-Ge band alignment. [4] At -40 V the devices are in the p-type regime. Due to traps at the Al-Ge interface the fermi-level is pinned close to the valence band of Ge so there is virtually no barrier and the holes can be easily injected into the semiconductor.

For the shorter devices the maximum is shifted to very high V_G and for ultra-short devices the maximum is not visible since these devices cannot reach the n-type behavior. For NW shorter than 100 nm a significant reduction of the barrier height can be observed. Such devices are near to the ballistic transport regime so that even at low temperatures it is possible to reach intense currents through the channel.

3. Conclusions

This work enabled us to determine the Schottky barrier height in Ge/Al hybrid nanosheet devices. While the shortest devices were expected to exhibit the largest current, we have however found that at a positive gate bias of 40 V the barrier height increases and the current decreases with the length. We eventually observed ballistic transport regime for ultra-scaled Al-Ge heterostructure devices (below 100 nm). Furthermore, when the nanosheets are 100-200 nm long the Schottky barrier appeared to be maximum and no effective electron injection is possible.

This first electrical characterization will be central to the future use of Ge/Al heterojunctions in nanoelectronics as well as integrated optoelectronic devices.

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Diode characteristics and room temperature EL emission for strained SiGe/Ge quantum well LEDs

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1. Introduction

In recent years, with the growing importance of quantum encryption technology, the use of circularly polarized light for optical communication has been proposed. Spin-LEDs are expected to be used as circularly polarized light emitting devices, and Ge, which can be monolithically integrated on Si substrates and emit light in the communication wavelength band, has attracted much attention as a spin-LED material. In particular, the (111) orientation of Ge enables the epitaxial growth of high-quality ferromagnetic materials on Ge and the injection of spin-polarized electrons from the ferromagnetic materials into the Ge surface [1]. Furthermore, the use of strained SiGe is expected to improve the spin lifetime due to the suppression of inter-valley scattering [2,3]. In this study, we fabricated strained SiGe/Ge-on-Si (111) LEDs using SiGe/Ge quantum wells as the active layer and succeeded in achieving a good on/off ratio and very strong EL emission at room temperature.

2. Sample preparation

SiGe/Ge hetero-structures were grown with solid-source MBE (Fig. 1). First, a tensile strained Ge layer was grown on a p-type Si(111) substrate by a two-step growth method in which a low-temperature (LT) Ge (Tg = 350°C, 40 nm) and a high-temperature (HT) Ge (Tg = 700°C, 500 nm) layers were successively grown. Then SiGe/Ge quantum well active layers and 500 nm P-doped Ge layers were grown at 350°C. After the growth of the p-i-n structure, a 2×10^{14} cm^{-2} δ-P doping was performed to form low resistance contacts, and a 2ML ultra-thin Si layer was also inserted to prevent surface segregation of P atoms [4]. Finally, a Ge layer (7 nm) was deposited. The grown sample was processed into a mesa-shaped diode by standard photolithography and reactive ion etching, followed by AuSb and AuGa deposition as top and back contacts, respectively. Figure 2 shows a laser microscope image of the fabricated device.

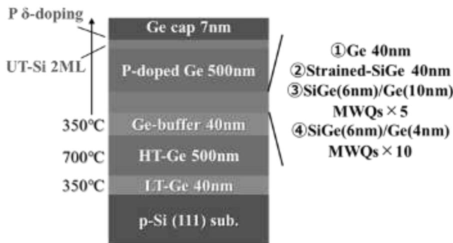

Fig. 1. Fabricated Ge-on-Si(111) LEDs with various active layers of Ge, strained-SiGe, SiGe/Ge MQWs(×5 and ×10)

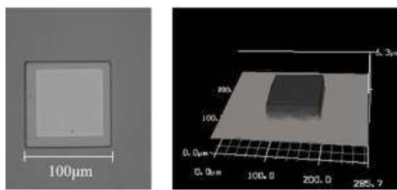

Fig. 2. Laser microscopic views of the device.

3. Results and Discussions

Figure 3 shows I-V characteristics of the fabricated diode devices with active layers of Ge, SiGe and SiGe/Ge MQWs (5 or 10 layers). Applied voltages are ranged from -0.5 V to 0.5 V. Compared to the diode with the Ge active layer, off-leakage currents are found to markedly decrease for the diodes with active layers of SiGe and SiGe/Ge MQWs. The on/off ratios are compared among 4 diodes as shown in Fig. 4. First, it was confirmed that changing the active layer from (1) Ge (on/off ratio = 8) to (2) SiGe (on/off ratio = 95) improved the off-leakage by about an order of magnitude. This is thought to be due to the band offset resulting from the strained SiGe layer acting as a barrier. A further improvement in off-leakage was confirmed by using SiGe/Ge multiple quantum wells in the active layer up to on/off ratio of 331 for (3) 5 SiGe/Ge quantum well layers and on/off ratio of 457 for (4) 10 layers.

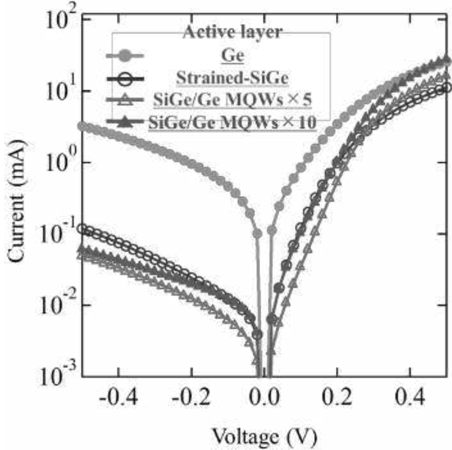

Fig. 3. Current-Voltage characteristics of Ge-on-Si LED.

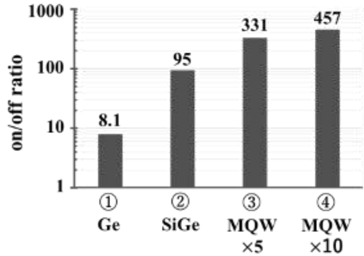

Fig. 4. The on/off ratio of the fabricated LEDs.

Figures 5 and 6 show EL spectra obtained at room temperature around higher and lower emission energy region, respectively, with various injected currents. The inset in Fig. 5 shows the EL intensity as a function of injected current.

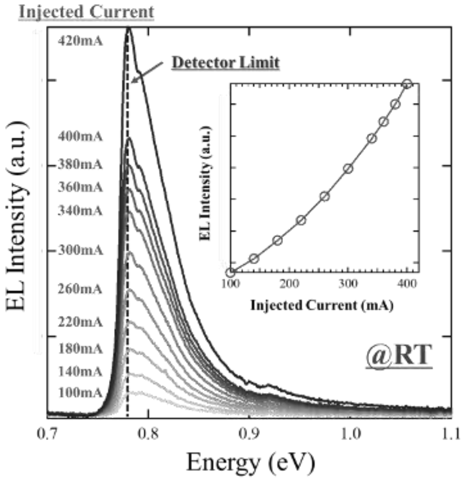

Fig. 5. RT EL spectra obtained around higher emission energy region for Ge-on-Si(111) LED with SiGe/Ge MQWs as active layer. The inset shows EL intensity against injected current.

Very strong EL spectra were obtained for both regions. It is noted that, around the lower energy region, several peaks are found at 0.63, 0.65 and 0.67 eV, assignments of which to QW confinement energy levels or resonant emission energies are undergoing.

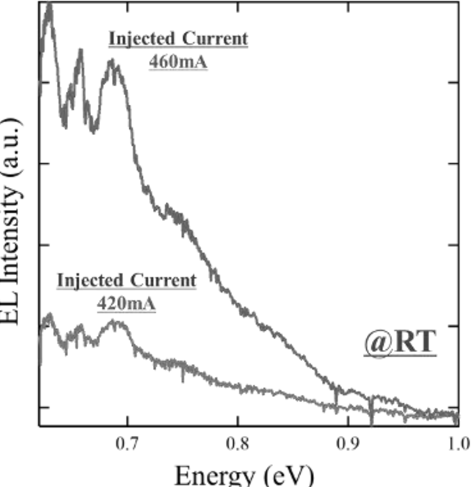

Fig. 6. RT EL spectra obtained around lower emission energy region for Ge-on-Si (111) LED with SiGe/Ge MQWs as active layer.

4. Conclusions

Light emitting diodes involving strained SiGe/Ge quantum wells as active layers were fabricated based on Ge-on-Si(111) virtual substrates. It was demonstrated that on/off ratio was significantly improved for diodes with SiGe/Ge MQWs compared to Ge as the active layers. As a result, very strong room temperature electroluminescence was obtained. These results indicate that the strained SiGe/Ge-on-Si structure is very promising as light emitting devices toward Si photonics applications.

Acknowledgements

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Modeling of Selectorless RRAM with Transient Characteristics for Computing-in-Memory Application

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1. Introduction

The advance of semiconductor industry pushes the evolution of artificial intelligence. However, the bottle neck of von-Neumann machine constrains the development of AI industry. Thus, the concept of computing-in-memory (CIM) mimics the human brain which consumes very low energy compared with AI machine designed with von-Neumann architecture. As for the development for the CIM application, researchers put more effort on this fast grown research field of non-volatile memory (NVM) for next generation application.

Among the NVM the resistive random-access memory (RRAM) shows its advantage regarding switching speed, operating voltage, CMOS compatibility and scaling. As for scaling, the high-density array could be achieved by utilizing the bilayer MIIM structure of transition metal oxide (TMO). The inserted material would increase the selectivity of RRAM that shows better stand by leakage current. The characteristic could be shown in Fowler Nordheim tunneling (FNT) and direct tunneling (DT) form [1,2]. Also, there are still some other mechanisms measured such as space-charge-limited current (SCLC) and Ohmic conduction during the voltage sweep [3]. These conduction mechanisms, either bulk limited, or electrode limited, could cover the transport behavior in the insulator fabricated by different methods, such as thermal grown, plasma-enhanced atomic layer deposition and solution deposition [4]. In this paper, the author propose a compact model that predicts the coexistence of both SCLC and tunneling behaviors for vast RRAM devices that are designed to adopt this novel concept and provides behavior prediction for CIM application.

2. Model methodology

The proposed model is built by SPICE compatible language, Verilog-AMS, which is widely used in semiconductor industry. To simulate the characteristics of RRAM cells, the model is mainly composed of a current calculation module, gap (filament) formation module and temperature calculation module. As shown is Fig.1, The gap formation model would calculate the movement of filament as follows:

$$dg/dt = v_o \exp(-U_a/kT)\sinh(qarE/kT). \quad (1)$$

where g is the tunneling gap between electrode and filament, U_a is the activation energy, a is the oxide lattice constant, and v_o and r are the escape attempt frequency and local enhancement factor, respectively, that could be extracted from different measured devices. E is the electric field across the oxide. The ionic drift/diffusion acts as the driving force of the conductive filament evolution. Thus, the tunneling gap would be determined. Then the electric field across the dielectric layers under different kinds of bias condition can be determined.

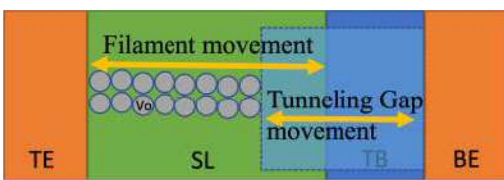

Fig. 1. Schematic of RRAM Schematic of tunneling gap and filament formation. The RRAM cell is composed of top electrode (TE), switching layer (SL), tunneling barrier (TB) and bottom electrode (BE)

The transition between direct tunneling (DT) and FN tunneling could limit the output current of RRAM in low-resistance state (LRS) at low electric field. Thus, the tunneling barrier creates the high selectivity of RRAM devices. The tunneling current can be expressed as follows:

$$J_{FNT} = AE^2 \exp(-B/E) \quad (2)$$

$$J_{DT} = AE^2 \exp(-BD/E). \quad (3)$$

where A and B can be extracted from experiment data, D is the correction term for direct tunneling, and E is the electric field. And then the total current is calculated by multiplying J and the filament contact area.

In the work of [5], the model assumed the metallic like filament as extension of metal electrode Fermi level, which simplified the current evaluation process and worked with some of the experimental cases [2]. To expand the usage for other measured cases that show bulk limited transport behavior, additional mechanisms should be considered, as demonstrated in this paper.

The typical SCLC and ohmic conduction behavior is described as follows,

$$Jsclc = (9/8)\mu\varepsilon(V^2/d^3) \quad (4)$$

$$Johm = q\mu n(V/d) \quad (5)$$

where μ is the mobility in the dielectric, ε is the dielectric constant, and d is the dielectric thickness.

As shown in Fig.1, the current transports between BE and TE. The transport mechanism is combined with both tunneling and SCLC for various device bias conditions in the model. While the tunneling gap shrinks, the electric field across the tunneling gap would rise, that mainly affects the value of tunneling current. In the meantime, the ohmic/SCLC conductive path increases that lower its output value. At high electric field regime, the FNT would dominate the output. At the low electric field regime, SCLC behavior dominates the output current. This phenomenon is also consistent with the observation in [4].

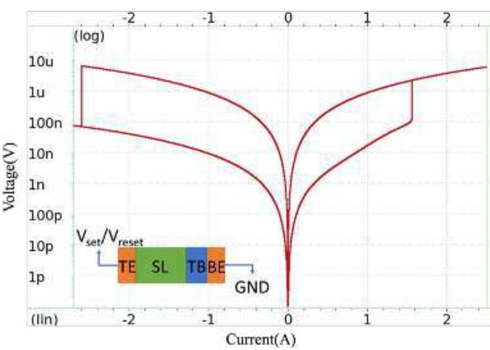

Fig. 2. The simulated IV characteristics of the RRAM device under set voltage and reset voltage.

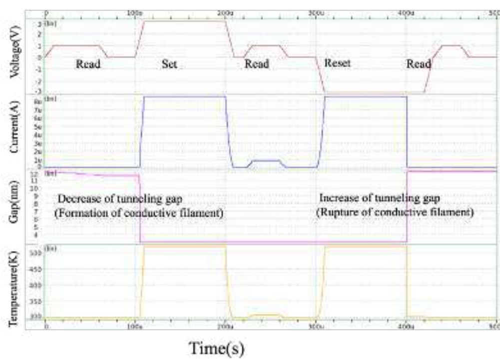

Fig. 3. The simulated transient behavior of the RRAM device under set voltage and reset voltage.

3. Conclusions

In this paper, we have proposed a selectorless RRAM compact model that is able to predict cell level behavior in nonvolatile memory array for device design consideration. Also, the model can emulate the volatile behaviors for computing-in-memory application.

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Impact of substrate doping on the performance of vertically illuminated Ge-on-Si photodetectors

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1. Introduction

Ge-on-Si photodiodes have been studied for more than twenty years, mainly for their application in integrated photonics in a waveguide configuration. [1] These devices tolerate fairly high dark current densities since the small volume and high optical power results in a sufficiently large signal to noise ratio.
Vertically illuminated photodetectors are instead required for imaging applications, of interest in the automotive and biomedical areas. In this case, a sufficiently low dark current density is required for the fabrication of multipixel devices. [2] [3]

Indium gallium arsenide is the state-of-the-art material for infrared imagers due to the lower dark current density (≈10^{-7} A/cm^2) as compared to Ge-on-Si (≈10^{-2} A/cm^2), but this kind of detectors are rather expensive (>10k€/device) while, Ge-on-Si photodetectors (~100€/device) can be produced in CMOS foundries. The difference in the dark current of the two materials mainly arises from fundamental physical reasons. In fact, the dark current density is proportional to the intrinsic carrier concentration that is proportional to the effective masses, as shown in eq. (1).

$$J_d \propto n_i^2 \propto m^{*3/2}. \quad (1)$$

The direct band structure of the InGAs results in an electron effective mass (m_e*=0.037 m_0) substantially lower than that associated with L-valleys electrons in Ge (m_e*=0.22 m_0). As a consequence, for an indium gallium arsenide alloy featuring a 0.8 eV bandgap, *i. e.* equivalent to the direct-bandgap of germanium, the intrinsic carrier concentration is 50 times smaller than that of Ge. Yet, the dark current of epitaxial Ge-on-Si devices is orders of magnitude larger than that of bulk Ge detectors, indicating that, despite the fundamental limits set by the Ge bandstructure, there's still room for reducing the reverse current of Ge epitaxial layers.

In recent years the reduction of threading dislocations [4] and the implementation of surface passivation [5] strategies have been investigated to reduce the dark current density. Instead, the effect of the doping profile of the silicon-germanium heterostructure on the dark current has been not fully analyzed. Starting from the paper by Osmond *et al.* [6], in which it possible to find some relation between the substrate doping and the dark current density, we have made a systematic analysis of Ge-on-Si photodiodes grown on silicon substrates with different doping levels. In this work we will report on the growth and fabrication of the Ge-on-Si photodiodes and their characterization. Temperature dependent current-voltage and capacitance-voltage measurements have been performed to obtain information on the physical mechanisms giving rise to the dark current in heterojunctions with different doping profiles. The device characterization has been completed by performing photocurrent measurements to estimate the responsivity and detectivity dependence on substrate doping.

2. Samples growth and fabrication

To evaluate the impact of silicon substrate doping on dark current and photoresponse, a set of Ge-on-Si p-i-n structure were grown by LEPECVD (Low-Energy Plasma Enhanced CVD) and microfabricated by optical lithography and reactive ion etching.

All the investigated photodiodes feature a 1500 nm thick nominally intrinsic germanium layer, and heavily p-type doped Ge top contact layer with a thickness of 100 nm. The intrinsic germanium layer is annealed to reduce the threading dislocations density. The silicon substrates doping has been varied from 10^{15} cm^{-3} to 10^{19} cm^{-3}. Metal contacts are deposited by E-Beam Evaporator. The scheme of the final structure is reported in Fig.1.

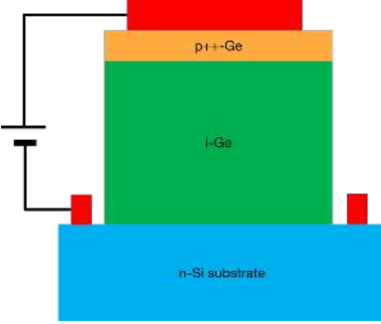

Fig. 1. Structure of the Ge-on-Si photodiode.

3. Electrical characterization

To characterize the photodiodes current/voltage measurements have been performed. The resulting dark current densities are shown in fig. 2 for the case of 3×10^{15}(n), 3×10^{16}(n+) and 1×10^{19}(n++) phosphorous atoms per cubic centimeter. A clear trend between the dark current density and the doping levels of the substrates is observed.

Dark current in Ge-on-Si devices arises mainly from three mechanisms: diffusion, generation-recombination and trap-assisted tunneling. Temperature dependence I-V and C-V measurements have been performed to evaluate the relative weight of these three different mechanisms in determining the dark current.

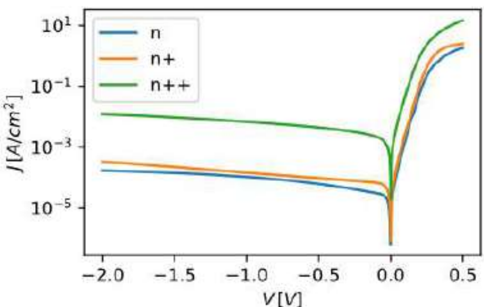

Fig. 2. Dark Current Density for different doping levels of the Si substrate

These measurements indicate that, at room temperature, generation-recombination and trap assisted tunneling give the main contribution to the total dark current. These two mechanisms depend on the depletion region width in germanium and so, on the doping levels in the heterojunction.

4. Optical characterization

To characterize the photoresponse of the photodetectors, the responsivity has been measured in the wavelength range between 1300-1700 µm, for different reverse biases. Specific Detectivity has also been estimated as a figure of merit of the detector.

The results for an applied bias of -1V are shown in fig. 3. It possible to observe that the Responsivity decreases with the doping level of the silicon substrate, along with the dark current. The Specific Detectivity, results to be the most appropriate figure of merit to describe the device performance since it depends on both the quantities.

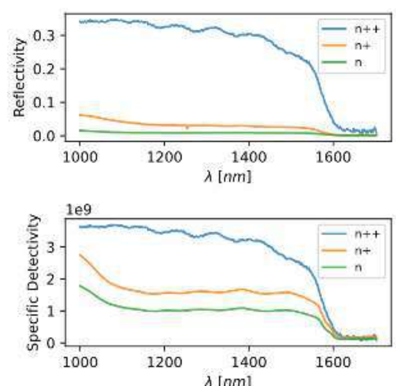

Fig. 3. Responsivity and Specific Detectivity with an applied bias of -1V.

5. Conclusions

We have observed that the generation-recombination and trap-assisted tunneling mechanism give an important contribution to the total dark current, and since they both depend on the depletion region width in the Ge layer, they are strongly influenced by the substrate doping level.

Photocurrent measurements indicate that there might be an optimal substrate doping level maximizing the Specific Detectivity of the Ge-on-Si photodetectors.

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Controllable charge distribution and dynamics of conduction electrons around metallic nanowires

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1. Introduction

The successful advances in the microelectronic industry have included critical approaches to boost silicon-based technologies and to introduce silicon-compatible alternatives. At the same time, size reduction remains a priority, with the ongoing generalization of integrated circuits with 7 nm or less as characteristic length. As these dimensions approach the range in which quantum effects become important and connections between elements appear as quantum wires, the knowledge of the quantum-mechanical properties of charge carriers in nanoscale devices has become key to the design of future nanocircuits.

Fortunately, 1D semiconductor nanostructures such as nanowires, nanobelts, and nanotubes have been the subject of intense research in both academia and industry so that the quantum properties of charge carriers in these structures are rather well known. An important result concerns the confinement of the charge carriers in quantum states *inside* the wires if they are thin enough, which allows practical applications in the fields of electronics and optoelectronics. Quite remarkably, in contrast, the properties of charge carriers in the *outside* vicinity of nanowires in semiconducting media have attracted little, or even no attention at all. Thus, there remain many unanswered questions for such a case. For instance, do quantum states form around nanowires? What are their quantum-mechanical properties? How do these properties depend on the wire electric potential and on its size? Do the transitions between these states give rise to resonances in the electromagnetic spectrum? These are important questions whose answers could contribute to the understanding of the quantum mechanics of electrons in semiconductors as well as to the development of new electronic and optoelectronic devices.

In this theoretical work, we study these questions in the case of charge carriers bound around charged metallic wires inside a semiconductor film. We show that the eigen energies of the quantum-mechanical states expectably depend on the bias voltage, making the transition frequencies easily tunable. This is in opposition to the case of applications based on transitions inside semiconductor nanowires whose energies are mainly determined by the size and shape of the wires so that changing the transition frequencies by means of an applied voltage is not easily achievable.

2. Model and Methodology

Obviously, the interaction of a single cell with the radiation field is too weak to have noticeable effects in practice. This leads us to consider an array of wires rather than a single isolated one. We choose a regular centered square lattice of parallel metal nanowires embedded in an insulating or weakly-doped *n*-type semiconductor film and aligned perpendicularly to the film surface. They are located at the corners and centers of the square lattice, as shown in Fig. 1. The semiconductor film (GaN in our study) is enclosed at the top and bottom by insulating layers to keep the charged carriers confined in it. The wires at the square corners, or vertices, are at a common potential taken as ground potential while those at the square centers, connected together, are at a different potential, which we call the bias voltage. The wires are wrapped in an insulating sheath of HfO_2. The high dielectric constant and the large energy gap make this oxide a nearly perfect insulator. It should also avoid any charge exchange between the semiconductor film and the metal wires in the case of these systems.

Since the doping level in the semiconductor film is sufficiently weak, we consider that electrons are present in low concentration such that the Fermi level lies relatively close to the ground-state energy of the states bound to the central wires. In the case of thin wires, so that the eigenfunctions are somewhat compact, the Coulomb repulsive energy between electrons prevents the occupation of the bound states by more than a single electron and we can restrict ourselves to the study of single-electron properties. In the case of thick wires, the average distance between electrons in different eigenstates is large and the Coulomb repulsion is too weak to prevent the occupation of a cell by several electrons. However, the same electrical interaction is also too weak for the correlations between electrons to play an important part in the studied properties, especially in the optical ones. Therefore, the one-electron approximation used in this work seems appropriate for both thin and thick nanowires. We neglect spin-orbit coupling and relativistic effects and we use the well-known effective-mass approximation for the electrons. On

this basis, the sought electron eigenstates and eigenvalues are the solutions of Schrödinger's equation with the electric potential distribution in the cell array. Technical details can be found in Ref. [1].

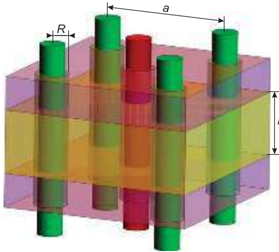

Fig. 1. View of a square cell of the wire array. R: wire radius, including the thickness of the insulator sheath; a: lattice parameter; h: film thickness.

3. Results

The electric-potential distribution $V(\mathbf{r})$ to be used in Schrödinger's equation is first obtained by solving the 2D Laplace equation inside a cell with periodic boundary conditions on the square sides opposite to each other and Dirichlet conditions on the wires bringing them either to the ground potential or to the bias potential, depending on the wire position. The AC/DC module of the COMSOL Multiphysics platform [2] was used to that purpose.

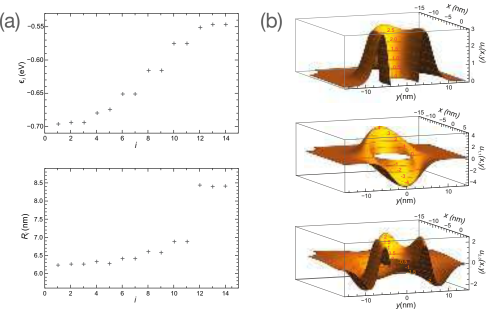

Fig. 2. (a) Eigen energies (top) and average wave function radii (bottom) of an array with R = 4 nm and a = 30 nm as function of the solution number i. (b) Cut views of 3 wave functions: (top) ground-state, (middle) first excited state in the first shell, (bottom) first state in the second shell.

Figure 2(a) gives the eigen energies and average electron-charge radii of the 14 first solutions versus i, the eigenstate number in order of increasing eigen energies. The results show that the eigenstates can be grouped into different shells as in atomic physics. The difference in radius between the first two shells is clearly visible while the difference in energy between eigenstates in different shells depends on the wire radius and the bias voltage but is typically a few tens of meV. Inside a shell, the radii have almost the same value for all the wave functions and the energy distribution is almost continuous. The wave functions in the ground-state, the first excited state of the first shell, and the first state of the second shell are shown as cut-views in Fig. 2(b).

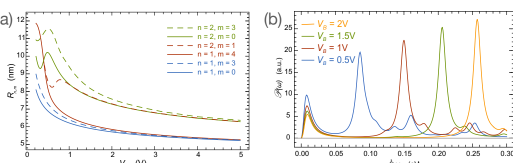

Fig. 3. (a) Average wave function radius as function of bias voltage for different (b) Absorbed power vs. incident photon energy for different bias voltages

Calculations also show that the eigen energies decrease almost linearly with increasing bias voltage, the energy shift being equal for all states in a given shell. The eigen energies of states in high-order shells (those with quantum number $n > 1$), depend more strongly on the bias voltage. This is an interesting property as the possible optical applications would probably involve transitions between states with different values of n. The average distance of the electron from the central cylinder axis decreases with increasing bias, as shown in Fig. 3(a) for a few low-order states. The behavior of the eigenstates in the shells with $n > 1$ deviates from this rule at low bias voltages. We find that in this case, the wave function is not localized next to the central wire.

The energy of excitation between two different shells of levels is in the range of 10meV or a few tens of meV. This corresponds to photon frequencies in the THz range, where emitters and detectors are not numerous, leading to a potential application as radiation detector that exploits the modification of the in-plane electrical conductivity brought by an electromagnetic wave. Thus, we determined the linear response of the bound electrons to an ac electric field. Figure 3(b), where the absorbed power is plotted as function of the incident photon energy for different bias voltages, shows that if photodetectors based on the studied system could be built, they could be easily made tunable in a range from 10 THz to 100 THz.

4. Conclusions

Conduction electrons in a semi-insulating dielectric film containing a centered square array of metal nanowires normal to its plane are bound in quantum states around the central wires if a positive bias voltage is applied between the wires at the square vertices and these latter. We show that the position of the absorption peaks is strongly dependent on the bias voltage. This makes them good candidates for the development of easily tunable novel infrared devices.

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Structure and electrical property of polycrystalline silicon trap-rich layer by in-situ annealing

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1. Introduction

Polycrystalline silicon (Poly-Si) is widely used in the field of radio-frequency silicon-on-insulator (RF-SOI) since its grain boundary (GB) as trap-center in the band gap can effectively capture free carriers [1]. As RF-SOI wafers access to the 300mm market, wafer warpage is a non-negligible problem that lead to film cracking and process failure [2]. Poly-Si layer will introduce high compressive stress, which seriously worsens the warpage of RF-SOI wafer. The compressive stress of polycrystalline films can be effectively released by high-temperature annealing [3]. However, for phosphorus-doped Poly-Si, the film conductivity can be enhanced by high-temperature annealing because the increase of grain size and the generation of specific GBs are promoted [4]. To meet the high trap density requirements of high-frequency applications, undoped Poly-Si layers with small grain sizes prepared by chemical vapor deposition (CVD) are required. In this work, the variation of electrical resistivity of undoped Poly-Si films grown by atmospheric pressure chemical vapor deposition (APCVD) after in-situ high-temperature annealing are reported. In addition, the GB evolution of Poly-Si layers during in-situ annealing is investigated. It is indicated that the low bulk resistivity of Poly-Si after in-situ annealing is caused by the decrease of the overall GB density and the generation of CSL low-Σ GBs.

2. Experiments and characterization

In this study, two 300 mm high-resistivity silicon (HR-Si) wafers with a native-oxide layer (≤15Å) were used as substrates. Poly-Si films were grown by APCVD process using hydrogen and trichlorosilane as gas source. One of the two wafers is in-situ annealed in the reactor after deposition. Then, Poly-Si films of two samples were polished to 2μm thickness by chemical mechanical polishing process. The resistivity distribution with depth of samples was measured by spreading resistivity profile (SRP) technique. The grain size and GB distribution were investigated by transmission kukichi diffraction (TKD). The hydrogen concentration of the films and substrates was obtained by secondary ion mass spectrum (SIMS).

3. Results and discussion

The second-harmonic level of coplanar waveguide can be reflected in the RF substrate resistivity distribution. The resistivity distribution curves of as-deposited and as-annealed Poly-Si layers with depth are shown in Fig.1. The decrease of bulk resistivity with depth is caused by SRP model [5]. The bulk resistivity of Poly-Si does not change with film thickness [6], so that the bulk resistivity of films is approximated by the near-surface value. It is demonstrated that the bulk resistivity of Poly-Si layer is significantly reduced by in-situ annealing.

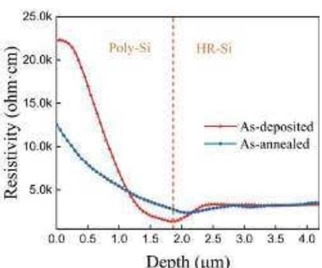

Fig.1. Resistivity distribution of as-deposited and as-annealed Poly-Si layers with depth

The oriented-grain distribution of deposited and annealed polysilicon is analyzed by TKD, as shown in Fig.2. There are a lot of tiny grains on the polished surface of the as-deposited Poly-Si layer. Due to the recrystallization of grains during the thermal process, the tiny grains are aggregated as larger grains, which results in the decrease of GB density. The average grain sizes of the two samples are 52.76nm and 131.78nm, respectively. It is illustrated that in-situ annealing significantly lowers the trap-state density of Poly-Si while reducing the GB density by almost two times.

The quantitative analysis on the variation of as-deposited and as-annealed Poly-Si misorientation are

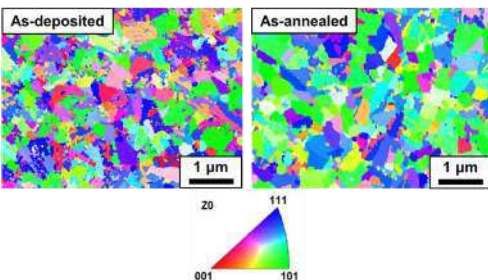

Fig.2. Surface oriented-grain mapping of as-deposited and as-annealed Poly-Si layers

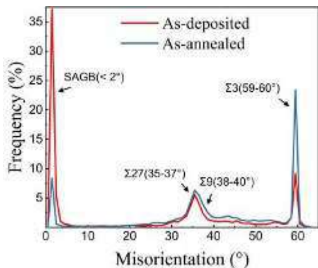

Fig.3. Misorientation distribution of as-deposited and as-annealed Poly-Si layers

shown in Fig.3. Each type of GBs has a corresponding misorientation angle. The results show that small-angle grain boundaries (SAGBs) reduce by about 30% and the Σ3 GBs increase by about 13% after in-situ annealing. The unstable SAGBs transform into low-energy CSL low-Σ3 GBs as a result of the high quantity of energy released during thermal process. Compared to SAGBs, Σ3 GBs have lower mobility and electron recombination activity [7]. Therefore, the trap density at the single boundary of polysilicon decreases during the annealing stage.

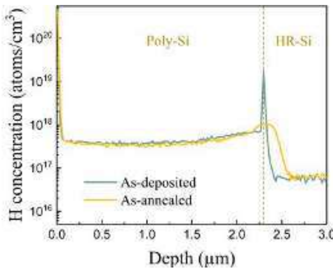

Fig. 4 Hydrogen concentration distribution with depth of as-deposited and as-annealed Poly-Si layers

Hydrogen concentration distribution curves with depth of as-deposited and as-annealed Poly-Si wafers are shown in Fig.4. There is a hydrogen peak as high as 2E19 cm^{-3} at the Poly-Si/HR-Si interface before in-situ annealing. It is considered that the free hydrogen molecules in the chamber will combine with dangling bonds on the HR-Si surface to form weak Si-H bonds in the pre-deposition stages. In the deposition process, Si-H bonds are to break due to the high temperature. The free hydrogen ions will be captured by trap-states in the Poly-Si GBs at the Poly-Si/HR-Si interface. During in-situ annealing, the hydrogen atoms gain energy to escape and mainly diffuse to the HR-Si substrate with trap-free state. The hydrogen concentration at the interface becomes similar to that in the Poly-Si layer, and the resistivity dip at the interface disappears.

4. Conclusion

In summary, in situ high-temperature annealing is assumed to be an unfavorable post-treatment process for the RF performance of Poly-Si trap-rich layers. The bulk resistivity of Poly-Si decreased significantly during in-situ annealing for the following two reasons: First, recrystallization of Poly-Si occurs during in-situ annealing, reducing the overall GB density; Second, SAGBs with high recombination activity transform into CSL-Σ3 GBs with low recombination activity. However, the dip in the resistivity of the Poly-Si/HR-Si interface disappears due to the out-diffusion of hydrogen by in-situ annealing.

Acknowledgements

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First-Principles Calculation of Alloy Scattering for $Ge_{1-x}Sn_x$ and their Contribution to the Mobility.

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1. Introduction

Silicon microfabrication technology has focussed on producing smaller, more efficient integrated circuits (ICs). However, at present, the heat generated during the switching of transistors is starting to limit achievable switching rates [1]. In response, an attempt has been made to grow higher mobility semiconductors such as strained Ge [2, 3]. Alloying is a commonly used method of engineering the mechanical, optical and electronic properties of semiconductors, and this work shows that alloying Ge with Sn can increase the mobility by effecting transport on the direct conduction band at Γ, as suggested by Sau et al [1]. At the same time, alloy scattering can significantly reduce the mobility. To determine if the mobility can be significantly increased, and what amount of alloying is necessary, we use first principles methods to calculate the alloy scattering parameters and the mobility of the GeSn alloy as a function of composition.

2. Method

2.1. Alloy Scattering Parameters

The required carrier scattering matrix elements are calculated from the energy splitting of nearly degenerate Bloch states [4], which arise when one host atom in a supercell is replaced by a Ge or Sn atom. In this case, a Sn atom replaces a Ge atom in a 64 and 128-atom supercells. Scattering parameters for all relevant L, Γ, ½X and X intra-valley and inter-valley scattering are calculated. Atomic relaxation affects the scattering parameters significantly. Calculations are performed in a plane-wave pseudopotential formalism using Density Functional Theory with the ABINIT code [5].

The alloy scattering matrix elements are calculated using the following [4]

$$\langle V_{\alpha\beta}\rangle = \langle V_{\alpha\beta}^{Sn}\rangle - \langle V_{\alpha\beta}^{Ge}\rangle = N\langle\psi_\alpha|\Delta V^{Sn}|\phi_\beta\rangle - N\langle\psi_\alpha|\Delta V^{Ge}|\phi_\beta\rangle \qquad (1)$$

where ΔV^A is the perturbing potential caused by the substitution of an impurity into periodic host by atom A, ψ is the Bloch state of the periodic host lattice and ϕ labels the eigenstate in the presence of the perturbing potential.

2.2. $Ge_{1-x}Sn_x$ Mobility

The properties calculated are used to find the alloy scattering contributions to the room temperature n-type electron mobility of GeSn, which is predominantly determined by the electron-phonon scattering rate $R_\lambda^\alpha(E)$ and the material's effective mass $m_\lambda^{(\alpha)}$ at valley α, where λ runs over the longitudinal and transverse directions. The mobility is described by the relation below,

$$\mu_{\lambda\lambda}^{(\alpha)} = \frac{2e}{3k_BTn^{(\alpha)}m_\lambda^{(\alpha)}}\int_{E_c^{(\alpha)}}^{\infty} dE\,\frac{E\rho^{(\alpha)}(E)}{R_\lambda^{(\alpha)}(E)} \qquad (2)$$

where $\rho^{(\alpha)}(E)$ is the density of states at α and $n^{(\alpha)}$ is the carrier density at α. Since the conduction band minima occur at L and Γ for Ge and Sn respectively, the scattering rates and effective masses were found at these valleys. The alloy scattering rates $R_{\alpha\beta}$ at valley α were calculated using [4],

$$R_{\alpha\beta} = \frac{2\pi}{\hbar}x(1-x)\frac{a_0^3}{8}\sum_\beta\left|\langle V_{\alpha\beta}\rangle\right|^2\rho^\beta(E) \qquad (3)$$

where x is the Sn content, a_0 is the cubic lattice constant, β represents the valleys into which scattering occurs and $\rho^\beta(E)$ is the density of states in the final valley β. The electron-phonon contribution is

calculated using deformation potentials and phonon energies of Ge from [6-9]. Since we only consider low Sn content (0-25%), we use the scattering parameters corresponding to Ge.

3. Results

We calculated all relevant scattering matrix elements for the intra-valley and inter-valley scattering at the L and Γ valleys in $Ge_{1-x}Sn_x$.

The intrinsic n-type room temperature mobility, using the Boltzmann transport equation in the relaxation time approximation, is found to be 4384 $cm^2 V^{-1} s^{-1}$ for Ge, which is within reasonable agreement with experiments on unstrained bulk alloys (3900 $cm^2V^{-1}s^{-1}$ for Ge [10]).

Figure 1 (below) displays the behaviour of the mobility of GeSn against Sn concentration and also against the difference in energy between the L and Γ valleys. From this figure, we can see that alloying Ge with a Sn lowers its mobility to 570 $cm^2 V^{-1} s^{-1}$ at 8% Sn. Beyond this concentration, the material becomes a direct gap material and the mobility begins to increase. To significantly raise the mobility beyond that of pure Ge, the conduction band energy of the Γ valley must be 0.06 eV lower than the L valley, which occurs at a concentration of at least 11.5% Sn. The proportion of electrons at Γ must be at least 0.058 in order to achieve an increase mobility greater than that of Ge. We can also see from the figure that the maximum mobility in GeSn for low Sn concentrations to be 42,770 $cm^2 V^{-1} s^{-1}$. This occurs at 19% Sn, where the conduction band energy of the Γ valley is 0.175 eV lower than the L valley, and the proportion of electrons at Γ is 0.864. Beyond this point, alloy scattering reduces the mobility.

4. Conclusions

The increase found in the mobility of Ge due to alloying with Sn alongside the alloy's direct band gap could make GeSn a more attractive semiconducting material than pure Ge. At the presentation, we will use our parameters to find what combination of GeSn alloying and strain can increase the n-type mobility.

Acknowledgements

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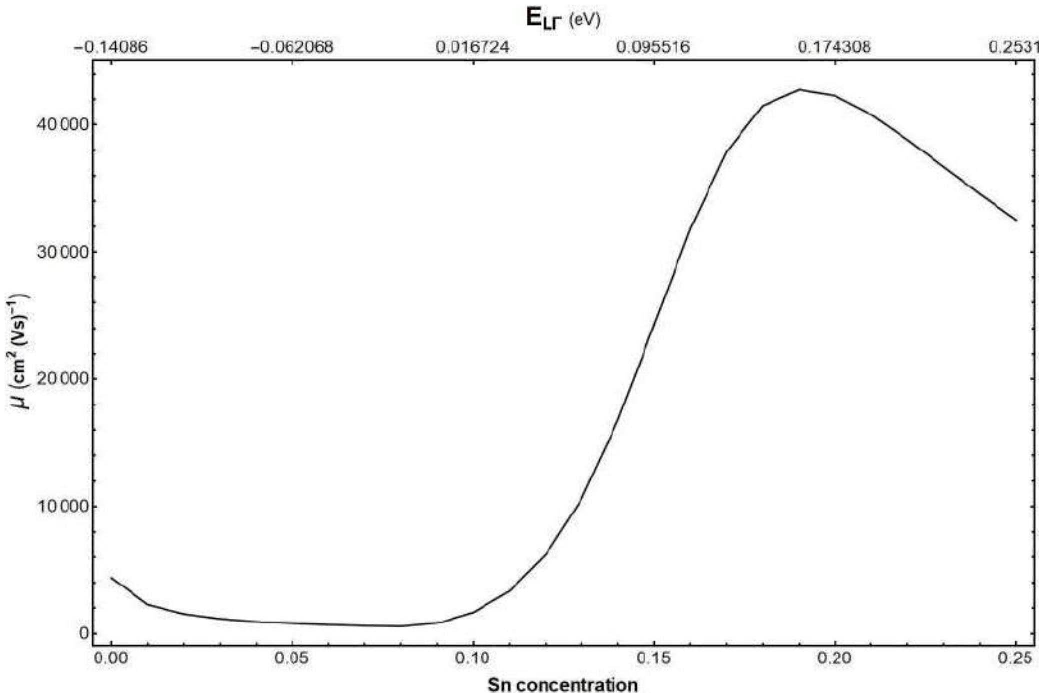
$E_{L\Gamma}$ (eV)
−0.14086
−0.062068
0.016724
0.095516
0.174308
0.2531
40 000
30 000
20 000
10 000
0
μ (cm² (Vs)⁻¹)
0.00
0.05
0.10
0.15
0.20
0.25
Sn concentration

Voids detection in trenches filled with N-type doped silicon

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1. Introduction

We recently investigated the filling of trenches in Si with Si:P Selective Epitaxial Growth (SEG) [1]. Co-flow processes with the use of various SiH_2Cl_2/HCl Mass-Flow Ratios (MFRs) enabled us to properly fill cavities. To benefit from good electrical performances, defect-free filling is mandatory, however. Reliable characterization techniques are thus required to detect voids with appropriate spatial resolution. Scanning Electron Microscopy (SEM) and Transmission Electron Microscopy (TEM) are techniques typically used to investigate cavity filling [1-4]. Their main drawback is that only a single cleaving plane of the cavity is observed. Some authors tried to overcome such a limitation by acquiring SEM cross-sectional images perpendicularly to different cleaving planes in trenches [5] or by using a Secco chemical etch to reveal filling defects [3]. The latter method was time-consuming and prone to errors if performed manually, however. Moreover, true shapes and numbers of voids cannot be determined from two-dimensional (2D) sections. In 2020, Barzaghi *et al.* [6] overcame such a drawback by using three-dimensional Focused Ion Beam-Scanning Electron Microscopy (3D FIB-SEM), to localize and gain access to the shape of voids.

In this work, we present a reliable characterization methodology to detect voids in trenches filled with N-type doped monocrystalline silicon. The impact of high temperature anneals under H_2 on the morphology of voids in trenches is also investigated, the aim being to annihilate them or at least merge them, reducing thereby their densities in trenches.

2. Experimental procedure

2.1. Epitaxy and annealing processes

Patterned wafers were fabricated by dry-etching rectangular trenches (**Fig. 1**) in P-type doped 300 mm Si (001) substrates covered with 6 µm $P^{(-)}$ layers and oxide/nitride/oxide hard-masks.

Growth was performed in a 300 mm Epi Centura Reduced Pressure – Chemical Vapor Deposition (RP-CVD) chamber from Applied Materials. A chlorinated chemistry with dichlorosilane (DCS or SiH_2Cl_2) and HCl was used to selectively grow at 950 °C, 10 Torr and with H_2 as a carrier gas, N-type doped monocrystalline silicon inside cavities. Phosphine (PH_3) or arsine (AsH_3) were used as phosphorus or arsenic doping precursors. Three steps with varying DCS/HCl Mass-Flow Ratios (MFRs) were implemented during growth, as described in [1].

Annealing processes were carried out just after the filling of trenches to investigate voids evolution during two minute anneals in the epitaxy reactor in a hydrogenated atmosphere (H_2), at low pressure (10 Torr) and high temperature (1000 – 1100 °C).

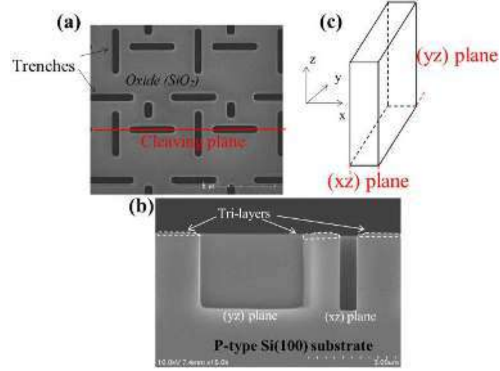

Fig. 1. Etched trenches prior to N-type doped Si trench filling: (a) top-view and (b) cross-sectional SEM images and (c) schematic 3D-view with definition of planes.

2.2. Metrology control

Manual cleaving was used for SEM measurements. This method was controlled optically to cleave as much as possible in the middle of trenches. As cleaving was not always perfectly along a single crystal plane, some trenches were selected to obtain images in the middle of structures. Such a sample preparation technique obviously had a lower degree of control than a FIB (Focused Ion Beam) milling of lamella used for TEM and 3D reconstruction.

3. Experimental results

3.1. Voids detection

SEM observations gave us access to (xz) and (yz) planes, as trenches were at 90° to one another. The planes that could be imaged were semi-random, but regions of interest could be selected and observed. In the same cleaved sample, many different observations were conducted as the whole wafer was not perfectly

cleaved along a single crystallographic plane. Meanwhile, FIB milling used for TEM lamella preparation was site specific, enabling the observation of (yz) planes at the very middle of trenches. As shown in [1], no defects were visible at the substrate/epitaxial growth interface. Small voids (*i.e.* holes in the lattice) were detected away from it. However, SEM and TEM gave us access only to single two-dimensional sections of trenches that may not contain all the information, resulting in erroneous conclusions concerning the suitability of a given filling process. Conventional 2D microscopy methods were therefore not enough and an alternative observation approach necessary.

Detecting filling defects was made feasible by observing three-dimensional structures with FIB SEM. **Fig. 2** shows some 3D reconstructions of trenches filled with Si:P.

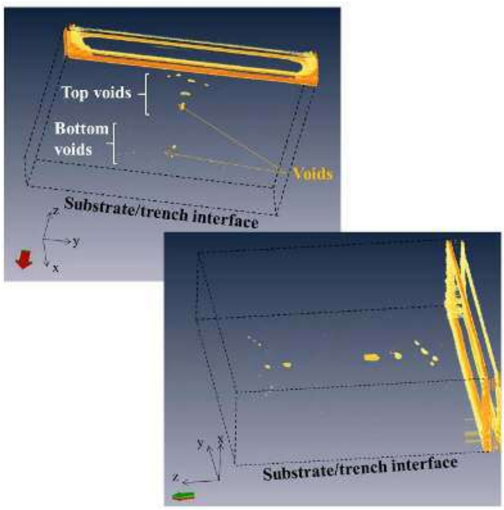

Fig. 2. 3D reconstructions of trenches after their filling.

Voids were clearly detected. They were located in the same sectioned area (yz): the plane in the middle of the trench. Two groups of voids were clearly distinguished: i) at the bottom and ii) at the top of the cavity. Those at the bottom, of a smaller size, seemed to be symmetrical with respect to the (xz) section in the middle of the trench. They could be due to the meeting of (110) lateral planes with the lower (100) plane during the first stages of the filling process. Meanwhile, the upper ones, which were larger, were likely generated when two (110) lateral planes met each other during the latter stages of the growth.

3.2. Impact of H_2 annealing on voids evolution

We used the above technique to track the morphological evolution, upon H_2 annealing, of voids in monocrystalline silicon. The aim was to see whether or not we could use such an approach to localize and, ideally, eliminate them. Voids were still observed whatever the annealing conditions. A difference in the voids morphology and density was obvious, however, when comparing a sample without any anneal and a sample annealed at 1100 °C for 2 minutes (**Fig. 3**). The number of voids was reduced and their size increased, most likely because of merging, after annealing: i) from six before down to two voids after at the top of the trench and ii) from eight down to five voids at the bottom of the trench. Top voids had originally an oval shape. They became round or rectangular with rounded corners after the H_2 anneal.

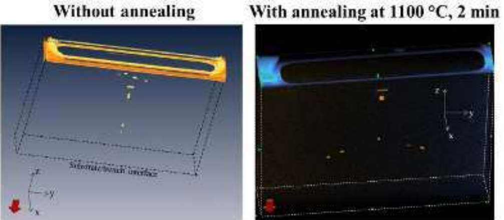

Fig. 3. Comparison between filled N-type doped Si trenches without annealing and after 2 min H_2 annealing at 1100 °C.

4. Conclusions

FIB-SEM characterization, combining focused ion beam milling and scanning electron microscopy, was found to be the best method to characterize trench filling. Three-dimensional reconstructions of cavities were obtained, enabling the detection and spatial localization of voids. This method was more reliable than conventional 2D microscopic techniques such as TEM or SEM. Annealing under H_2 at different temperatures (from 1000 to 1100 °C for 2 min) did not result in a complete healing of filling defects (voids) but their morphologies (dimensions, shapes) evolved. 3D observations helped us optimize our SEG processes, with in the end only a few small voids in trenches.

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Radiative Carrier Lifetime in GeSn Mid-Infrared Emitters

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1. Introduction

$Ge_{1-x}Sn_x$ alloys constitute an emerging class of group IV semiconductors providing a tunable narrow bandgap, which has been highly attractive to implement scalable, silicon-compatible mid-infrared photonic and optoelectronic devices [1]. Notwithstanding the progress in growth processes and device engineering, the impact of structural characteristics on the carrier dynamics is yet to be fully understood. This includes the role of Sn content, lattice strain, and growth defects in shaping the nature and magnitude of the recombination mechanisms and their consequences on the carrier lifetime. Particularly, investigating the latter remains a daunting task due to the lack of methods and tools that can be applied to probe charge carriers in narrow bandgap materials.

Recent studies employed time-resolved photoluminescence (PL) with a nonlinear crystal allowing the upconversion of photons emitted to a shorter wavelength that can be detected by a conventional silicon-based avalanche photodiode [2]. An effective carrier lifetime of $217\,\mathrm{ps}$ at 20 K was estimated for $Ge_{0.875}Sn_{0.125}$ with -0.55% strain using this method [2]. Additionally, by investigating spin-dependent optical transitions leveraging the Hanle effect under steady-state excitation, systematic studies combining modeling and magneto-PL analysis of pseudomorphic layers at a Sn content below 10% reported a radiative lifetime in the 0.5-$2.5\,\mathrm{ns}$ range at $10\,\mathrm{K}$ [3]. However, significantly higher carrier lifetimes reaching $450\,\mathrm{ns}$ were recently reported for $Ge_{1-x}Sn_x$ (x below 0.06) grown on InAlAs buffers as measured by contactless microwave photoconductive decay [4]. This scarcity of studies on carrier dynamics limits the development of accurate and predictive designs of $Ge_{1-x}Sn_x$-based mid-infrared optoelectronic devices.

In this work, we demonstrate that straightforward PL analyses along with the proper theoretical framework are sufficient to alleviate these challenges and extract the radiative carrier lifetime in $Ge_{1-x}Sn_x$ mid-infrared emitters. The approach relies on the simulation of the experimental PL spectra by combining the band structure calculations using the *k.p* formalism together with the envelope function approximation (EFA) and the Fermi's golden rule to estimate the absorption and spontaneous emission spectra. In the following sections, the theoretical framework is described followed by the experimental demonstration using as-grown $Ge_{0.83}Sn_{0.17}$ layers, emitting at wavelengths above $3\,\mu\mathrm{m}$ as a model system.

2. Theoretical framework

The PL spectrum intensity is usually determined using the direct inter-band emission theory and the spontaneous emission spectrum r^{sp} [5], [6] whose computation requires prior knowledge of the band structure of the semiconductors, the momentum matrix elements, and the quasi-Fermi levels. In the literature, for a single bulk direct bandgap semiconductor, r^{sp} is commonly computed using the joint density of states (JDOS) model, which relies on the parabolic bands approximation (PBA), and therefore leading to a set of relatively easy analytical formulas [7]. This model is mostly accurate for a non-degenerately doped semiconductor in weak-injection conditions with the quasi-Fermi levels lying within the bandgap and away from the different band edges by several kT. However, a different picture is expected with increasing values of the excitation power and/or the doping concentration which would shift the quasi-Fermi levels towards the band edges. Besides, for a biaxially strained semiconductor, the $\vec{k}$ direction degeneracies in the Brillouin zone (BZ) are expected to be broken. In this situation, the band dispersion would be more and more anisotropic, challenging one of the core arguments of the PBA.

In our study, r^{sp} is estimated using the eight-band *k.p* formalism together with the EFA Unlike the JDOS model, the evolution of the strength of the optical transitions with the wave vector $\vec{k}$ is explicitly computed. Besides, the computation of the integrals over the BZ, required for estimating the quasi-Fermi levels and r^{sp}, relies on the special-lines approximation (SLA). Within this approximation, the three-dimensional BZ integrals are replaced by a sum of one-dimensional integrals over some characteristic directions (denoted as "special") of the crystal lattice.

The steady-state radiative carrier lifetime τ_{rad} is determined by the net spontaneous emission rate R_{sp}^{net} and the excess carrier concentration Δn, which gives equation (1) [8]. $R_{\mathrm{sp}}^{\mathrm{net}}$ is defined as the amount by which the non-equilibrium spontaneous recombination rate R_{sp} exceeds the

thermal equilibrium generation rate G_0, which is the same as the thermal equilibrium spontaneous emission rate.

$$\tau_{\text{rad}} = \frac{\Delta n}{R_{sp}^{\text{net}}} = \frac{\Delta n}{R_{\text{sp}}^{\text{neq}} - R_{\text{sp}}^{\text{eq}}} \tag{1}$$

Herein, R_{sp} is defined as the integral of the spontaneous emission spectrum r^{sp} over the range of energy greater than the bandgap of the material.

3. Results and discussion

The accuracy of the established theoretical framework has been evaluated through the analysis of the PL spectra, from $Ge_{0.83}Sn_{0.17}$ samples, previously reported in [9]. For these $Ge_{0.83}Sn_{0.17}$ samples, the electrons and holes were reported to diffuse to the top layer (TL), where they should mainly recombine. Indeed, the PL spectra are confirmed to originate from carrier recombination in this specific layer [9]. Therefore, from a theoretical standpoint, the PL results could be analyzed as if they were from a single bulk $Ge_{0.83}Sn_{0.17}$ material. On this basis, the different power-dependent PL spectra, recorded at 4 K, were simulated by iteratively evaluating r^{sp} as well as the excess carrier concentration Δn, and the results are presented in Fig.1. For each value of power density, a coefficient of determination (R^2) factor of around 99.5% is observed, thus highlighting the accuracy of the simulated spectra. Moreover, using equation (1), the steady-state radiative carrier lifetime τ_{rad} was extracted and shown to go from 3.52 to $1.89\,\text{ns}$ in the range of power density used in this study. A similar analysis was done for the temperature-dependent PL, and the evolution of the steady-state radiative carrier lifetime with temperature and strain was extracted. From this analysis, a minimum R^2 factor of about 98% was observed throughout the range 4-$240\,\text{K}$, and τ_{rad} was shown to increase going from $\sim 3.44\,\text{ns}$ at 4 K to $\sim 20.2\,\text{ns}$ at 240 K.

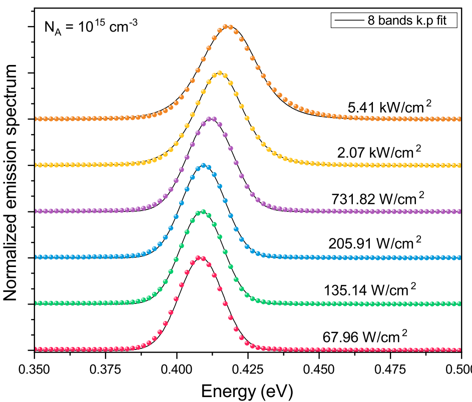

Figure 1. Power-dependent photoluminescence at T = 4 K for the -1.27% biaxially strained $Ge_{0.83}Sn_{0.17}$. The scatter points are from the measurements while the black lines are the results from the simulations

4. Conclusion

To circumvent the limitations facing the experimental studies of carrier dynamics in narrow bandgap $Ge_{1-x}Sn_x$ materials, this work demonstrates a straightforward method to obtain the carrier radiative lifetime from simple PL spectra. For a $Ge_{0.83}Sn_{0.17}$ material under an in-plane biaxial compressive strain $\varepsilon_{\parallel} = -1.3\%$, the analysis revealed a lifetime τ_{rad} in the nanoseconds range increasing from 3 to $20\,\text{ns}$ for temperatures between 10 and $240\,\text{K}$. Additionally, the introduced model also solves the restrictions that are inherent to the JDOS model resulting from the PBA and the weak-injection approximation.

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Synthesis of relaxed $Ge_{0.9}Sn_{0.1}$/Ge by nanosecond pulsed laser melting

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1. Summary

$Ge_{1-y}Sn_y$ alloys with high Sn content is a keystone for a large number of applications ranging from high performance nanoelectronics to integrated mid-infrared photonics in Si [1]. Here, we present a new approach to the fabrication of fully relaxed $Ge_{1-y}Sn_y$ layers on Ge with Sn concentration y up to 13 at. % [2]. The incorporation of Sn in Ge was obtained by sputtering of thin Sn films (<20 nm) directly on Ge wafers followed by pulsed laser melting in air. Microstructural analyses combining high-resolution transmission electron microscopy, atom probe tomography and nanobeam precession electron diffraction were performed to investigate the Sn distribution and the strain state down to the nanoscale (Fig. 1). If $y < 6$ at. %, $Ge_{1-y}Sn_y$ layers are fully substitutional and fully strained with no or very few extended defects. The formation of Sn-rich regions in correspondence of dislocations is instead observed for $y > 6$ at. %. However, outside these regions, $Ge_{1-y}Sn_y$ layers present a very homogeneous Sn distribution, full Sn substitutionality, full strain relaxation, and excellent crystalline quality. This new approach could offer, if properly optimized, an alternative to epitaxy or ion implantation to fabricate high quality $Ge_{1-y}Sn_y$ alloys, with important potential for further developments due to the ability of pulsed laser melting to perform spatially confined (both laterally and deeply) thermal processes.

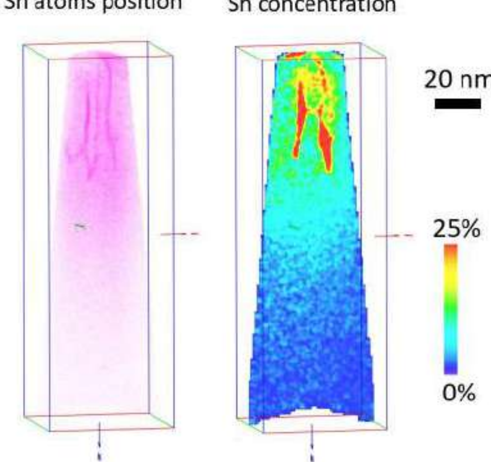

Fig. 1. (left) Atom probe 3D reconstruction of Sn atoms positions; (right) vertical slice showing the local Sn concentration.

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Strain Analysis of Ge Quantum Well on a Si_xGe_{1-x} barrier

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1. Introduction

Among all the semiconductor-based quantum technologies, silicon has been pointed out as an outstanding candidate for quantum information processing. One of the main reasons lies in the long coherence time of spins of localized electrons and efficient controllability in silicon [1]. Moreover, the present microelectronics infrastructures are performed in silicon platforms. Among the properties of these platforms stand out its scalability, low economic costs, harmless for the environment, well-known fabrication processes and it allows to apply advanced engineering techniques [2,3].

Consequently, the search of quantum materials compatible with silicon for epitaxial growth led to implement germanium (Ge) quantum well (QW) in Si structures, similar to the one depicted in Fig. 1. Another advantage of the use of Si and Ge for quantum applications came with the demonstration that an electron hole qubit can be created with both Si and Ge [4]. Ge is a semiconductor with a lattice parameter with 4% mismatch with Si and it holds a narrower indirect bandgap [5]. Such a mismatch introduces strains in Si/Ge heterostructures hindering mobility. Thus, to achieve higher mobility, scattering must be minimized by diminishing strains and interface roughness.

In this regard, one of the main challenges to achieve high mobility in Si/Ge heterostructures is to minimize the dislocation density. One route to diminish the strains is the introduction of Si_xGe_{1-x} alloy layer between the Ge virtual substrate and the Ge QW with gradual grading of Si in the Si_xGe_{1-x} film to reduce nucleation of dislocations. Another route consists in growing a virtual Ge layer between the Si substrate and the Si_xGe_{1-x} matrix. The mismatch of the lattice parameter between the virtual layer and the substrate will localize all the defects at the interface, far from the Ge QW in which the structure will be relaxed [6].

In this work, we grew a Si/Ge heterostructure embedding a Ge QW for quantum computing purposes by chemical vapor deposition (CVD). In a first step we chemically and structurally localized the Ge QW within the Si_xGe_{1-x} matrix using energy-dispersive X-ray (EDX) spectroscopy and scanning transmission electron microscopy (STEM) techniques. Both techniques will reflect the quality of the material and the roughness of interfaces. Finally, we aim to study local strain of the Ge QW by means of geometric phase analysis (GPA).

2. Experimental methods

2.1. Growth

In this study, thin film heterostructures for quantum computing purposes were grow by CVD on a (001) Si substrate as shown in Fig. 1. On a first step, a Ge virtual substrate of ~600 nm thickness was deposited on (001) Si substrate. On a second step, we grow a graded Si_xGe_{1-x} layer of 1.2 µm ending with a 300 nm barrier Si_xGe_{1-x} layer with a Si content of x = 10%. Thirdly, we grew a Ge QW with a thickness of 15 nm. Finally, a top 55 nm Si_xGe_{1-x} barrier layer with the same Si/Ge ratio of the bottom barrier was grown.

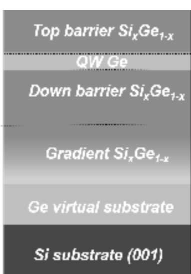

Fig. 1. Schematics of Si/Ge heterostructure.

2.2. Energy-dispersive X-ray (*EDX) spectroscopy*

EDX is a technique performed in an electron microscope in which the sample's structure can be related to its chemical composition. In this study, we have used an EDX-STEM with a spatial resolution of 3 nm, to locate and quantify Si and Ge elements in our QW and both Si_xGe_{1-x} barriers as well as the diffusion of elements at the interfaces. STEM images of the samples were performed in a Jeol JEM F200 cFEG TEM/STEM to evaluate roughness of interfaces and defects.

2.3. Geometric phase analysis (GPA)

GPA is a microscopic technique by STEM based on the signal processing of HR-TEM images and its Fourier transform. This method of local strain analysis permits the calculation and mapping of a localized area in the sample. Thus, evaluate the relaxation in the Ge QW.

3. Results and discussion

EDX analysis reveals a well-defined Ge QW embedded in both Si_xGe_{1-x} barriers. Besides, we have measured by EDX the Si/Ge ratio in the Si_xGe_{1-x} matrix. As expected, results confirm Si/Ge concentration ratio of 10/90.

In Fig. 2 (a), we display a HR-TEM image of both Si_xGe_{1-x} barriers and the embedded Ge QW. GPA performed in this area shows strain mapping in four different directions: xy rotation (Fig. 2 (a)) and ε_{xx}, ε_{xy} and ε_{yy} directions (Fig. 2 (b), (c) and (d), respectively). Tensile strain can be observed in the GPA analysis along the Ge QW and in the Si_xGe_{1-x} top barrier in the xx direction. The Si_xGe_{1-x} bottom-barrier is relaxed in the GPA calculations for all directions.

3. Conclusions

In this work, we grow Si/Ge heterostructure on a silicon substrate. Chemical analysis by EDX allowed to confirm the accurate ratios of Si/Ge stablished during the CVD growth. Moreover, EDX combined with STEM imagining confirms the presence of well-defined interfaces between Ge QW and Si_xGe_{1-x} barriers with lack of diffusion. Finally, GPA revealed tensile-relaxed strains in the xx direction along the Ge QW interfaces and in the top Si_xGe_{1-x} barrier. This study proved the high quality of our material making it suitable for integration in Si platforms for quantum computing purposes.

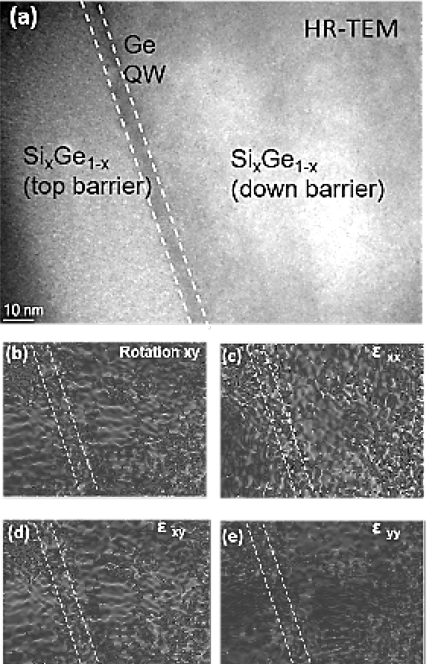

Fig. 2. (a) HR-TEM image of Ge quantum well embedded in a Si_xGe_{1-x} matrix HR-TEM and GPA mapping of the same area showing strains in the following directions: (b) rotation xy, (c) xx, (d) xy and (e) yy.

Acknowledgements

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Polarization-Induced Fano Resonances in All-Dielectric SWIR Metasurface

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1. Introduction

All-dielectric nanostructures are versatile platforms to engineer light-matter interactions and exploit a range of processes including Fano interference [1] and strong coupling [2]. Their fundamental properties support both electric dipole (ED) and strong magnetic dipole (MD) resonances, which substitute lossy ohmic currents with low-loss displacement currents. This is in contrast to plasmonic particles, where a non-negligible magnetic response can only be achieved using complex geometries [3].

It is thus highly coveted to develop low-loss resonators made entirely of dielectrics with average permittivity in the $\approx 2-14$ range. The resonant multipole interplay in all-dielectric metasurfaces can induce sharp features in light reflection and transmission spectra, including Fano resonances. Tuning these resonances mainly rely on changing the asymmetry parameter, the geometry, or the coupling distance within the unit cell of the metasurface [4].

Herein, we propose a new material system to leverage the flexibility offered by the emerging silicon-compatible GeSn semiconductors [5] to implement all-dielectric core/shell Si/GeSn base-tapered nanowire (NW)-metasurfaces. By rotating the polarization state of incident light, polarization-induced resonance (PIR) modes are observed and finely controlled with a modulation depth as high as 75%. Furthermore, by combining the narrow Fano resonance linewidth with the strong near-field confinement, we demonstrate a room-temperature optical refractive index (RI) nanosensor operating between 1.6 and $1.9\,\mu\mathrm{m}$, with a sensitivity as high as $386\,\mathrm{nm}$/RIU and a figure-of-merit (FoM) of 12. The Fano resonance spectral shift is induced by a 10^{-2} change in the properties of the surrounding environment RI.

2. Results and Discussion

2.1. Epitaxial growth of Si/GeSn based NW metasurfaces

Using a state-of-the-art pilot line for $130\,\mathrm{nm}$ SiGe BiCMOS technology, Si NW with diameters of 20-$150\,\mathrm{nm}$ (top-bottom) were fabricated from a $300\,\mathrm{mm}$ Si(100) wafer by a multi-step procedure, including a anisotropic Ar:BCl_3:Cl_2-based reactive ion etching (RIE) process [6]. The Si NWs sample was then cleaned in an HF-based solution prior to loading in the chemical vapor deposition (CVD) reactor. The GeSn shell was grown at $300\,^{\circ}\mathrm{C}$ using ultra-pure H_2 carrier gas, and 10 % monogermane (GeH_4) and tin-tetrachloride ($SnCl_4$) precursors. A constant precursor supply with a GeH_4/$SnCl_4$ ratio of $\sim$ 1700 was provided during the GeSn growth, hence with the same parameters as in the reference $Ge_{0.90}Sn_{0.10}$ thin film layers grown on a Ge on Si substrate [7]. The pitch was varied from $500\,\mathrm{nm}$ to $2\,\mu\mathrm{m}$. A scanning electron microscopy (SEM) image of the metasurface and the corresponding EELS images of the Si, Ge, and Sn elements acquired using TEM are displayed in Fig.1a-b.

2.2. Optical characterization of GeSn based NWs

Polarization-resolved reflectance was undertaken to study the optical response of these metasurfaces [8], [9]. Systematic angular- and polarization-resolved reflectance spectroscopy showed the effect of the $Ge_{0.9}Sn_{0.1}$ shell on mode resonance of the different arrays, as highlighted in Fig.1c. Finite difference time domain (FDTD) simulation and Mueller Matrix ellipsometry measurement unveil the anisotropic response in the Si/$Ge_{0.9}Sn_{0.1}$ NW array, with a polarization-dependent modal splitting originating from the interplay between the magnetic and electric dipole resonances. To exploit the NW metasurface in sensing application, a

refractive index sensing device was developed where the sensitivity was measured for different RI and at different polarization angles (0° and 90°). The Fano resonance contributes greatly the the sensitivity enhancement, as demonstrated in Fig.1d.

3. Conclusion

In summary, this work highlights the fabrication and the optical characterization of a core/shell Si/GeSn nanowire structures. Polarization-resolved reflectance of Si/GeSn core/shell NWs revealed direct interplay between the surface diffracted modes and the resonant modes, which permitted the fabrication of a RI nanosensor with a sensitivity of $386\,\mathrm{nm/RIU}$ at a polarization angle of $90°$.

Acknowledgment

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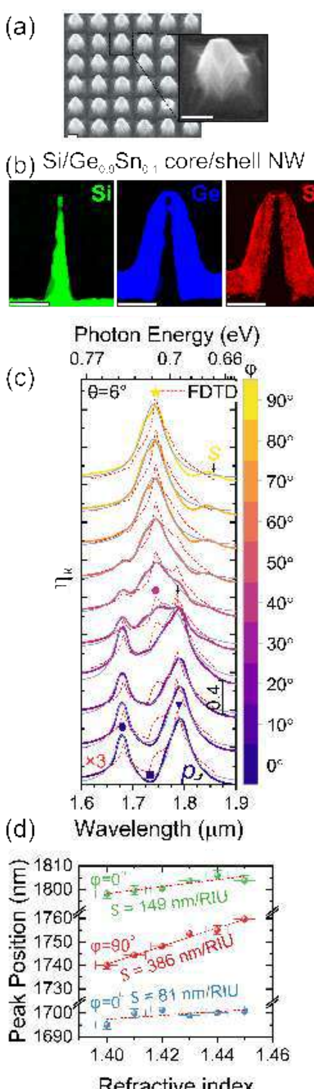

Figure 1. (a) SEM image of the top-down etched Si/$Ge_{0.9}Sn_{0.1}$ core/shell NW metasurface where the zoom in map highlights the tapered base. (b) The associated individual EELS maps for Si, Ge, and Sn atoms are also shown. The scale bar in all images is fixed to $200\,\mathrm{nm}$. (c) Polarization-dependent reflectance ratio characterization at a fixed angle of incidence of 6°. The polarization is rotated from *s*-to *p*-state with a 10° step. The simulated FDTD specular reflectance ratio at each polarization is also overlaid in red-dashed traces. (d) RI sensing. spectral shift of the resonances vs. RI of the surrounding solutions, at different angle of polarization.

The layer transfer of Ge-lattice-matched SiGeSn epitaxial films

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1. Introduction

Recently, the interest in SiGeSn alloy has significantly increased due to its tunable band gap and higher carrier mobilities as compared to Si and Ge. The ternary SiGeSn alloy possesses two compositional degrees of freedom to achieve the desirable band gap and alignment [1]. Therefore, the energy band engineering using SiGeSn heterostructures can be conducted for group IV optoelectronics. Most SiGeSn-based devices were fabricated with SiGeSn alloys grown on bulk Ge or Si. Meanwhile, the SiGeSn-on-insulator (SiGeSnOI) structure is an attractive platform for group IV optoelectric integrated circuits [2-4]. Therefore, the study of SiGeSn layer transfer accelerates for its potential application in 3D integration on Si CMOS and flexible optoelectronics. The Ge-lattice-matched SiGeSn alloy offers the high possibility of realizing the superior crystalline and reliable SiGeSnOI platform as starting materials to fabricate the Ge-based optoelectric devices. However, there are hardly any reports on Ge-lattice-matched SiGeSnOI structure, and its device performance is limited. In this work, we demonstrated the layer transfer of the SiGeSn films epitaxially grown on Ge. The SiGeSn MSM photodetector was then fabricated on the SiGeSnOI platform, exhibiting photosensitivity at the wavelength of 1550 nm.

2. Experiments and Discussion

2.1. Growth of SiGeSn alloy

The Ge-lattice-matched SiGeSn epitaxial films (~50 nm thick) are grown by UHV-MBE on Ge (001) substrate. Fig. 1 shows XRD-2DRSM around the Ge $\bar{2}\bar{2}4$ reciprocal lattice point of SiGeSn film on Ge substrate. Since the SiGeSn peak with a clear fringe pattern overlapped with the Ge peak perfectly, we confirmed the high-quality epitaxial growth of the Ge-lattice-matched SiGeSn layer on the Ge (001) substrate. Fig. 2 (a) shows the Raman spectra of the SiGeSn layer on the Ge substrate. The distinct Raman peaks corresponding to Si-Si, Si-Ge, and Ge-Ge modes from SiGeSn alloy were observed. The sharp peak near 301 cm^{-1} is attributed to the Ge crystalline under the thin SiGeSn film. By combining XRD-2DRSM and Raman data, the composition of the SiGeSn film was evaluated to be $Si_{27.8}Ge_{64.2}Sn_8$. The direct and indirect bandgap energy of $Si_{27.8}Ge_{64.2}Sn_8$ alloy are also extracted to be 1.21 eV and 0.778 eV, respectively [5], offering type-I band alignment to Ge [6]. RMS roughness of the SiGeSn surface is 0.3 nm, which is low enough for direct bonding afterward.

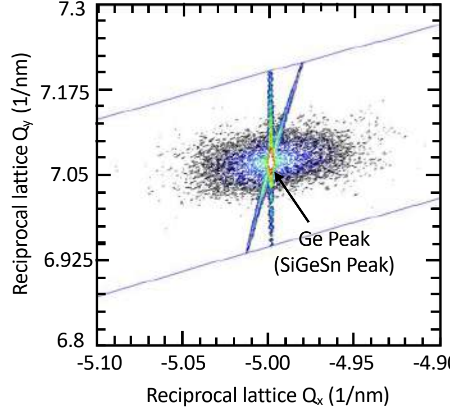

Fig. 1. X-ray diffraction–2-dimensional reciprocal space mapping (XRD–2DRSM) around the Ge $\bar{2}\bar{2}4$ reciprocal lattice point of the lattice-matched SiGeSn epitaxial layer on the Ge (001) substrate.

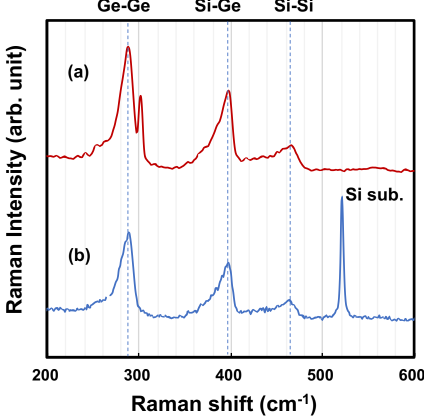

Fig. 2. Raman spectra of Ge-lattice-matched SiGeSn layer grown on Ge substrate (a) and transferred on Si substrate (b).

2.2. Layer transfer of SiGeSn films

SiGeSn/Ge heterostructure was directly bonded to the SiO_2(10 nm)/Si substrate with the wet activation treatment at room temperature. The initial bonding occurred spontaneously, and post-bonding-annealing was carried out at 200 ˚C to further enhance the bond strength [7]. The bonding strength is sufficiently strong to prevent detachment during the SiGeSnOI fabrication. Then, the high-speed and uniform wet etching of donor Ge substrate (450 μm) was carried out by $H_3PO_4/H_2O_2/H_2O$ (2/2/1) solution with the etching rate of 368 nm/min at room temperature [8]. After the thickness of the Ge substrate was reduced to ~10 μm, the residual Ge was etched by H_2O_2 solution until SiGeSn layer exposure. While the H_2O_2 solution etches Ge with the etching rate of 15.3 nm/min, SiGeSn with high Si composition is not etched due to the insoluble SiGeSn oxide formation in the H_2O_2 solution, resulting in significantly high etching selectivity between SiGeSn and Ge. It should be noted that the low-temperature layer transfer process is essential for demonstrating reliable layer transfer because the process is almost free of the issue of thermal expansion mismatch in different materials.

SiGeSn material quality can be well maintained after the layer transfer, as revealed by Raman spectra before and after the layer transfer (Fig. 2 (a) and (b)). The peak positions of Si-Si, Si-Ge, and Ge-Ge modes from SiGeSn layer match entirely before and after the layer transfer. Strong Si Raman peak around 520 cm^{-1} after the layer transfer indicates the formation of SiGeSn layer on the Si substrate.

2.3. SiGeSnOI MSM photodetector

Using the SiGeSnOI platform, we demonstrated SiGeSn MSM photodetectors. After the mesa isolation of SiGeSn layer, Ni/Au pad metal was formed on the SiGeSn layer by a lift-off process. Fig. 3 shows the I-V characteristics of the SiGeSnOI MSM photodetector in the dark and under illumination at 1550 nm. The sensing area is 100 × 100 μm^2, and the incident power is 34.6 μW with a light spot diameter of 50 μm as shown in the inset. We observed clear photoresponse from the SiGeSn MSM photodetector. The photocurrent was extracted by the difference between the current in the dark and under illumination. Responsivity is a key parameter for evaluating the performance of photodetectors, which is given by the following equation.

$$\text{Responsivity (R)} = \frac{I_{illumnation} - I_{dark}}{P_{in}}$$

The Responsivity increase with increasing bias voltage and the maximum responsivity of 9.03 mA/W achieves at 5 V. We verify the distinct photoresponse of SiGeSn layer at 1550 nm, which is close to the bandgap of $Si_{27.8}Ge_{64.2}Sn_8$. These results suggest the high-quality layer transfer of the SiGeSnOI epitaxial films, which is applicable for Ge-based optoelectric devices.

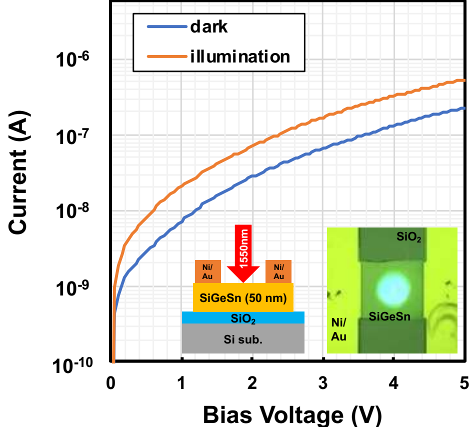

Fig. 3. I-V characteristics of SiGeSnOI MSM photodetector in the dark and under illumination at a wavelength of 1550 nm. The incident power is 34.6 μW. The inset is a top view of SiGeSnOI MSM photodetector.

3. Conclusion

We demonstrated high-quality layer transfer of Ge-lattice-matched SiGeSn films epitaxially grown on Ge substrate utilizing the direct bonding and the Ge substrate removal at low temperature. To remove the Ge substrate, a two-step etching was performed by $H_3PO_4/H_2O_2/H_2O$ solution with a high-speed Ge etching followed by H_2O_2 solution with extremely high etch selectivity over SiGeSn. Raman measurements reveal SiGeSn films transferred on Si substrate maintaining high crystallinity. We also report the first experimental demonstration of SiGeSn MSM photodetector on a novel SiGeSnOI platform, which is promising for future 3D optoelectronic integration.

Acknowledgements

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Post growth thermal treatments of Silicon-Germanium-Tin-on-insulator alloys

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1. Introduction

$Si_{1-x-y}Ge_xSn_y$ alloys are promising materials for future applications in opto- and nanoelectronics [1, 2]. These alloys enable effective band gap engineering, a broad adjustability of the lattice parameter, exhibit much higher carrier mobility than pure Si and are compatible with the CMOS technology. Unfortunately, the equilibrium solid solubility of Sn in $Si_{1-x}Ge_x$ is less than 1% [3] and pseudomorphic growth of $Si_{1-x-y}Ge_xSn_y$ on Ge or Si can cause in-plane compressive strain in the grown layer. This degrades the superior properties of the alloys. Therefore, post-growth strain engineering using ultrafast non-equilibrium thermal treatments to improve the layer quality is needed. In this contribution, we discuss the influence of the millisecond flash lamp annealing (FLA) and nanosecond pulsed laser annealing (PLA) on $Si_{1-x-y}Ge_xSn_y$ alloys on insulator.

2. Material fabrication and investigation methods

20 nm thick $Ge_{0.94}Sn_{0.06}$ and $Si_{0.14}Ge_{0.80}Sn_{0.06}$ alloys are directly grown by MBE on commercial silicon-on-insulator (SOI) wafers with a 20 nm thick Si layer and treated by 3 ms FLA or 28 ns PLA. The material is analysed by micro-Raman spectroscopy, Rutherford backscattering spectrometry (RBS) and X-ray diffraction (XRD) before and after the thermal treatments.

3. Results and Discussion

Before annealing the lattice of the $Ge_{0.94}Sn_{0.06}$ and $Si_{0.14}Ge_{0.80}Sn_{0.06}$ layers are in-plane compressive strained and out-of-plane elongated, due to the pseudomorphic growth on Si. This is confirmed by high resolution x-ray diffraction (HR-XRD) of the symmetrical (004) reflection and reciprocal space mapping (RSM) of the asymmetrical (-2-24) reflections.

The HR-XRD results in *Fig. 1* show a significantly higher intensity, relaxation of the out-of-plane lattice parameter and a reduced full width at half maximum (FWHM) of the GeSn and SiGeSn (004) reflexions after PLA. On the contrary, after f-FLA the reflexions are almost unaffected compared to the as-grown state.

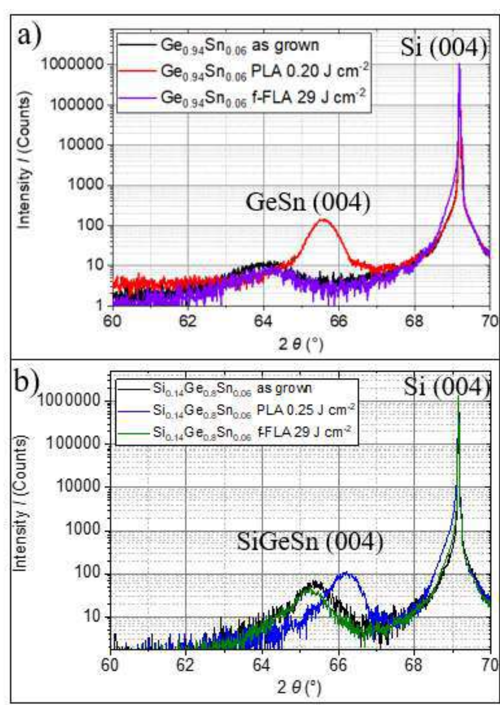

Fig. 1. HR-XRD of the symmetrical (004) reflections before and after post growth thermal treatment with PLA and front side FLA of the 20 nm thick $Ge_{0.94}Sn_{0.06}$ a), $Si_{0.14}Ge_{0.80}Sn_{0.06}$ b) layer and the Si Substrate.

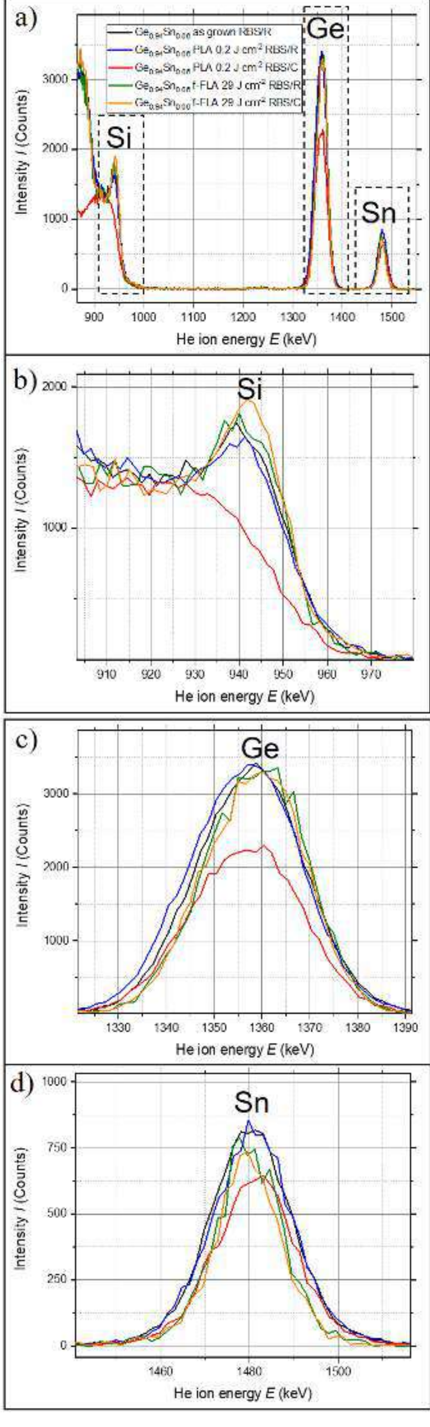

Fig. 2 RBS R/C results of the $Ge_{0.94}Sn_{0.06}$ film after the direct growth on Si, PLA with 0.2 Jcm^{-2} and f-FLA with 29 J cm^{-2} a). Additionally, the enlarged windows from a) shows the Si contribution of the thin Si layer below $Ge_{0.94}Sn_{0.06}$ b), the Ge contribution of $Ge_{0.94}Sn_{0.06}$ c) and the Sn contribution of $Ge_{0.94}Sn_{0.06}$ d).

The RBS random (RBS/R) results in Fig. 2 indicates that the selected PLA and FLA parameter does not cause a Si, Ge or Sn redistribution, since the RBS/R spectra are almost identical. The aligned RBS channeling (RBS/C) measurements show a reduced channeling yield for the Si, Ge and Sn contributions after PLA. On the other hand, no significant channeling could be obtained for the as-grown state and after f-FLA.

4. Conclusion

After annealing, the material is single-crystalline with much better crystallinity than the as-grown layer and the compressive strain is partially released. PLA performed for 28 ns and energy densities between 0.2 and 0.25 J cm^{-2} significantly improves the quality of thin $Si_{1-x-y}Ge_xSn_y$ films on insulator. The presented approach can be used as a technique to improve the performance of vertical thin film devices like junction-less nanowire transistors (JNT) or reconfigurable field-effect transistors (RFET).

Acknowledgements

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Fabrication of Si/Ge microbridges based on Ge-on-Si (110) and effect of bridge length

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1. Introduction

Ge has emerged as one of promising candidates for light sources in Si photonics [1,2] since introduction of tensile strain into Ge can enhance the direct transition probability via reduction of the Γ-valley, resulting in an increase in luminescence efficiency. By epitaxial growth of the Ge directly on the Si (Ge-on-Si), the tensile strain can be induced in the Ge layer due to the difference in thermal expansion coefficients between Ge and Si. So as to increase the strain amount further, fabrication of Ge microbridge (MB) structure has been intensively researched so far. It has been shown that the uniaxial tensile strain can be largely enhanced in the MB, offering further improved luminescence efficiency [3,4]. It was predicted that band shift of the Γ-valley via the tensile strain is expected to be the largest for <111> directional uniaxial strain [5]. In common, Ge layers are formed on a Si(100) substrate, whereas the Ge MB cannot be defined along <111> direction. In this study, therefore, we fabricate strained Ge MB along the <111> direction based on a Si(110) substrate.

With the increase in the tensile strain and resultant large Γ-valley reduction, however, the luminescence wavelength from the strained Ge becomes longer beyond telecommunication wavelength bands. Therefore, controlling of the light emission wavelength, especially to shorter wavelength region, is strongly demanded. As SiGe has larger bandgap than Ge, introduction of SiGe/Ge heterostructures into MBs allow us to control the emission wavelength. For this purpose, we attempt to re-grow SiGe layers after fabricating Ge MBs and observe blue-shifted PL emissions.

2. Experimental procedures

Ge layers were directly grown on a Si (110) wafers by solid-source molecular beam epitaxy (MBE) by a two-step growth method. First, a low-temperature (LT) Ge layer (Tg = 350°C, 40 nm) and a high-temperature (HT) Ge layer (Tg = 550°C, 500 nm) were successively grown and subsequently annealed at 800°C for 10 min. to improve the crystallinity. Then, patterning of the MB structures as shown in Fig. 1 was performed by standard photolithography process. The structure consists of the microbridge with the width and length of 5 and 40-130 μm and the pad areas with the width and length of 20 μm. Next, the grown Ge and the underlying Si substrate were etched down by reactive ion etching (RIE). After the etching, the Si underneath the MB was removed to form freestanding structures by selective etching of the Si with KOH.

After the fabrication of the Ge MB structure, the strained SiGe regrowth on the MB was carried out. 50 nm thick Ge buffer and 300 nm thick SiGe layers were successively overgrown on the Ge layer at 350 °C.

Micro-photoluminescence (μ-PL) spectroscopy measurements were performed at room temperature.

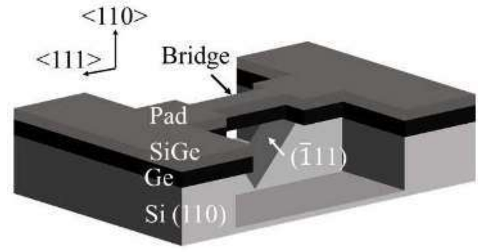
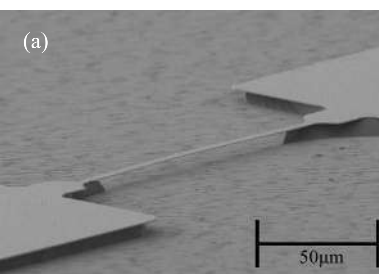
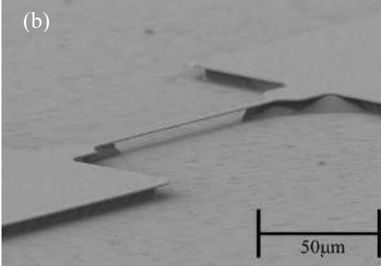


Fig. 1 Schematics of SiGe/Ge microbridges fabricated in this study.

3. Results and discussions

Figures 2 show SEM images of the fabricated SiGe/Ge MBs. Figure 2(a) shows MB with the bridge length of 130 μm, and it is clearly seen that the SiGe/Ge bridge is freestanding in a wide area owing to complete Si etching under Ge. By contrast, for MB with the bridge length of 40 μm, as shown in Fig. 2 (c), a SiGe/Ge freestanding part is limited in a narrow area due to insufficient Si etching. Very low etching rate along <111> direction is considered to be responsible for this.





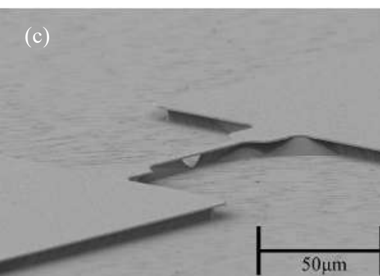


Fig. 2 SEM images of the SiGe/Ge MB.
Bridge length (a)130μm. (b)70μm. (c)40μm.

Figure 3 shows the room temperature PL spectra for the SiGe/Ge MBs with various bridge lengths. The PL intensity increases as the bridge length increases. Comparing the MBs with length of 40 and 70 μm, the PL peak is seen to red-shift with the bridge length increases. This is attributable to the strain increase owing to sufficient under etching as shown in SEM. Remarkable changes in the PL spectrum are observed for the MB with 130 μm bridge length. We observe resonant peaks around 1800 ~ 2000 nm and strong peak around 1600 nm coming from SiGe. Additional strain increase with increased freestanding length is considered to play an important role for this changes. While reasons for the SiGe peak appearance with the length are still under investigation, we can say that sufficiently long freestanding SiGe/Ge MBs can offer strong light emissions in wide wavelength range.

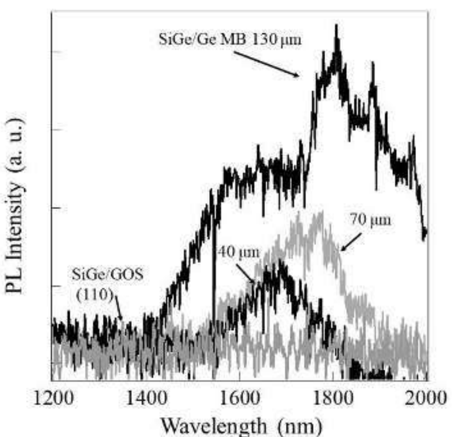


Fig. 3 Room temperature PL spectra for SiGe/Ge microbridges (MB).

4. Conclusions

In this study, uniaxially tensile-strained Ge microbridges along <111> direction were fabricated based on the strained Ge epitaxially grown on a Si (110) substrate (Ge-on-Si). The strained SiGe layer was re-grown on the fabricated Ge MB and we obtained strong PL from the overgrown SiGe layer, wavelength of which was blue-shifted due to the wider bandgap of SiGe. It has been also shown that the longer bridge provides the stronger PL owing to sufficient under etching.

Acknowledgements

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Processing of the stacked n-Si channel over p-Si channel for fabrication of CFETs

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Abstract

By vertically stacking PMOS and NMOS, the CMOS device area can be effectively reduced, and this device architecture can effectively mitigate the scaling challenges that sub-2nm technology nodes are facing. In this project, a device process technology of combing Si/Ge/Si multilayer epitaxy and selective etching was proposed. In this process flow, following defining and etching of device active region, the H_2O_2 solution was used to selectively etch the Ge interlayer between top p-Si layer and bottom n-Si layer. Because the etching selectivity of Ge over Si in H_2O_2 solution is almost near infinity, the final structure of pSi channel stacking over n-Si channel is perfect.

Index Terms—Si/Ge/Si multilayer epitaxy, Ge/Si selective etching, stacking p- and n-channel CMOSFETs

1. Introduction

It is generally considered that the conventional lateral positioning of devices such as nanowire or nanosheets channel FETs will face a big challenge of device area shrinking when the technology node reaches beyond 2nm. So innovative vertical stacking structure such as vertical nanowire and nanosheet will be most likely utilized beyond 2nm instead of conventional structures of laterally positioning channels. In this project, we proposed to fabricate 3D-stacked complementary FETs (CFETs) on the cost effective traditional Si substrates [1-5]. The epitaxial n-Si/Ge/p-Si stack structures were selectively etched by using H_2O_2 solution to form both n-Si and p-Si nanowire
channels. The fabrication process exhibits the advantages of (1) isotropic etching without ion bombardment and extremely high Ge/Si selective etching rate ratio; (2) low cost, low process complexity, and in line with standard process and mass production;
(3) both n-Si and p-Si nanowire channel fabrication. These advanced designs are expected to improve the gate controllability and device characteristics. As the semiconductor-related field gradually enter the physics limitation, Ge/Si epitaxial multi-layer combined with selective etching is considered as the most likely implementation of the vertically stacked CFET. This will be able to achieve low complexity, high performance, high packing density and so on. In this work, we successfully developed the stacked p-Si and n-Si channels by using Si/Ge/Si epitaxial layers and high selective isotropic etching technologies. Because the etching selectivity of Ge over Si in H2O2 solution is almost near infinity, the final structure of p-Si channel stacking over n-Si channel is perfect. The achieved vertically stacked Si channels can be easily used to fabrication of so-called CFET devices.

2. Stacked Single-Crystalline Si/Ge/Si structure

The whole process flow was shown in Fig. 1. For epitaxial growth of Si/Ge/Si multilayers structure, a full 8” SOI wafer was first cleaned using RCA standard method. Then the wafer was dipped in H_2O:HF=50:1 for 20sec to remove Si native oxide on the surface. After that, wafer was immediately loaded into an ASM Epison 2000+ epitaxial reactor for epitaxy. The SiH4 and GeH_4 (10% in H_2) gases were used as Si layer and Ge layer growth respectively. In the whole growth process, hydrogen gas with flow rate of 15 SLM was used as carrier gas in the chamber, and growth pressure was kept at 20torr all the way. The GeH4 and SiH4 flow rates were set to 250sccm and 50sccm respectively. Large lattice mismatch between Ge/Si will prevent Ge/Si epitaxial layers from growing at a 2D mode. In order to avoid island growth, Ge epitaxy temperature was kept at 400℃ and Si one was kept under 500℃. In addition, the epitaxy process should not be interrupted during the period of switching from Ge to Si epitaxy and vice versa. For selective etching of Ge interlayer between bottom p-Si and top n-Si layers, it is very easy in our proposed methods. Just put the sample after fin structure formation (Fig. 1(b)) into chemical solution of H_2O_2:H_2O=1:10 for 5~10min at room temperature.

The Ge can be completely etched away. Here, the Ge etching rate is around 20nm/min. However, the H_2O_2 solution has no any etching effect on Si layers. Fig. 1 (c) The Ge interlayer between top n-Si and bottom p-Si was selectively etched away by using H2O2 solution and Fig. 1 (d) the expected final device structure. Fig.2 shows cross sectional SEM images for the formation of structures at various steps.

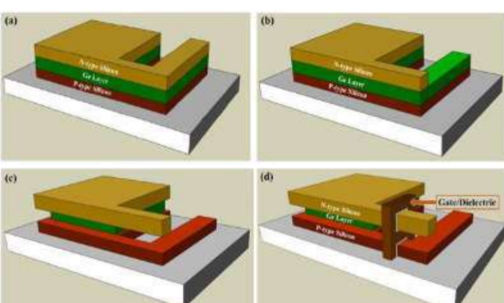

Fig. 1. The process flow for formation of stacked n-Si channel over p-Si channel.

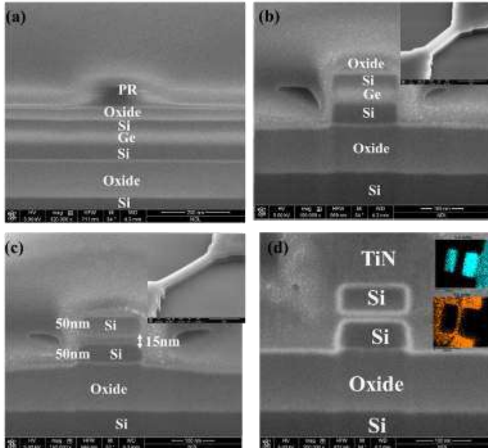

Fig. 2 The SEM images at various steps in the process flow for formation of stacked n-Si channel and p-Si channel.(a) As grown p-Si/Ge/n-Si (b) Fin formation by dry-etching(c) After Ge was partially etched (d) Stacked and separated p- and n-Si channels

3. Process Flow of CFET

3D schematic illustration of the CFET fabrication is shown in Fig. 3, including active region formation (Fig. 3(a)), top Si anisotropic dry etching to exposed bottom Si source region reserved for p-FET and top Si channel release by removing Ge sacrificial layer using selective wet etching (Fig. 3(b)), gate stack deposition and gate formation (Fig. 3(c)), inter-layer oxide deposition (Fig. 3(d)), contact and metallization for electrodes formation (Fig. 3(e),(f)). The CFET device architecture inherently forming an invertor and electrodes for invertor characterization are also indicated in Fig. 4.

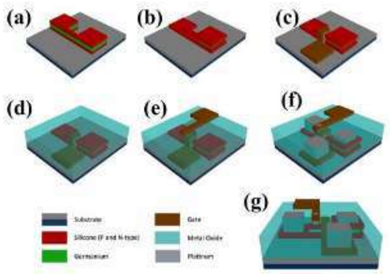

Fig. 3 Schematics of the key process in the fabrication of CFET. (a) active region definition (b) top n-Si etching at VDD region and Ge selective wet etching (c) gate formation (d) ILD deposition (e)&(f) gate and S/D contact and electrodes formation (g) different view of (f).

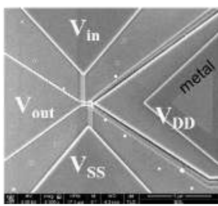

Fig. 4 SEM image of the complete CFET device consisting of top Si NS n-NOSFET and bottom Fin p-MOSFET. Electrodes for invertor characterization also indicate.

4. Characteristics of the CFET

Functional and symmetric n-MOSFET and p-MOSFET transfer characteristics in the CFET device architecture are successfully demonstrated. Both n-/p-MOSFETs show low subthreshold swing and high Ion/Ioff ratio of about ~106 (Fig. 5). Furthermore, the CFET device architecture (Fig. 5) inherently forming an invertor. Fig. 10 indicates the invertor consisting of the stacked n-/p-MOSFETs has a high gain of 59 under Vcc biasing at 1V. Table I benchmarks results of various stacked n-/p-MOSFET devices.

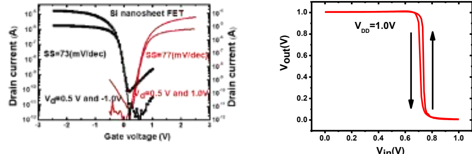

Fig. 5 ID-VG transfer characteristics of n-/p-MOSFETs and VTC of invertor in CFET.

5. Conclusions

The CFET with stacked single crystalline channels shows high potential for realization of compact logic circuits for future device technology nodes.

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Revealing very low thermal conductivity of germanium tin epilayers at room-temperature

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1. Introduction

Thermoelectricity is the direct conversion of heat into electricity or electricity into heat via two related mechanisms, the Seebeck effect and the Peltier effect. The performance of a thermoelectric material is characterized by a dimensionless quantity ZT, known as the figure of merit, and can be expressed as

$$ZT = \frac{S^2}{(k_e + k_l)}\sigma T \quad (1)$$

It is clear to see that low thermal conductivity ($k = k_e + k_l$), high Seebeck coefficient (S) and electrical conductivity (σ) of a material are essential for its application in thermoelectric. The electronic component of the thermal conductivity, k_e is a function of the heat carried by the charge carriers, while k_l is a measure of heat transferred through lattice vibration. The latter could be altered to supress k_l, to enhance the performance (ZT) of TE material toward addressing the poor efficiency of the modern thermoelectric devices operating around room-temperature. Although, the thermal conductivity of elementary materials in group IV semiconductors, like Si, Ge, C or Sn, [1]are high at around room-temperature, comparing to the most efficient thermoelectric (TE) material $Bi_{0.7}Sb_{0.3}Te$ [2], they are abundant, non-toxic, CMOS compatible and low cost. Alloying any of the group IV semiconductors is expected to reduce their thermal conductivity due to reduction of its k_l component. This study research thermal conductivity of relaxed $Ge_{1-x}Sn_x$ binary alloy epilayers with Sn content up to 9%.

2. Experiment

The intentionally relaxed $Ge_{1-x}Sn_x$ layers up to ~500 nm thick were epitaxially grown on 100 mm diameter Si (001) wafers via undoped relaxed ~600 nm thick Ge buffer layer in a reduced pressure chemical vapour deposition (RP-CVD) system [3, 4]. A schematic cross-section of the samples is shown in the inset of **Error! Reference source not found.**Fig. 1. Each epilayer thicknesses of the $Ge_{1-x}Sn_x$/Ge/Si (001) heterostructures was obtained via analysis of XTEM images. Degree of relaxation and Sn content, which was varied up to 9%, in each $Ge_{1-x}Sn_x$ epilayer were obtained by the analysis of HR-XRD data. The $Ge_{1-x}Sn_x$ epilayers exhibits over 80% relaxation. Thermal conductivity of the heterostructures and the individual $Ge_{1-x}Sn_x$ epilayers were obtained with the help of Raman spectroscopy at a relatively low non-heating laser power density of 25 kW/cm^2, using radial Gaussian distribution model as contained in the textbook of conduction of heat in solids [5]. A typical Raman spectrum of $Ge_{0.91}Sn_{0.09}$/Ge/Si heterostructure is shown in Fig. 1. Due to relatively low Sn content in the alloy, the Ge-Ge mode peak from the $Ge_{1-x}Sn_x$ epilayer in the Raman spectrum of each sample is the strongest. Therefore, it was used for measurements of thermal conductivity. To accurately measure the thermal conductivity of the $Ge_{1-x}Sn_x$ epilayer a series of suspended microwires, shown in Fig. 2, were fabricated. Dimensions of the microwires were measured with the SEM. Thermal isolation of epilayer from multi-layered heterostructure for subsequent thermal conductivity measurements is essential to eliminate any parasitic thermal effect from other layers and the substrate on the measurement.

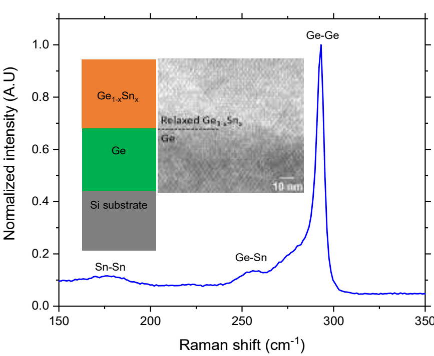

Fig. 1. Raman spectrum at 293 K of $Ge_{0.91}Sn_{0.09}$/Ge/Si heterostructure, showing Ge-Ge, Ge-Sn and Sn-Sn vibration modes at 297 cm^{-1}, 256 cm^{-1} and 176 cm^{-1}, respectively. The inset shows the cross-section schematics of heterostructure (left) and a HR-TEM image of the $Ge_{0.91}Sn_{0.09}$/Ge interface region (right).

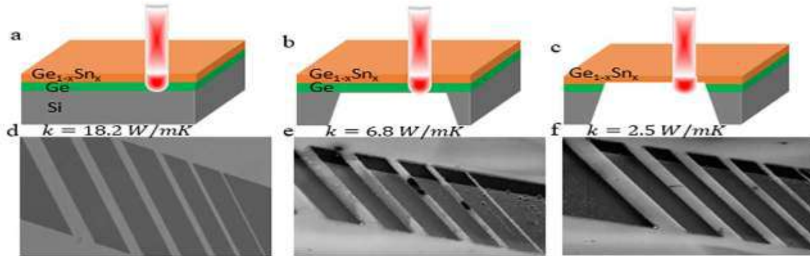

Fig. 2. 3D schematics of the characterised structures and their corresponding SEM image of patterned $Ge_{1-x}Sn_x$ /Ge/Si heterostructure (a & d), suspended $Ge_{1-x}Sn_x$ /Ge (b & e) and suspended $Ge_{1-x}Sn_x$ (c & f) microwires with measured thermal conductivities obtained from the $Ge_{0.91}Sn_{0.09}$ at room temperature.

3. Results and discussion

Fig. 3 summarises thermal conductivity at 293 K as a function of Sn content in the $Ge_{1-x}Sn_x$ alloy obtained in this work and available from literature. High thermal conductivity of 23.5 W/mK measured from relaxed $Ge_{0.91}Sn_{0.09}$/Ge/microwire was reduced to 2.5 W/mK in suspended relaxed $Ge_{0.91}Sn_{0.09}$ epilayer by our approach of thermal isolation. This value is ~7 times lower (see Fig. 3), demonstrating the elimination of the thermal loss impact on thermal conductivity via the Ge buffer layer and the Si substrate, whose thermal conductivities at 293 K are 58 and 130 W/mK respectively [1].

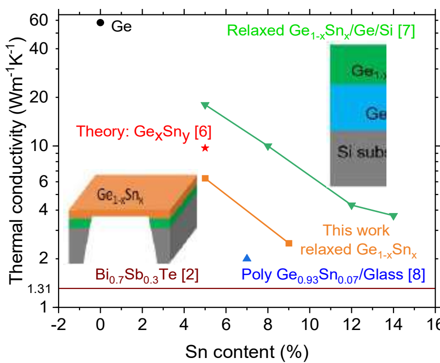

Fig. 3. Summary result of Sn concentration dependent thermal conductivity of a single layer $Ge_{1-x}Sn_x$ material compared to reference data of Ge, the most efficient TE material, $Bi_{0.7}Sb_{0.3}Te$ (brown), recent report on $Ge_{1-x}Sn_x$ theoretical data (red) [6], relaxed bulk (green) [7] and polycrystalline $Ge_{0.93}Sn_{0.07}$ material (blue) [8]. The inset showing the schematic of our suspended single layer $Ge_{1-x}Sn_x$ microstructure.

In comparison to thermal conductivity of Ge, Sn incorporation into Ge lattice, results in lower thermal conductivity of $Ge_{1-x}Sn_x$ alloy due to increase in-plane lattice constant of relaxed alloy and additional disorder of a binary alloy. Therefore, in our experiment, we vary only k_l component of the thermal conductivity, because all epilayers are undoped. As expected, the thermal conductivity in $Ge_{1-x}Sn_x$ reduces with increasing Sn content from 5 to 9%, as shown in Fig. 3. Similar behaviour was reported by *Spirito et al* [7] . However, thermal conductivity of the same relaxed $Ge_{1-x}Sn_x$ epilayers measured in our experiment is by ~3 times lower than reported modelling by *Spirito et al* [7]. It is explained by absence of heat loss in our suspended $Ge_{1-x}Sn_x$ epilayers. Also observed, our thermal conductivity in $Ge_{1-x}Sn_x$ alloy with 5% Sn content is by ~1/3 lower than reported theoretical work of *Khatami and Aksamija* [6].

4. Conclusions

In conclusions, we reveal very low thermal conductivity at room-temperature of monocrystalline $Ge_{1-x}Sn_x$ alloy epilayers with Sn content up to 9%. It decreases from 58 W $m^{-1}K^{-1}$ in Ge to ~6.3 and 2.5 W $m^{-1}K^{-1}$ in $Ge_{1-x}Sn_x$ with 5 and 9%, respectively. The lowest thermal conductivity is just 2 times higher than 1.3 W $m^{-1}K^{-1}$ in the state-of-the-art thermoelectric material ($Bi_{0.7}Se_{0.3}Te$). As a result, $Ge_{1-x}Sn_x$ shows enormous potential for applications in thermoelectric at around room-temperature and would be used to manufacture TE devices at very low cost and mass volumes.

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Study and reduction of dislocation densities in $Si_{1-x}Ge_x$ virtual substrates for quantum computing applications

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Strained silicon (Si) and germanium (Ge) can be used to confine single electron and hole spins in quantum dots, both excellent candidates for qubits due the availability of isotopes with zero nuclear spins resulting in long coherence times, and the compatibility of the materials with the semiconducting industry. To grow strained Si and Ge one commonly uses a strain relaxed $Si_{1-x}Ge_x$ virtual substrate on top of a Si (001) substrate. However, the relaxation of the VS is achieved by the formation of a misfit dislocation network, which terminates with threading dislocations leading to typical threading dislocation densities between $1x10^5$ and $1x10^7$ cm^{-2} [1]. Both types of dislocations are associated with local strain fluctuations and therefore uncontrollable potential fluctuations in the strained silicon or germanium layer, which can limit qubit performance [2]. Therefore it is crucial to explore techniques to reduce dislocation densities, while still obtaining full relaxation.

An interesting method to reduce dislocation densities is by providing a reservoir of pre-existing dislocations on the edge of the wafer by first growing a SiGe layer on the backside of the Si substrate prior to the VS growth [3]. Using this technique, we managed to reduce the threading dislocation density by an order of magnitude in $Si_{0.93}Ge_{0.07}$. This was done by growing a ~1μm of $Si_{0.75}Ge_{0.25}$ on the backside of the wafer in a reduced pressure chemical vapour deposition tool (Epsilon 2000). We then grow a ~1 μm of $Si_{0.93}Ge_{0.07}$ on the frontside after flipping the wafer by hand and count threading dislocations by *in-situ* preferential HCl etching [4].

As a next step we are exploring possibilities to obtain similar results for higher Ge concentrations. These include using a linear grading scheme and the use of a mask to grow $Si_{0.75}Ge_{0.25}$ on front edge of the wafer directly. Finally, we want to understand the influences of threading dislocation densities on transport properties measured from Hall bar transistors as well as properties relevant for qubits, such as charge noise. This will provide us with key insights into the influence of dislocations from the VS on qubit performance.

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Towards anisotropically strained in-plane Ge nanowires for quantum transport experiments

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1. Introduction

Developing scalable qubits has been a major obstacle in the development of practical quantum computers. Two major candidate qubit types are spin qubits and topological qubits. Recently, interest is growing in strained Germanium as a quantum material [1]. While in its unstrained form, it displays low g-factors and SOI, anisotropic strain changes this drastically. This can be realized by straining the Ge using epitaxial Silicon. A ideal platform for this are Ge nanowires with Silicon shells. These display a so called direct Rashba spin orbit interaction, which is tunable via an external electric field [2]. This tunability not only enables very strong SOIs, but also enables schemes where the interaction with the environment is turned on and off via a spin orbit switch.

These properties have been experimentally verified, but only using out-of-plane VLS grown nanowires [3]. These are not scalable and limit the complexity of the devices to single nanowires. Therefore, in this work, in-plane Ge nanowires are grown via metalorganic vapor phase epitaxy (MOVPE) and via molecular beam epitaxy (MBE) using selective area growth (SAG).

2. MOVPE grown Ge/Si Core shell nanowires

The nanowires are shown in figures shown in Figure 1. The left panel contains a representative SEM micrograph, showing an array of nanowires and displaying the ability to grow multiple wires in predetermined arrangements. The bottom middle panel shows a cross-sectional TEM image of a single wire. This reveals the core/shell structure of these wires, with a bright Ge core and a darker Si shell. Already visible in the TEM contrast, is an intermediate layer between the Ge core and the substrate. This is identified as a SiGe layer via EDX, shown in the top center accompanied by a linecut to its left showing the Si/Ge contents as a function of height. This SiGe layer is highly problematic as it simultaneously reduces the strain, hole confinement and the hole accumulation in the core.

3. MBE grown NWs with anisotropic strain

Using an MBE system with silicon and germanium e-gun evaporators, core/shell wires have been grown at a temperature of 570 °C. Due to the better control over the amount of deposited material relative to MOVPE, the wire cross-sectional dimensions could be reduced to 55 x 15 nm. The homogeneity and composition of the wires are still a challenge, however. Their thickness varies between 5 and 20 nm over the length of single wires. Also, the growth temperatures required for selectivity lead to significant interdiffusion reducing the Ge content to 60%. Geometric phase analysis was applied to the STEM data enabling the extraction of the local lattice constants, revealing anisotropic strain exceeding 1%.

3. Conclusions

In summary, in-plane Ge/Si core/shell nanowires were grown using both MOVPE and MBE. Both methods still suffer from mobility of the Ge leading to alloying of the cores. However, the MBE grown wires show strained interfaces with anisotropic strain exceeding 1%, as measured via GPA analysis.

Acknowledgements

We thank NanoLab@TU/e for their help and support. This work has been supported by TOPSQUAD (Grant No. 862046). We furthermore acknowledge Solliance, a solar energy R&D initiative of ECN, TNO, Holst, TU/e, IMEC and Forschungszentrum Jülich, and the Dutch province of Noord-Brabant for funding the TEM facility.

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Figures

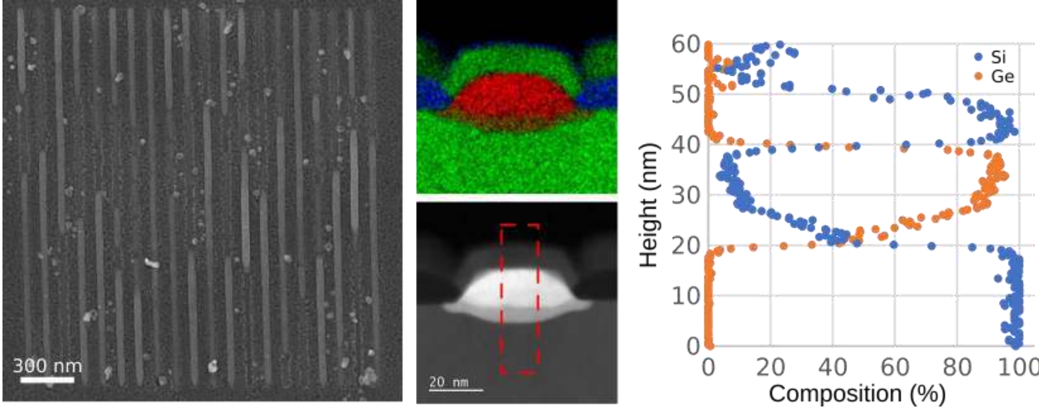

Fig. 1 - MOVPE grown Ge/Si nanowires. The left panel shows an SEM micrograph with the wires visible bright gray. The wire thickness varies strongly throughout the vertically running trenches. The middle panel shows EDX and STEM measurements, revealing both the core shell structure and an unintended SiGe intermediate layer. The right panel depicts a vertical linescan from which a nearly 50/50 ratio of Si and Ge in the intermediate layer can be extracted.

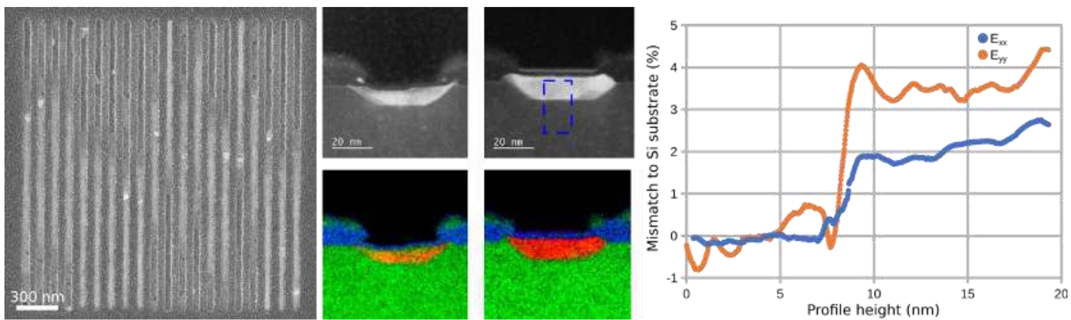

Figure 2 - MBE grown Ge/Si core/shell nanowires. The left panel shows an overview of 20 nanowires. The strong edge contrast is due to the wires in some parts being thinner than the SiO_2 mask. The middle panels show STEM images and corresponding EDX mappings of two representative wires. For the left wires, a thin non-oxidized shell is visible. For the left wire, GPA analysis in the area marked with blue dashes shows anisotropic strain, characterized by a difference in horizontal and vertical lattice constants.

Germanium/Silicon Core Shell Nanowires for Spin/Hole Qubits Fabricated by Chemical Vapour Deposition

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1. Introduction

Ultra-clean germanium/silicon (Ge/Si) core shell nanowires (NWs) have been predicted and proven to host highly stable hole spin qubits, controllable via Rashba spin orbit interaction [1] with a large scalability potential making it possible to develop realistic and reliable quantum computers [1, 2]. To maximise their performance, high quality crystalline NWs grown along ⟨110⟩ direction [3] with well-defined Ge/Si interfaces are needed. We develop ultra clean Ge/Si heterostructures by chemical vapour deposition (CVD) using the vapour liquid solid (VLS) techniques. More specifically, we have achieved the growth of crystalline Ge/Si core shell NWs, whose CVD deposition kinetics and crystalline quality were investigated.

2. Method

After deposition of metal catalyst nanoparticles (NPs) on a crystalline substrate, the substrate is heated up until the particles melt and mix with the substrate, forming eutectic alloy nano-droplets (Fig. 1a). Once the eutectic alloy is formed, the precursor gas (e.g. GeH_4) is injected into the reactor chamber at the desired temperature and pressure conditions.

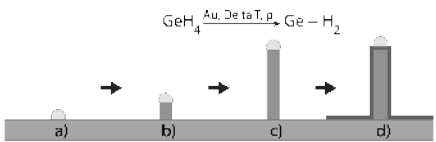

Fig. 1. General VLS process with a) formation of eutectic alloy nano-droplets (liquid), b) the addition of the precursor gas into the reaction chamber (vapour) and start of growth, c) elongation of the wires (solid), d) uncatalyzed shell growth.

Then, the NP acts as a catalyst to transform the GeH_4 to Ge and H_2. The Ge now accumulates in the NP until it is saturated. At this point, the Ge starts to precipitate at the interface between the NP and the substrate in a layer-by-layer manner, following the underlaying lattice order, when compatible - i.e. epitaxially. The NW starts to grow, in the so-called bottom-up fashion (Fig. 1b and Fig. 1c). As a last step, the growth conditions are changed and SiH_4 is injected into the chamber. SiH_4 decomposes and deposits in a conformal manner, leading to the formation of a Si shell around the Ge core (Fig. 1d).

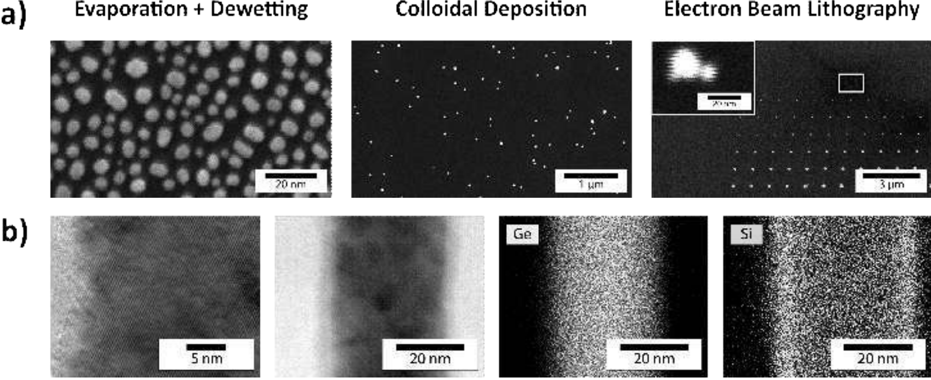

Fig. 2. a) Au NPs deposited by thin film dewetting (left), colloid deposition (middle) and EBL (right) b) HR-TEM bright field images of a crystalline defect-free Ge/Si core shell NW (left), STEM bright field image (middle left) and EDX analysis (right).

3. Results and Discussion

The growth of Ge/Si core shell NWs were obtained by the VLS mechanism, using gold NPs as catalyst. We optimized various NP deposition techniques to gain control over the NW diameter, areal density, and position (Fig. 2a). Special efforts were devoted to Electron Beam Lithography (EBL), leading to enhanced control over the NP material composition (right panel of Fig. 2a).

The growth kinetics of Ge and Si NW was investigated over a wide range of growth conditions. By optimising the CVD parameters, a reliable protocol was established to grow crystalline Ge NWs with the introduction of a low temperature (< 300 ºC) plasma enhanced deposition step for the Si shell. Using this approach, we were able to obtain fully crystalline Ge/Si core shell NWs, while avoiding the gold diffusion characteristic of high temperatures and responsible for shell contamination and disordered growth (Fig. 2b). The produced NWs exhibit Ge cores with diameters ranging from 5 to 30 nm, Si shells with thicknesses of up to 10 nm, defect free <110> axial nanowire growth direction and clean Ge/Si interfaces, as confirmed by electron microscopy (Fig. 2b).

4. Conclusions

We presented results on the bottom-up growth of crystalline Ge/Si core shell NWs, using a low temperature plasma enhanced shell growth technique, with dimensions in the range of 5-25 nm core diameter and 1-10 nm in shell thickness. The approach employed was gold (Au-)catalysed VLS mechanism by CVD.

Acknowledgements

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Germanium Quantum Wells for Spin Qubit Applications

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1.Introduction

In the last few years, interest in quantum computing has increased exponentially. One of the key aspects of this interest is the research of an optimal qubit realization scheme. Among many, the spin degree of freedom of electrons of holes in semiconductor quantum dots (QDs) represents one of these possible schemes [1], [2]. Hole spin qubits are created by electrostatically gating a 2DHG to define QDs with discrete energy levels, and the spin states are Zeeman-split by a magnetic field.

At the same time, interest in germanium is growing, as a material for applications beyond the state of the art of silicon devices. One of the reasons is that germanium is the mainstream semiconductor with the highest p-type mobility.

Ge quantum wells (QWs), are attracting interest due to possible applications which benefit from the properties of the 2-dimensional hole gas (2DHG) formed in the Ge QWs. Another factor of interest is the high compatibility of SiGe devices with existing Si-based technology, favouring a future integration.

The epitaxial growth of the germanium QW, cladded by barriers with relatively high Ge content, can be achieved following two different approaches: a reverse graded buffer, in which, starting from pure germanium, the Si content is increased up to the final amount [3], or a forward graded buffer, where starting from pure silicon the Ge concentration is linearly increased [4].

Material quality is a critical factor for qubit performances. For this reason the characterization of the electrical properties of the 2DHG by Hall measurements at cryogenic temperatures is a typical and effective approach, in order to extract different parameters: the carriers mobility represents a first indication of the material quality, and the percolation density is identified as the main figure of merit linking electrical properties to qubit performance.

In this work the electrical characterization of a 2DHG hosted in a Ge QW grown on a forward graded buffer is presented. In addition to the evaluation of the parameters mentioned above, a deeper analysis has been performed, understanding the contribution of different scattering mechanisms, and considering the quantum properties of the material.

2. Samples growth and fabrication

A Ge QW has been grown by a plasma-activated variant of chemical vapor deposition, LEPECVD (low-energy plasma-enhanced CVD) on a $Si_{0.3}Ge_{0.7}$ substrate.

Fig. 1. Schematic view of the grown structure.

LEPECVD is a fast and efficient growth technique so a relatively thick (several microns) forward graded buffer can be used in which the Ge content is linearly increased from pure Si up to the final amount desired.

The growth rate can also be decoupled respect to the substrate temperature. This allowed a reduction of substrate temperature, helping to mitigate interdiffusion effects at the QW interfaces and strain-induced roughening of the upper QW interface.

The sample has been then structurally characterized by HR-XRD, extracting the real composition of the different layers and confirming the strain applied on the quantum well [4].

Metal-oxide-semiconductor (MOS) structures are fabricated, using an AlOx dielectric deposited by ALD.

3. Electrical characterization

Electrical characterization measurements were performed at low temperature (1.6-10 K) on Hall bar devices, both gated and ungated, in order to understand the effect of the Al_2O_3 oxide deposition and of the metallic gate on the carrier mobility as a function of sheet density, reaching a value higher than 100000 cm^2/Vs [4].

A scattering mechanisms analysis has been performed, estimating the impact of each mechanism on carriers mobility and the different scattering lifetimes. This analysis resulted in the identification of the neutral impurities scattering as the main limiting factor for carriers mobility. This mechanism, along with roughness scattering, is keeping a relatively low value of the Dingle ratio, defined as the ratio between transport and quantum scattering lifetimes.

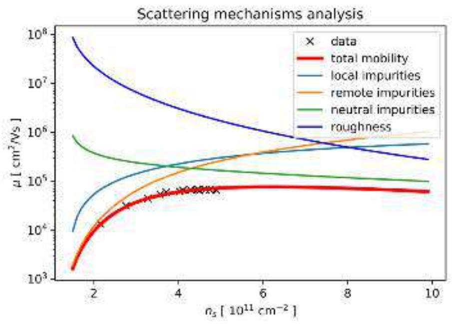

Fig. 2. Scattering mechanisms analysis plot.

From the same dataset the percolation density has been calculated, as one of the most relevant figures of merit for qubit stability, with a value of around 10^{11} cm^{-2}.

Shubnikov–de Haas (SdH) oscillations and quantum Hall effect were observed. The first allowed the direct calculation of the holes effective mass and of the Dingle ration. The last was observed in an anomalous form at high bias, lacking extended zero resistivity regions and corresponding plateaus in the transverse resistivity, while the peaks featured an elliptical shape instead of the theoretical Lorentzian shape.

Finally, the Landau level lifetime, which corresponds to the quantum scattering lifetime, was extracted from SdH oscillations. This proved to be relatively high as compared to the momentum lifetime coming from mobility, which may help to explain the excellent results obtained by collaborating research groups which fabricated qubits on this material [4].

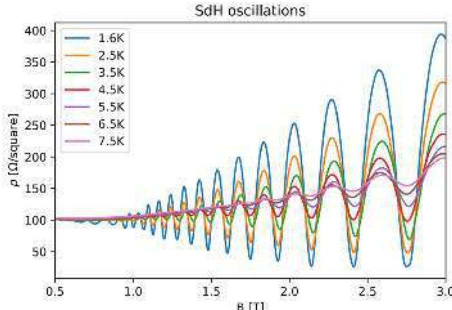

Fig. 3. Shubnikov-de Haas oscillations observed in the 2DHG.

3. Conclusions

A strained germanium quantum well designed for hosting a singlet-triplet qubit has been grown on a virtual substrate by LEPECVD, then structurally characterized by HR-XRD.

On this stack than Hall bar shaped MOS structures were fabricated and electrically characterized at cryogenic temperatures, extracting some important figures of merit such as the percolation density.

A deeper analysis on scattering mechanism was performed, highlighting the relevant role of neutral impurity scattering as the main limiting factor for carriers mobility.

Acknowledgements

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Optical study of isotopically pure ^{70}Ge-on-Si films

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1. Introduction

The growing need for fast and secure data processing and transmission has led to a quest for combining sensing, storage, and communication in semiconductor devices. Spin and photon degrees of freedom are emerging as potential alternatives to current electronics based on charge transport. Coupling them is challenging, but it holds the promise of creating a new generation of high-performance, energy-efficient, and multifunctional devices. Isotopic composition can have a significant impact on a wide range of physical properties relevant to this need. These properties include the energy and lifetime of phonons, bandgap amplitude, thermal conductivity, and expansion coefficient. A field that is particularly sensitive to the isotopic composition is spintronics, which utilizes the electron spin for information storage and transmission of data. By controlling the isotopic composition of a material, it is possible to intentionally introduce or eliminate nuclear spins and nuclear magnetic moments. This can have a significant impact on the spin coherence and spin lifetime, and, in turns, determine the ultimate performance of spintronic devices and quantum processors [1].

In this work, we explore some of the aforementioned features by investigating by means of Raman and photoluminescence (PL) spectroscopy the optical properties of isotopically pure ^{70}Ge films deposited on Si. Our findings can provide a steppingstone towards the use of isotopes in future Ge-based devices that demonstrate quantum advantages.

2. Discussion

2.1. Samples and Experimental Techniques

The samples were either 4 µm thick layers of ^{70}Ge or Ge having a natural abundance. The Ge films were epitaxially grown on Si(001) substrates using a low-pressure CVD reactor. Micro-Raman measurements were performed using a Horiba T6400 spectrometer and a 532 nm Nd:YAG laser. PL measurements were conducted at 4 K using a backscattering geometry in a closed-cycle cryostat. A Nd:YVO$_4$ laser at 1.165 eV was coupled to an optical retarder and used as a circularly polarized excitation source. The laser beam was focused to a spot size of approximately 50 µm in diameter, resulting in an excitation density of 3.2 kW/cm^2 on sample surface. The PL polarization was analyzed by a quarter-wave plate and a polarizer. Light was spectrally resolved through a grating spectrometer and an (In,Ga)As array detector. This experimental apparatus enabled us to accurately determine the energies of the direct gap transitions involving the strain-split light (LH) and heavy holes (HH) states.

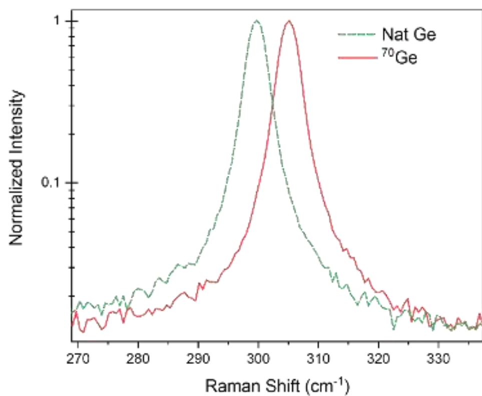

Fig. 1. Raman spectra of isotopically pure ^{70}Ge (solid red line) and natural Ge (dashed green line). These are 4 µm layers deposited on Si. The spectra were measured at room temperature using a 532 nm excitation laser.

2.2. Results

Figure 1 shows the Raman spectra of the samples in the vicinity of the first-order Ge-Ge vibrational mode. The Raman peak pertaining to the sample having a natural abundance of the isotopes turns out to be redshifted with respect to a reference provided by a commercial bulk Ge wafer (not shown). This elucidates the presence of a residual tensile strain (~0.2%), which is due to the thermal mismatch between the Ge epilayer and the Si substrate. Noticeably, the peak of the ^{70}Ge film shows a distinct displacement by about 5 cm^{-1} towards higher Raman shifts. This drastic change of the vibrational properties of the lattice provides us with a clear proof of the isotopic enrichment of this layer. We can find reassurance of this interpretation by the striking agreement between the measured blueshift and the results previously reported in the literature on enriched

bulk Ge crystals [2].

Since LHs hold the promise for future implementation of ultrafast gate-defined spin qubits [1, 3], in the following we investigate whether tensile strain can enable the lifting of the valence band LH/HH degeneracy at the center of the Brillouin zone also in the isotopically purified sample. For this purpose, we leverage a contactless investigation method offered by the optical spin orientation combined with the analysis of the polarization-resolved emission across the direct gap [4].

Following the spin-dependent selection rules for the dipole-allowed transitions, the radiative recombination involving strain-split light (cΓ-LH) and heavy hole (cΓ-HH) bands can be unambiguously resolved in our samples at cryogenic temperatures (see Fig. 2). Owning to the tensile strain in the Ge-on-Si heterosystem, the fundamental transition can be ascribed to be the cΓ-LH recombination. Above all, the energy separation between the two peaks of the doublet demonstrates to be consistent with previous reports on Ge-on-Si heterostructures and with the expected LH-HH splitting due to the tensile thermal strain experienced by the epilayers. Such a splitting is indeed present in the natural as well as isotopically enriched epitaxial Ge films.

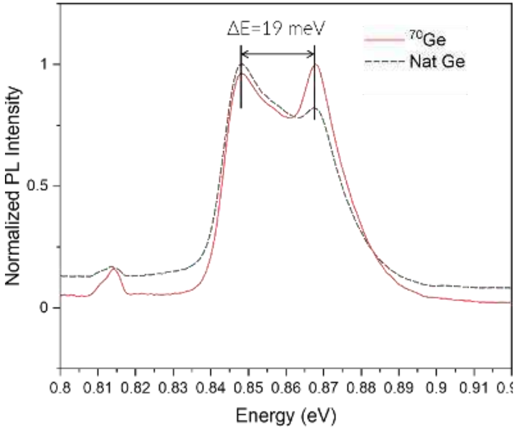

Fig. 2. Low temperature (4 K) polarization-resolved PL spectra of the epitaxial ^{70}Ge (red solid line) and natural Ge (black dashed line) layers. The low (high) energy feature is ascribed to direct gap optical transitions involving light (heavy) holes. The energy splitting of 19 meV is due to the tensile strain that is present in the epitaxial Ge-on-Si layers.

3. Conclusions

We have verified that our heterostructures are based on isotopically purified germanium in which tensile strain is present. This leads to the removal of the LH/HH degeneracy, which is of specific interest for quantum technology applications, e.g., for implementing single-photon receivers. These devices have the potential to maintain coherence between the polarization of the photon and the spin of the stored charge, thus opening novel routes towards effective information storage in quantum repeaters along secure communication networks [3, 5].

Acknowledgements

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CVD-grown Nuclear Spin-depleted 70Ge/SiGe Heterostructures

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1. Introduction

Ge-based heterostructures have been in the limelight because of their relevance to integrated photonic circuits,[1,2] sensing,[1] high-mobility electronics,[3] and solid-state quantum computing.[4] The latter aims at exploiting the advantages of hole spin in Ge, including their inherently large and tunable spin-orbit interaction (SOI) and their reduced hyperfine coupling with nuclear spins, to establish scalable spin qubits.[5-9] In fact, Ge/SiGe planar heterostructures are currently considered forefront candidates for quantum processors.[4] However, despite the anticipated reduced hyperfine interaction, recent reports pointed out to a still significant effect of nuclear spin bath on the hole spin qubit behavior.[10]

These observations indicate the need for nuclear spin-depleted heterostructures to elucidate the sensitivity of Ge qubits to hyperfine interactions. At the same time, these isotopically engineered heterostructures will also allow to decouple the role of charge noise, which is believed to be the dominant decohering process. Tackling this research line requires the development of Ge-based quantum devices that are depleted from ^{73}Ge, which is the only Ge nuclear spin-full stable isotope.

With this perspective, herein we demonstrate the epitaxial growth of isotopically purified ^{70}Ge quantum well (QW). The growth of ^{73}Ge-depleted QWs is achieved using the chemical vapor deposition (CVD) method which is broadly adopted in Ge device research and is compatible with the processing standards in of the semiconductor industry.

2. Method

The epitaxial growth of Ge/SiGe heterostructures was carried out in a reduced-pressure CVD on 4-inch (001)-oriented Si wafers using isotopically purified monogermane ($^{70}GeH_4$) with an isotopic purity higher than 99.9% carried by hydrogen gas. The precursor was enriched in a centrifugal setup using natural monogermane as a starting gas. After purification, the precursor contains a negligible amount (<0.006 at. %) of other Ge isotopes. Moreover, the chemical contaminants, including other hydrides, in the ^{70}GeH4 precursor have an average content below 0.06 µmol/mol.

The QW structure (Fig.1 (a)) growth begins with the Ge virtual substrates (VS) that is annealed at 875°C followed by graded SiGe and SiGe-VS, using natural unpurified precursors. Without stopping the growth, the supply is switched to the purified $^{70}GeH_4$ precursor to grow the 290nm first barrier (BR1) at 600 °C and 20 Torr with partial pressures of 0.16 Pa for Si_2H_6 and 2.11 Pa of $^{70}GeH_4$ and growth rate of 36.3 nm min^{-1}. The reactor is then purged in H_2 for 90s before resuming the growth of the ^{70}Ge QW layer (600 °C, 20 Torr, 2.82 Pa of $^{70}GeH_4$, for 45nm min^{-1}). The 28 nm second barrier (BR2) is then grown at the same conditions as BR1. Finally, a Si Cap of a few nm is grown to protect the structure.

The characterization of the resulting structure was performed with several techniques. The crystalline quality as well as lattice strain were evaluated from X-ray diffraction (XRD) (224) reciprocal space map (RSM) on a Bruker Discover D8.

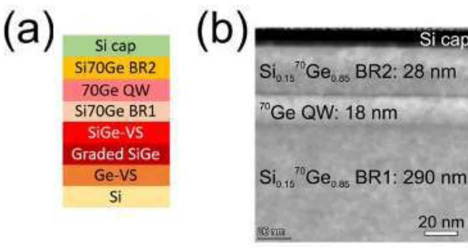
The microstructure of the ^{70}Ge/SiGe QWs was investigated using transmission electron microscopy (TEM) with a Thermo Scientific Talos F200X S/TEM system at an acceleration voltage of 200 kV.

The isotopic purity and chemical composition of the QW structure were studied by time-of-flight secondary ion mass spectrometry (ToF-SIMS) and atom probe tomography (APT).

3. Results and Discussion

Observing the heterostructure by TEM reveals (Fig. 1(b)) well-defined layers and no obvious defects close to the QW stack. The transitions between the BR1-2 and QW layers, as seen in TEM is of the order of 1-2 nm.

XRD analysis of the as-grown heterostructures demonstrates sharp 224 reflections for the virtual substrates, barriers as well as the signature of the strained 18 nm thick ^{70}Ge layer, suggesting an excellent degree of crystallinity across the structure (Fig. 1(c)). Here, the difference in composition between the natural and purified SiGe alloy layers ($Si_{0.18}Ge_{0.82}$ *vs.* $Si_{0.15}{}^{70}Ge_{0.85}$ as determined by APT) is related to the composition differences of the germane precursor supplies.



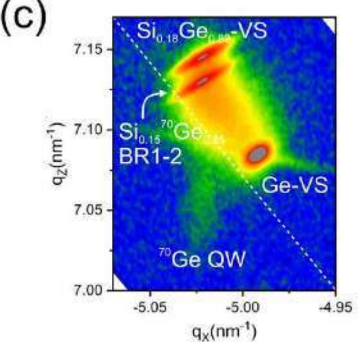


Fig. 1. (a) Schematic illustration, (b) representative cross-sectional TEM image, and (c) the (224) RSM results of the CVD grown ^{70}Ge/SiGe heterostructure.

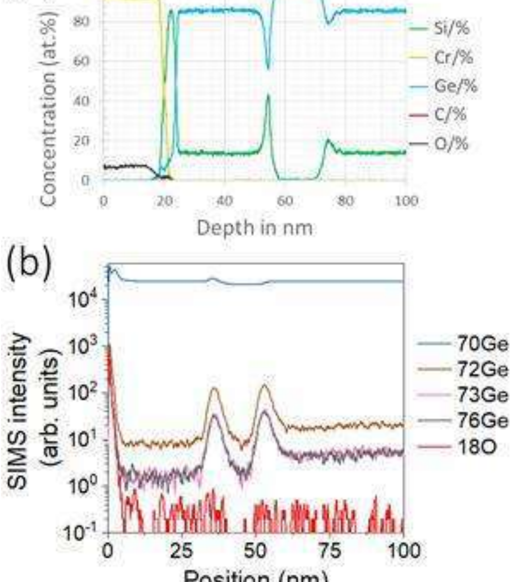


Fig. 2. (a) APT determined composition profiles and (b) ToF-SIMS intensity of different elements as a function of depth in as-grown ^{70}Ge/SiGe heterostructure.

APT results (Fig. 2(a)) indicate that BR1 and BR2 are $Si_{0.15}{}^{70}Ge_{0.85}$ alloys, and that the ^{70}Ge QW is close to 100% Ge, with relatively uniform elemental compositions except at the interfaces between BR1-2 and the ^{70}Ge QW layer, where a steep rise in the silicon concentration is evident. The width of the resulting interfaces is determined to be a few nm in APT, consistent with TEM observations. Optimization of spin qubit performance requires sharp and ordered QW interfaces and improvements to the growth process of our structures are now considered.

ToF-SIMS analysis results (Fig. 2(b)) qualitatively presents the distribution of relevant isotopes and contaminants as a function of depth in the sample. By estimating the ^{70}Ge purity using the ^{70}Ge/^{76}Ge intensity ratio for the Ge-VS layer, excellent purities of 99.98% in the BR1, 99.97% in the 70Ge QW and 99.94% in the BR2 layers are found. Similar levels of purities are obtained when using the intensity ratios for other Ge isotopes. This level of purity seems to degrade around the BR-QW interfaces. As for the contamination levels in the structure, oxygen (18O-) concentration is negligeable and only detected near the surface of the structure.

3. Conclusions

An isotopically purified (>99.9% ^{70}Ge), highly crystalline ^{70}Ge quantum well structure grown with CVD was demonstrated. Ongoing efforts aim to improve the sharpness and composition of the interfaces of the QW and grow structures with purified ^{28}Si to remove ^{29}Si nuclear spins. The interplay with the heterostructure structural properties and optical and electronic behavior will be discussed at the conference.

Acknowledgements

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Optimizing Germanium Quantum Wells for Spin Qubits

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1. Introduction

Semiconductor-based qubits using the spin degree of freedom are making strong progress as a quantum computing hardware platform [1]. Hole spin qubits are created by electrostatically gating a two-dimensional hole gas (2DHG) to define quantum dots (QDs) with discrete energy levels, and the spin states are Zeeman-split by a magnetic field [2]; the spin-orbit interaction then allows electrical manipulation of individual spins [3-5].

2DHGs formed by gating a metal-oxide-semiconductor structure based on a germanium quantum well (QW) have demonstrated mobilities of around one million cm^2/Vs and higher, with mobility generally increasing as the hole sheet density in the 2DHG increases [6]. Since the formation and operation of qubits requires almost complete depletion, another more relevant figure of merit is the critical sheet density at which the transition from metallic to percolation transport takes place [7]. These parameters are generally obtained via the characterization of the 2DHG by Hall measurements at cryogenic temperatures.

The highest mobilities have been measured in Ge QW structures grown by reduced-pressure chemical vapour deposition (RP-CVD), using a “reverse-graded” buffer in order to obtain a high-quality strained Ge QW on a silicon substrate. Ge QWs grown by low-energy plasma-enhanced chemical vapor deposition (LEPECVD) using a forward-graded buffer tend to show maximum mobilities of only around 100,000 cm2/Vs [8] but have nevertheless led to the realization of qubits with very good performance [4].

In this work, electrical characterization of the 2DHG hosted in Ge QWs grown by LEPECVD is presented. In addition to the figures of merit mentioned above, calculations of scattering mechanisms and simulations of transport in the Shubnikov–de Haas and quantum Hall effect regimes are performed in order to gain insight into the paths towards optimizing Ge QWs for spin-based qubits.

2. Sample growth and fabrication

2.1. Growth of QW structures

The LEPECVD uses a low-energy plasma to activate gaseous precursors (SiH_4 and GeH_4) so that growth rates are almost completely independent of substrate temperature, and can reach 5-10 nm/s. This allows a 10 µm forward-graded buffer with low dislocation density to be grown to a final Ge content of 70% in 30 minutes [9]. The Ge QW stack and $Si_{0.3}Ge_{0.7}$ barrier and cap were then grown at a substrate temperature of 350°C and growth rate of about 0.4 nm/s. The QW and cap composition, strain state, and thickness were verified with high-resolution x-ray diffraction and dynamical simulations [4].

2.2. Hall bar fabrication

Hall bar were fabricated with electron-beam lithography and a dry etching process to define the mesa. Electrical contacts were made using Pt. ~20 nm of aluminum oxide was grown by atomic layer deposition at 300°C to form a gate dielectric. The gate itself consists of 3 nm Ti and ~100 nm Pd.

3. Electrical characterization

Electrical measurements were carried out down to 1.6 K and up to 7.5 T in a closed-cycle cryostat with a superconducting magnet. Mobility and sheet density were generally found from low-field measurements (< 1 T). The effective mass m^* and Dingle ratio between transport and quantum scattering lifetimes $\alpha = \tau / \tau_q$ were found from Shubnikov–de Haas oscillations while at higher fields the quantum Hall effect (QHE) was observed.

4. Analysis

4.1 Scattering mechanisms

The mobility was analyzed in terms of linear transport theory, considering scattering from both local and remote charged impurities, neutral impurities, and interface roughness. Both transport and quantum scattering lifetimes were calculated so that Dingle ratio data could be used to distinguish mechanisms leading to small or large angle scattering.

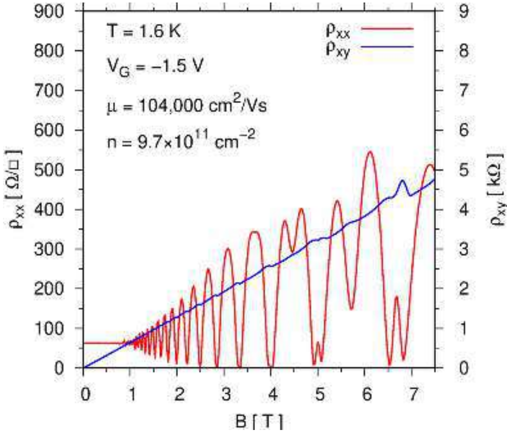

Fig. 1: At high bias, quantum Hall plateaus are washed out and there are no extended regions of $\rho_{xx} \sim 0$.

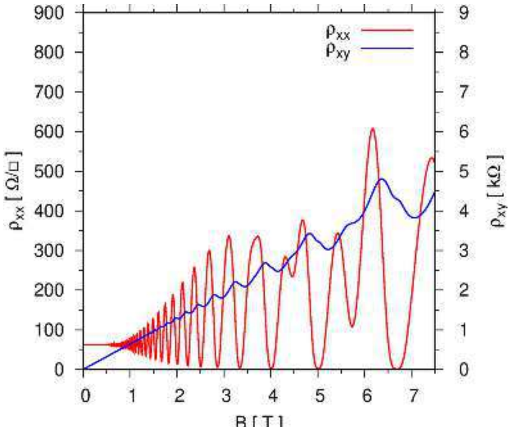

Fig. 2: Simulation of Shubnikov-de Haas oscillations and the QHE regime without Fermi level pinning, with $\alpha \sim 5$ and $g^* \sim 4$.

4.2 Strong magnetic field regime

Low-field Shubnikov–de Haas oscillations are usually understood in terms of the oscillatory components of the density of states [10-12] which describes a series of spin-degenerate Landau levels (LLs) broadened by τ_q and then further broadened by the Fermi occupation function at non-zero temperature. At higher fields, Zeeman splitting of spin states can be approximated by $\pm\frac{1}{2}g\mu_B B$ in the absence of spin relaxation [13]. The model can be extended into the quantum Hall effect regime as long as some common approximations, valid at low field, are no longer allowed.

In order to conserve the sheet density of carriers, the Fermi energy needs to change as the density of states varies. The low density of states between LLs would mean that the Fermi level skips from one LL to the next, but in the quantum Hall regime the characteristic ρ_{xy} plateaus, accompanied by ρ_{xx}~0, require that the Fermi level remain pinned between LLs. This is usually explained in terms of localized states due to the presence of impurities. The anomalous behavior seen at high bias in Fig. 1 suggests an absence of Fermi level pinning, as simulated in Fig. 2.

5. Conclusions

Ge QWs have been grown on forward-graded buffers by LEPECVD. Analysis of Shubnikov–de Haas oscillations suggest that τ_q is relatively long in these QWs, especially when biased towards high sheet density. τ_q may even be higher in LEPECVD-grown QWs than in QWs grown by RP-CVD despite the lower overall mobility. At higher magnetic fields with the QW in the quantum Hall effect regime, ρ_{xy} showed conventional plateaus, accompanied by ρ_{xx}~0, at low bias but anomalous behavior was observed at higher bias.

The relatively long quantum lifetime and absence of Fermi level pinning at high bias suggest that neutral rather than charged impurities limit the mobility.

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