IC/semiconductors(IC+OSD)

3D x3D x3D

Chee Wee Liu (劉致為)
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http://nanosioe.ee.ntu.edu.tw

High mobility/high K/FinFET

PPACR (performance, power, area, cost, reliability)

Google Scholar Page

(Citation :7472/ H index:39 / i10 index:182)

https://www.digitimes.com.tw/seminar/DWebinar_20220824/

「白米滿足人類食物需求；
電晶體滿足人類精神所需」

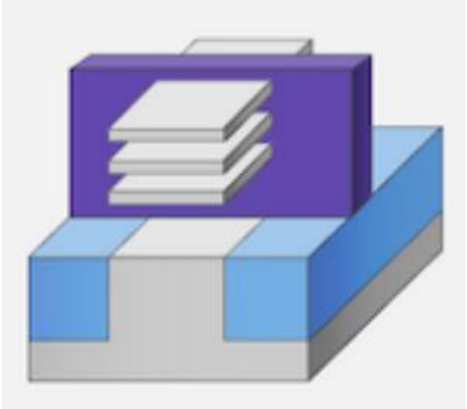
蔡明介董事長

Saturday 2-4pm free course

- Free handout
- Free textbook
- Free schedule
- Cyclic
- No need to register for special project course
- Welcome to join 2-4 pm on Sat
- Snacks, Pizza ??
- Research involvement:4000-8000NT

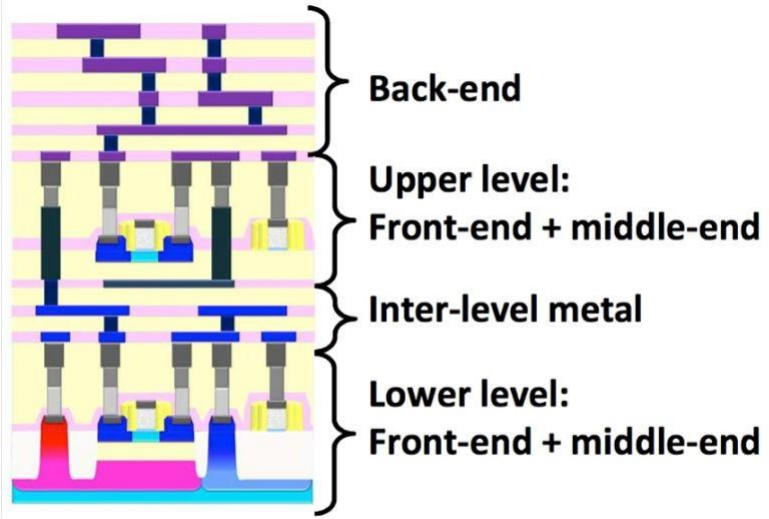
3Dx3Dx3D

3D



Channel stacking

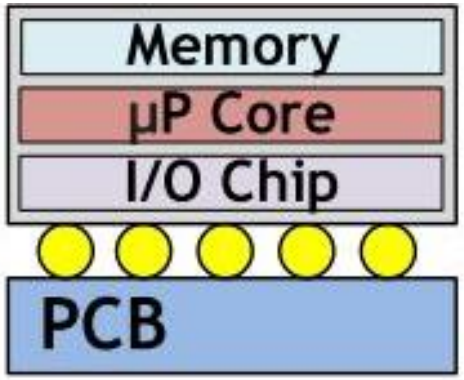
3D



Transistor stacking

Monolithic /Sequential (w/ BEOL)

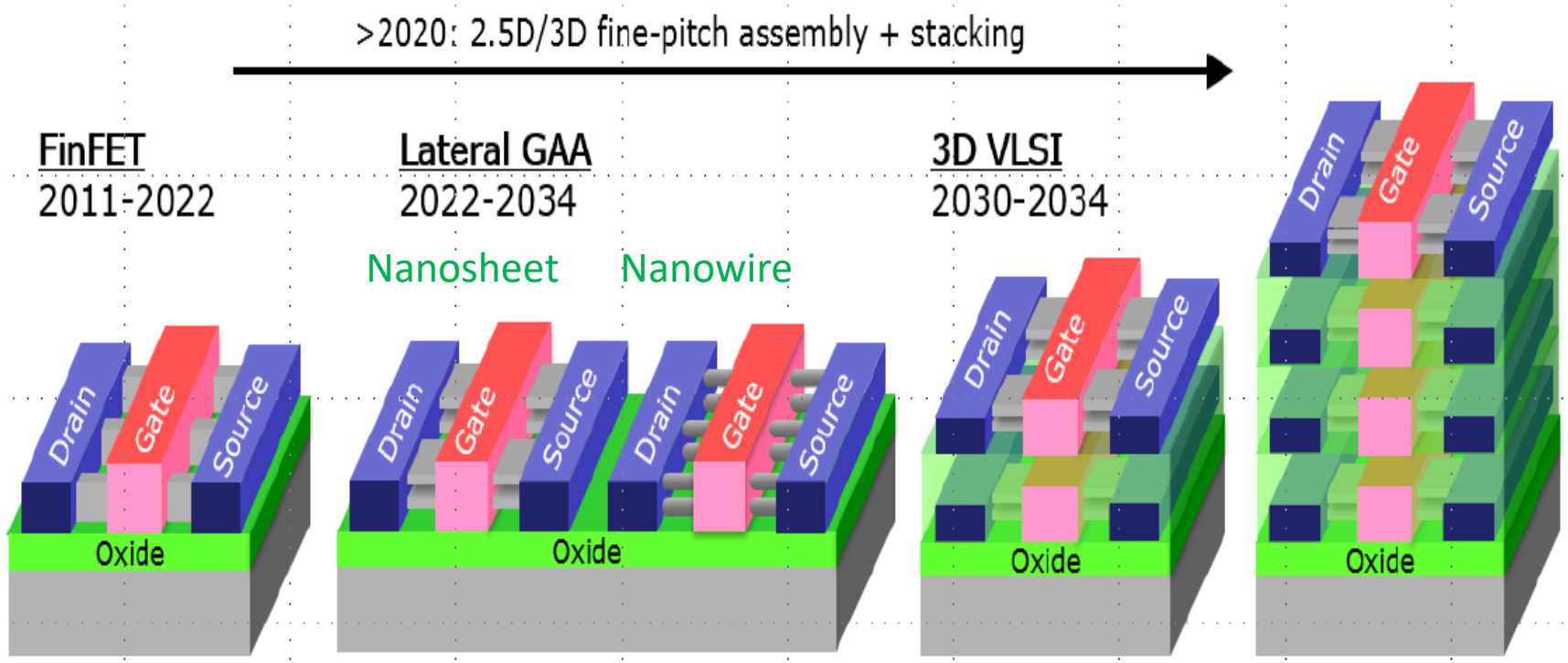
3D (Far backend/ Heterogeneous integration)



Dielets/Chiplets Stacking

SoIC (2D+3D)

IRDS,2020 Edition More Moore



Research topics

- **CMOS:**

  Stacked Nanosheet /King/tree channel (1nm and beyond)

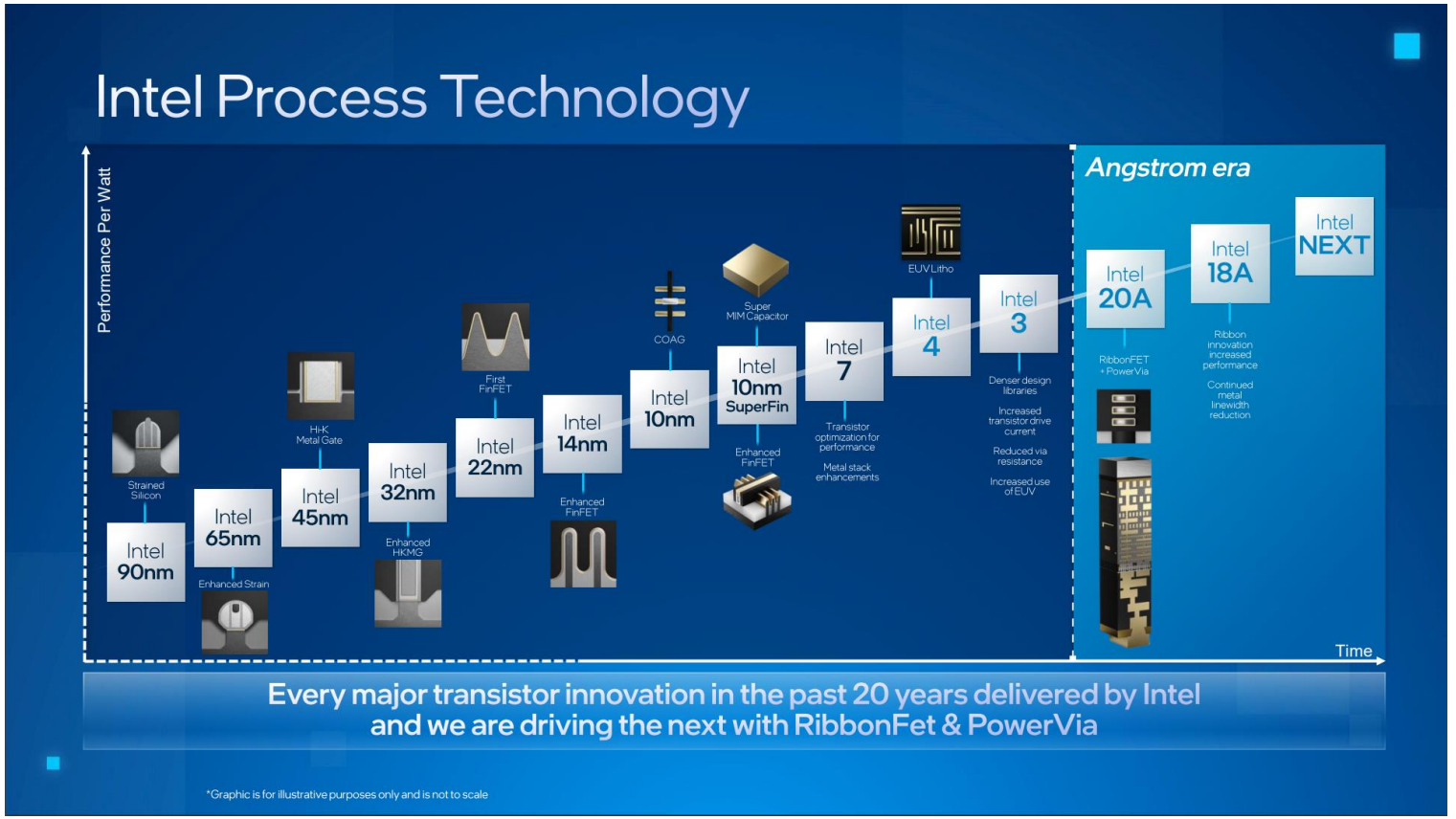
  Thermal modeling

  SRAM

  transistor stacking (CFET n/p)
- **xxx MRAM/MTJ/SOTxxx**
- MIM/FTJ/DRAM
- IGZO (backend transistor) 3D integration
- CMOS image sensor

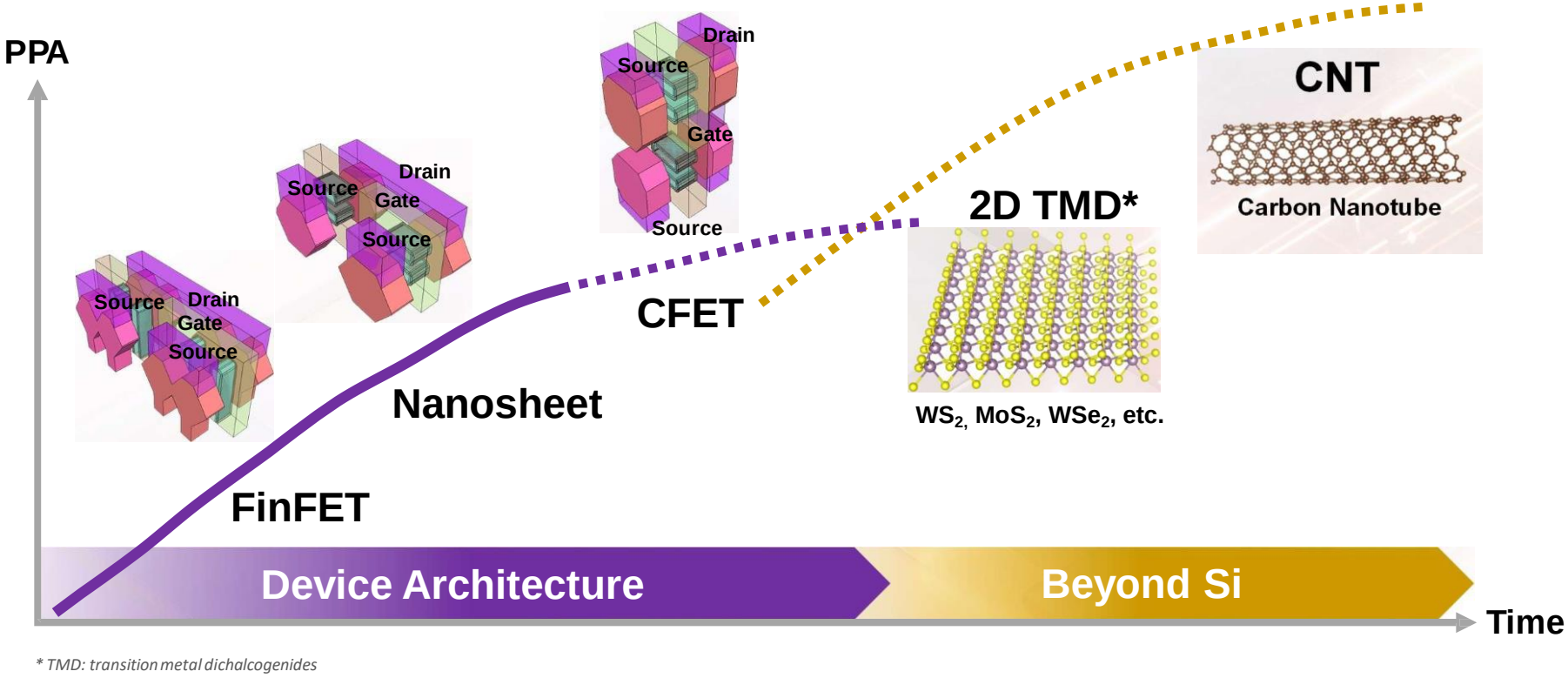
IMEC 2022

- CFET (transistor stacking, nFET on pFET or p on n) starts at A5 (0.5nm node)
- Atomic (2D) in A2 node (0.2 nm node)



- **Intel 20A & 18A(Angstrom Era) → 1st RibbonFET(4 stacked channels) + Power Via**
- **TSMC GAA 2nm/Samsung GAA 3nm**

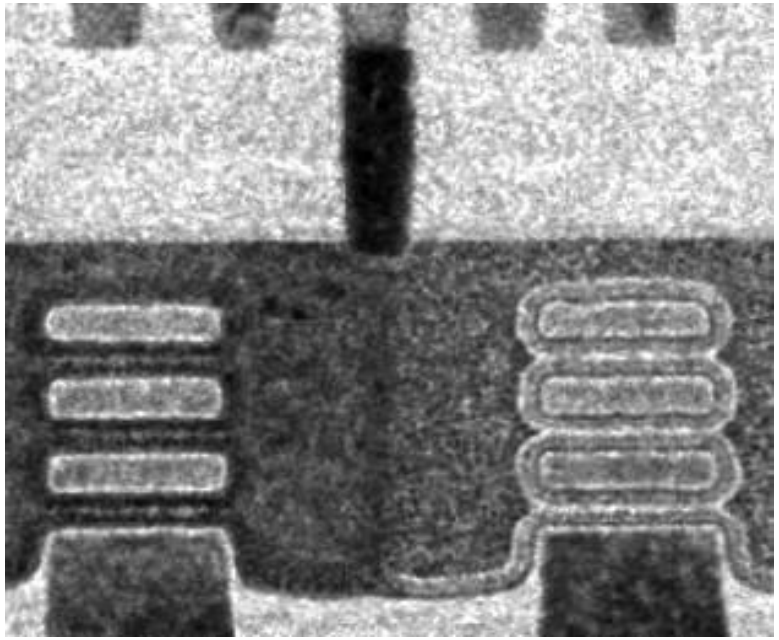
Device Architecture Outlook

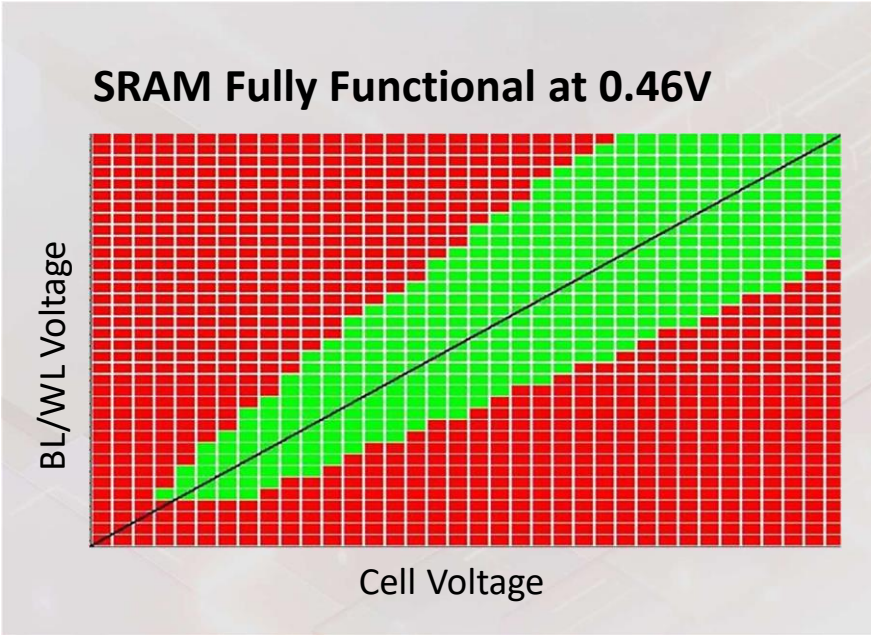


* TMD: transition metal dichalcogenides

- **CFET after nanosheets**
- **2D after CFETs**

Nanosheet Transistor

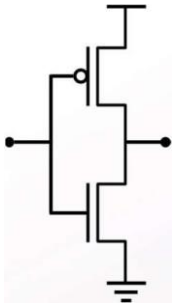


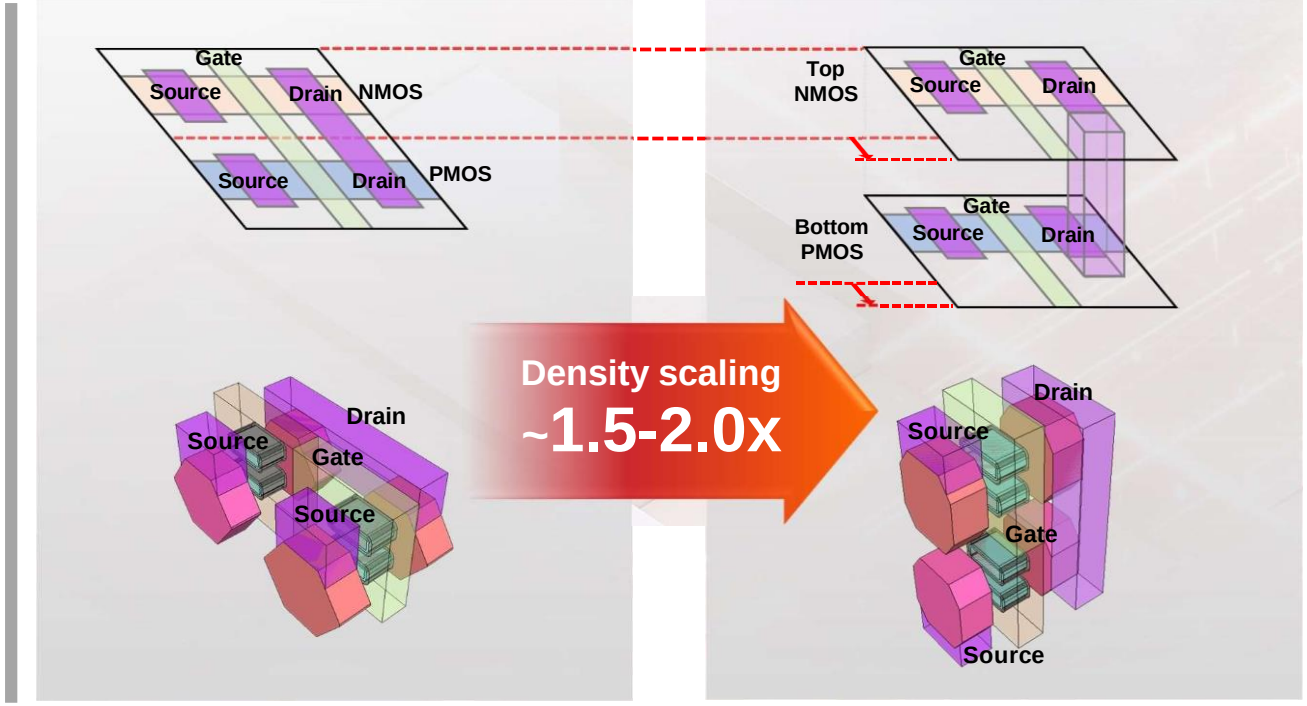


- Tight space sheet reduces para C.
- N/P are different
- Smaller SS and better short channel control to achieve low Vdd and low power.

CFET Density Scaling

Inverter





CFET Process Challenges

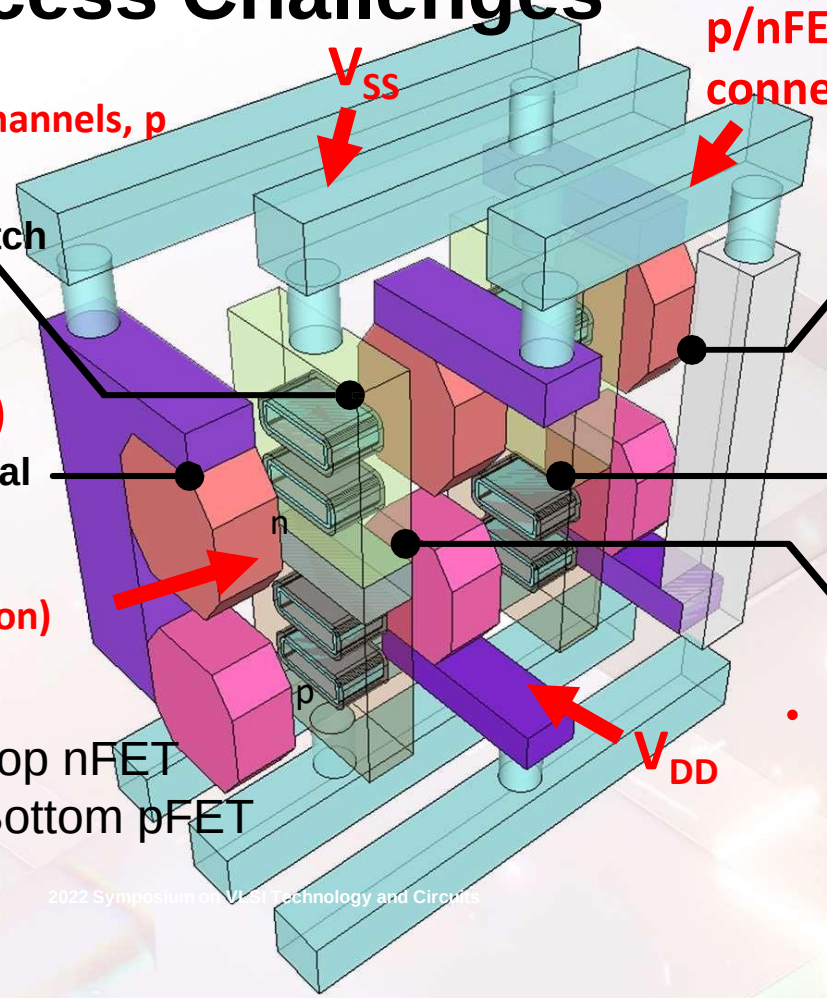
- Fin height including n channels, p channels, and SLs

High aspect ratio etch

(Same as nanosheet)

Low resistance metal gap-fill

(dielectric isolation)



High AR & Low-R metal gap-fill

- Vertically stacked dual metal gate process is needed. (recess and deposition)

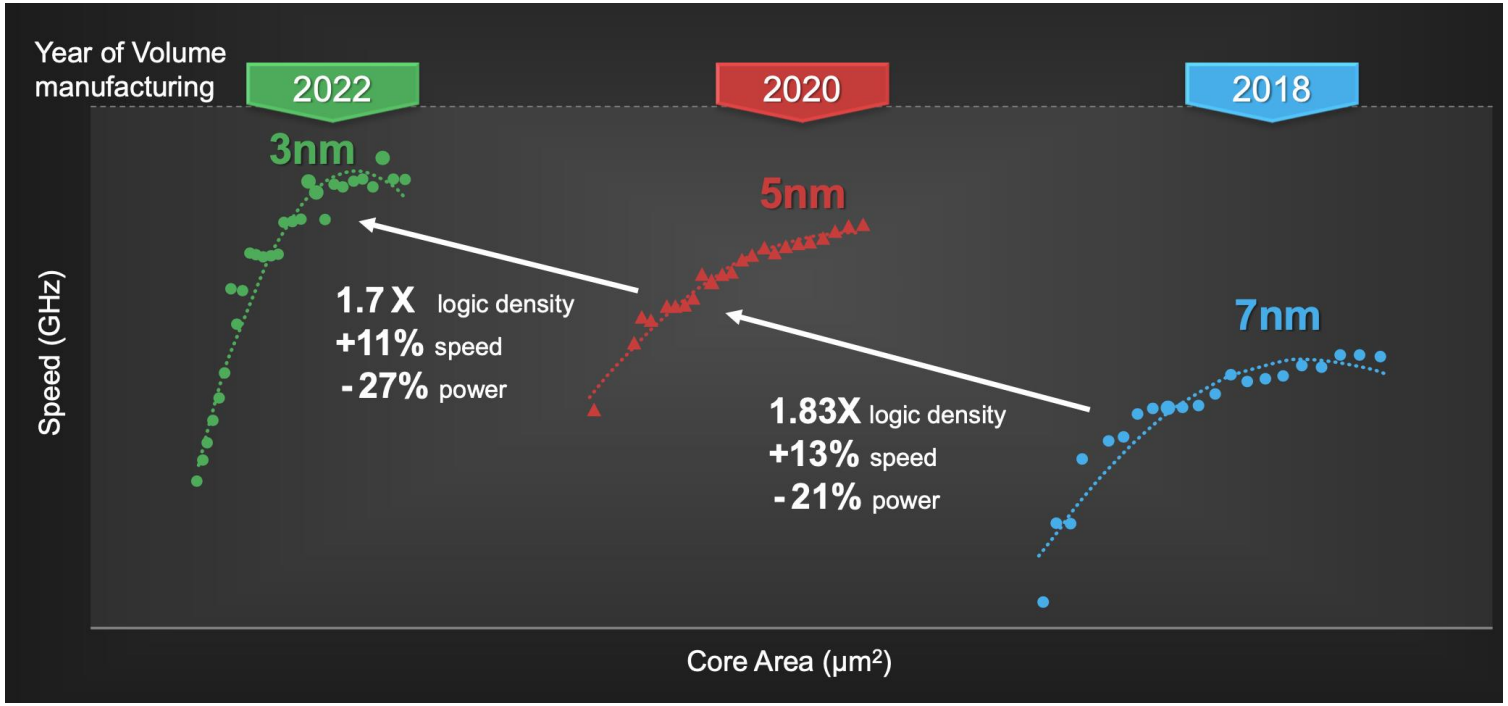
Multi-Vt for both n/pMOS

(independent gate control)

Gate isolation

- Creating isolation between NMOS/PMOS gate

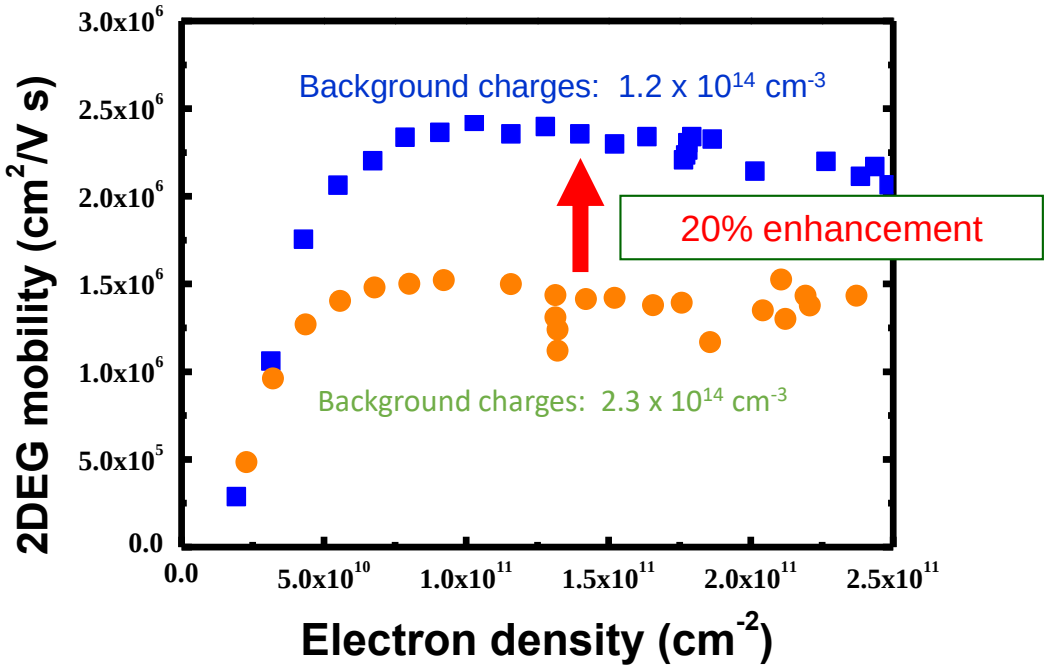
7, 5, 3 nm



Mark Liu, Plenary Session 1.1, ISSCC 2021.

- **Marching forward at historical rate for full nodes w/ ~1.8X density/2 years**
- **2nm will be on scheduled**
- **PPACR**

Record High 2DEG Mobility (2.4 M $cm^2/V\ s$)

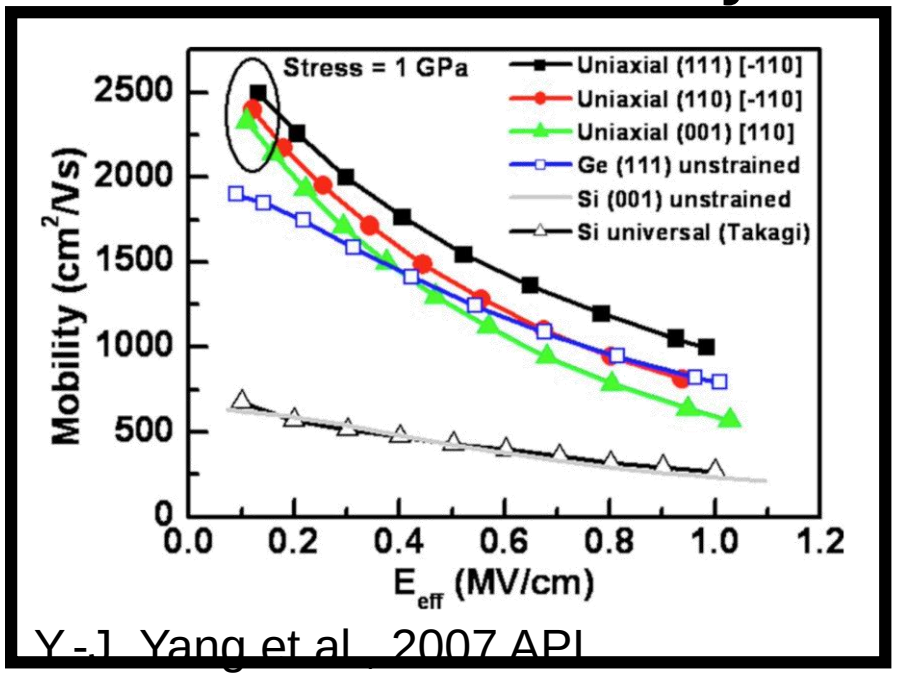


M. Yu. Melnikov et al., APL, 106, 092102 (2015).

Collaborate with Prof. S. V. Kravchenko, Northeastern Univ.

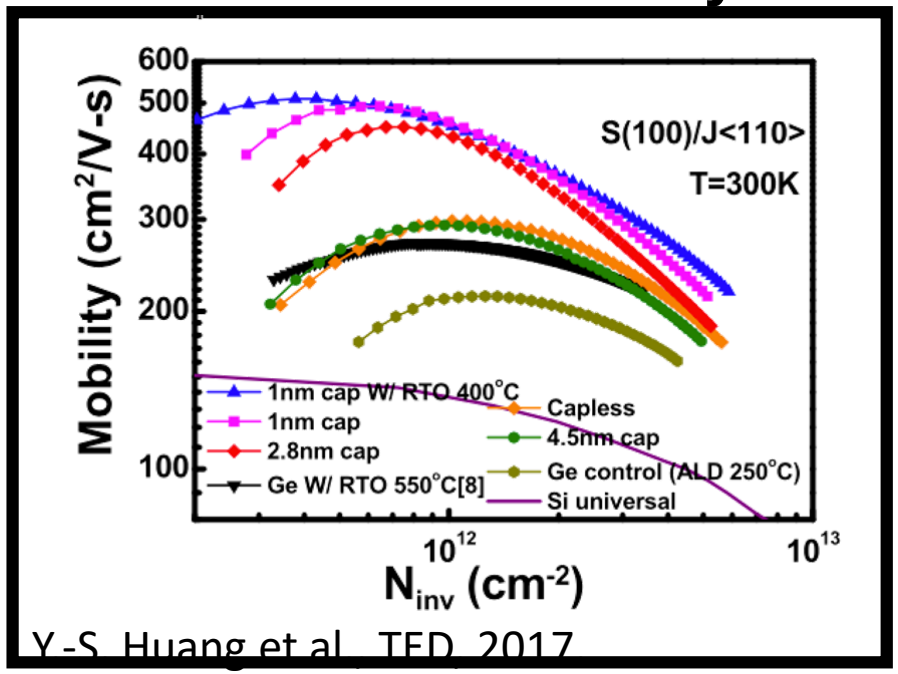
- 2.4 x 10^6 $cm^2/V\ s$ by the reduction of background charges from 2.3 x 10^{14} cm^{-3} to 1.2 x 10^{14} cm^{-3}.

Ge electron mobility



Y.-J. Yang et al., 2007 APL

GeSn hole mobility

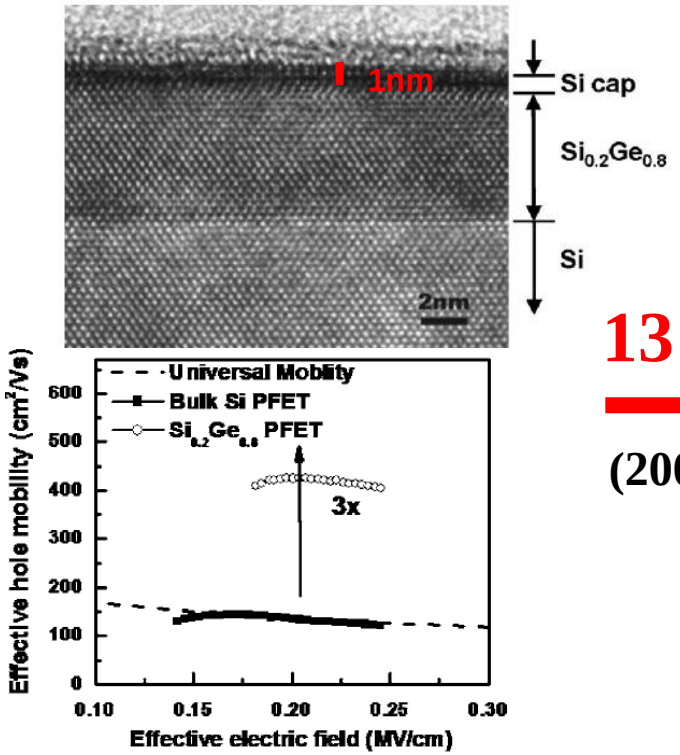


Y.-S. Huang et al., TED, 2017

- **Ge has higher electron mobility than Si.**
- **GeSn/Ge has higher hole mobility than Si.**

MOST advanced FinFET on the market

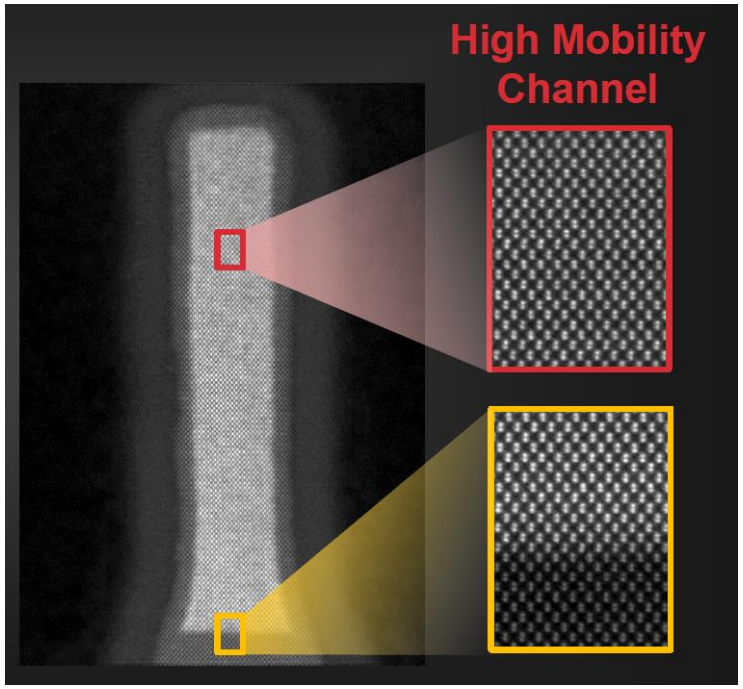
2007 APL



13 years

(2007-2020)

2021 TSMC ISSCC



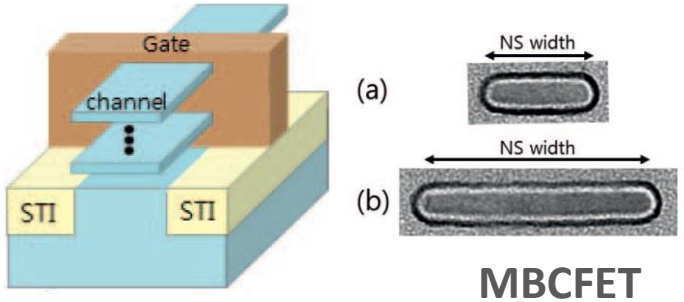
Mark Liu, Plenary Session 1.1, ISSCC 2021.

C.-Y. Peng, F. Yuan, C.-Y. Yu, P.-S. Kuo, M. H. Lee, S. Maikap, C.-H. Hsu, and C. W. Liu, Appl. Phys. Lett. 90, 012114 (2007) .(Cited No./Self Cited No.= 30/ 7)

- **$Si_{0.2}Ge_{0.8}$ channel with 1nm Si cap, having higher mobility(3X) than Si.**
- **It takes 13 years to commercialize HMC.**

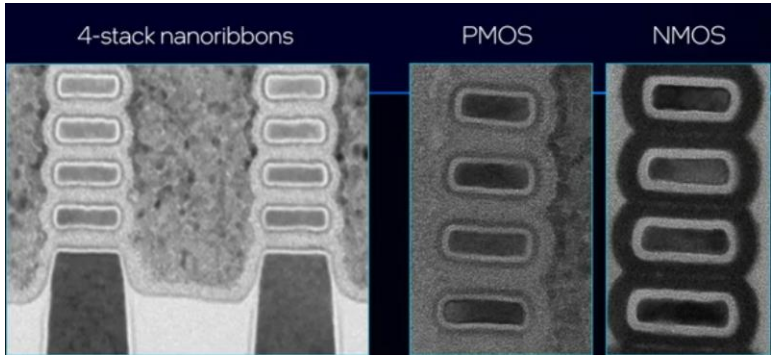
Status Quo of Industry for 3/2nm

2018 IEDM Samsung 3nm (?)



MBC: Multi-Bridge-Channel.

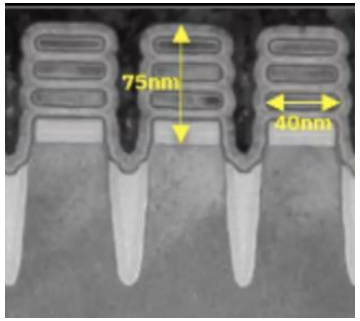
2024 Intel 20A (4)



RibbonFET, 4 stacked nanoribbons

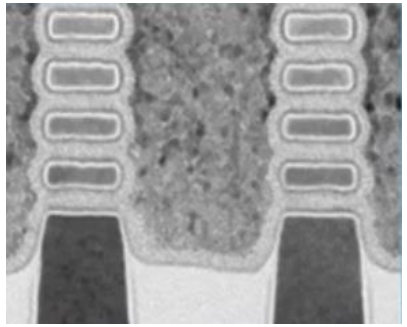
Ref: Intel Accelerated, July 26, 2021.

2021 IBM 2nm (3)



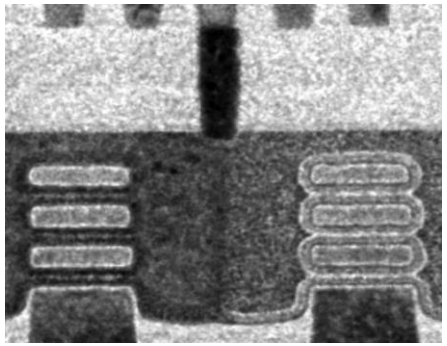
IBM 2nm technology node,
3 stacked nanosheets.

2025 Intel 18A (4)



4 stacked nanoribbons
(In early development)

2021 ISSCC TSMC 2nm (3)

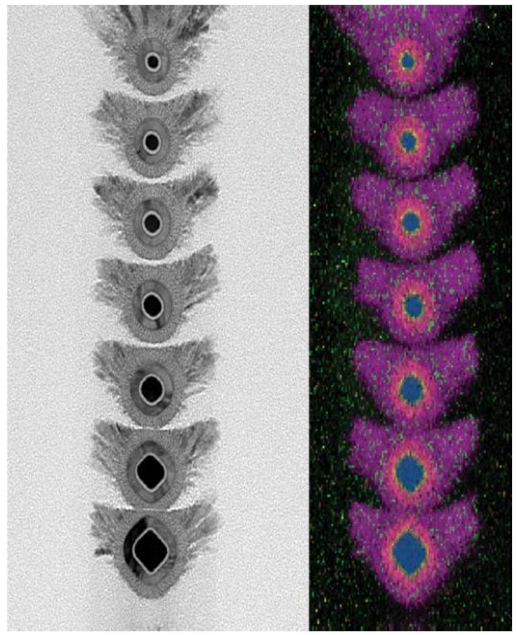


TSMC 2nm technology node,
3 stacked nanosheets.

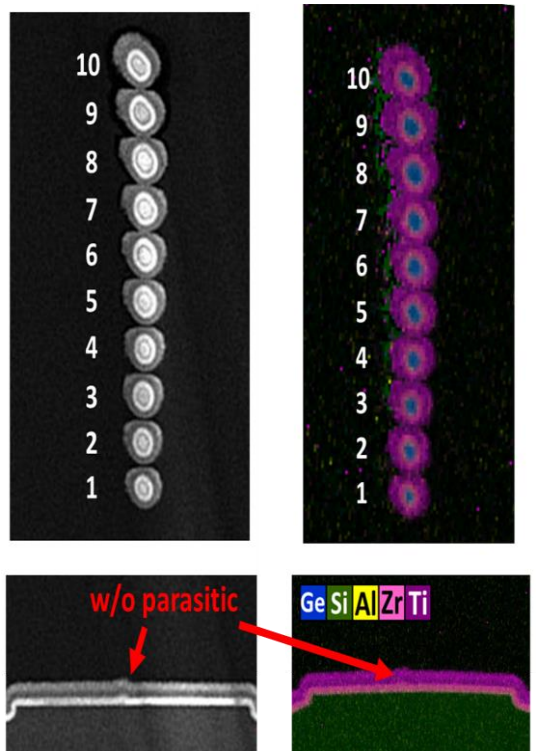
Mark Liu, Plenary Session 1.1, ISSCC 2021.

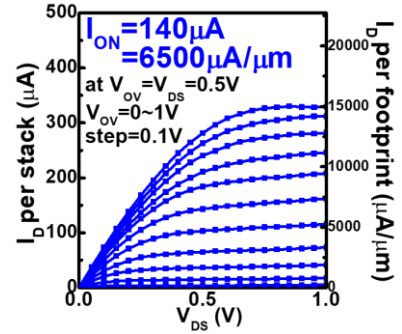
Post the 2021 Nature Electronics Research Highlight (July, 2021)/ VLSI 2021 highlight paper

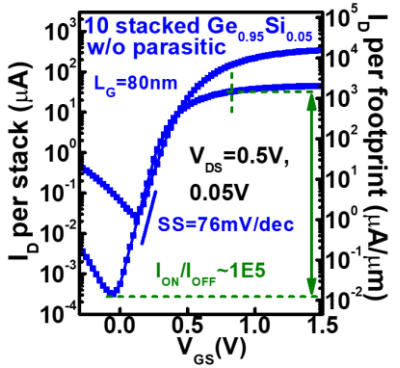
7 stacked GeSi nanowires



Nature Electronics, Vol. 4, July 2021, 452.



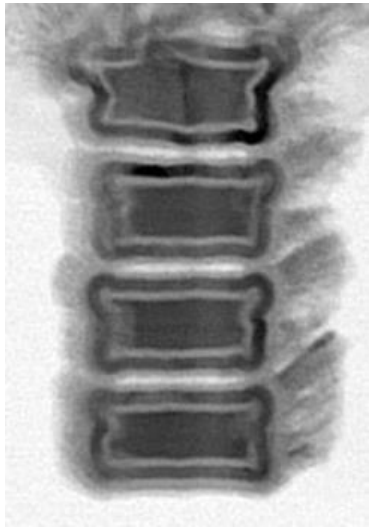




- **10 stacked $Ge_{0.95}Si_{0.05}$ nanowires without parasitic channels**
- **I_{ON} = 6500 μA/μm at V_{OV} = V_{DS} = 0.5V**
- **SS = 76 mV/dec and I_{ON}/I_{OFF}～1E5**

(Unpublished)

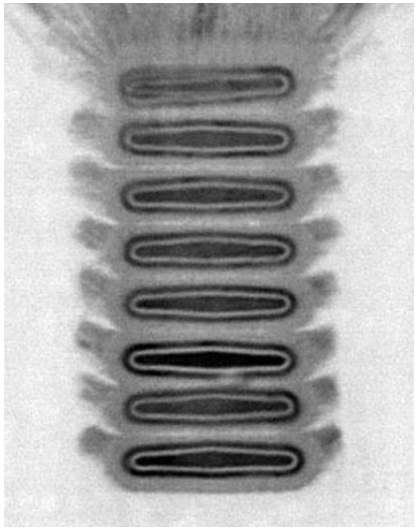
NTU 2020 IEDM 4 stacked GeSn



NTU 4 stacked nanosheets

Yu-Shiang Huang et al. and C. W. Liu, International Electron Devices Meeting (IEDM), 2020.

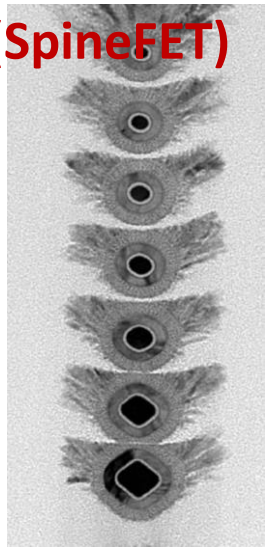
NTU 2021 VLSI 8 stacked GeSi



NTU 8 stacked nanosheets

Yi-Chun Liu et al. and C. W. Liu, Symposium on VLSI Technology (VLSI-Technology), 2021.

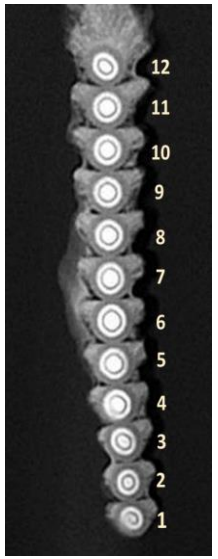
NTU 2021 7 stacked GeSi (SpineFET)



NTU 7 stacked nanowires

Yi-Chun Liu et al. and C. W. Liu, Symposium on VLSI Technology (VLSI-Technology), 2021.

12 stacked GeSi (SpineFET)

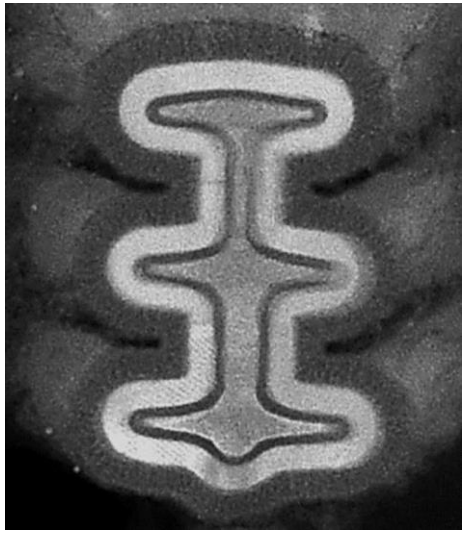


NTU 12 stacked nanowires

16 stacked GeSi (SpineFET)

NTU 16 stacked nanowires

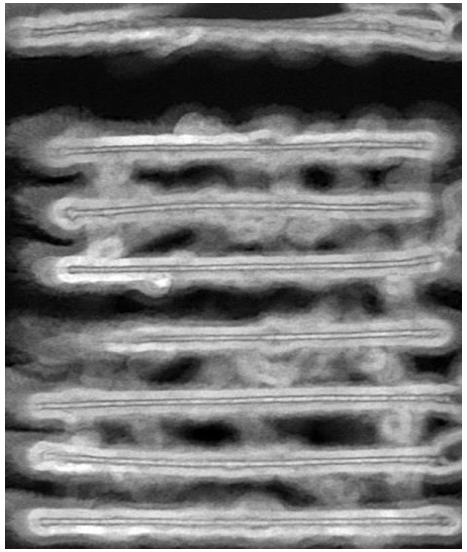
NTU 2021
3 stacked GeSi
{110} TreeFET (王)



NTU 3 stacked TreeFET

Chien-Te Tu et al. and C. W. Liu, EDL2022

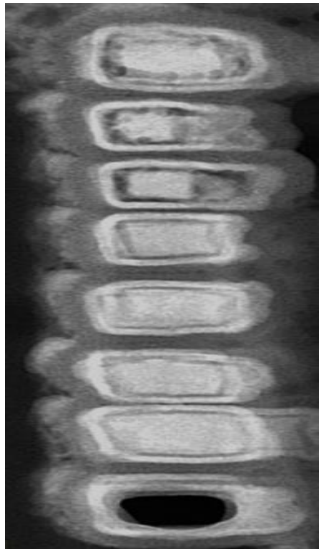
NTU 2021 (2D)
8 stacked GeSn
Ultrathin bodies



NTU 8 stacked ultrathin bodies

Chung-En Tsai et al. and C. W. Liu, International Electron Devices Meeting (IEDM), 2021.

NTU 2021
8 stacked GeSn
Nanosheets

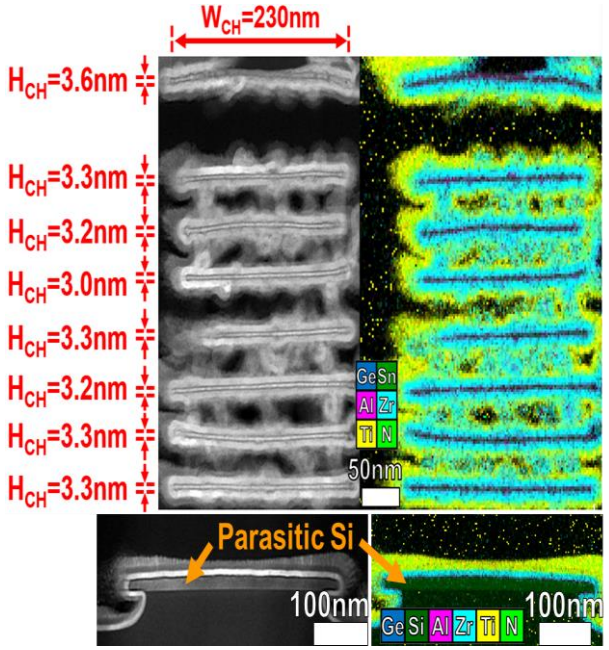


NTU 8 stacked nanosheets

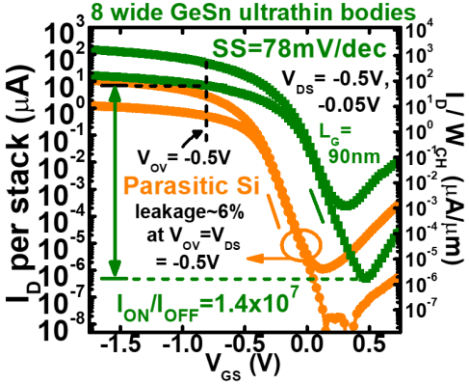
Chung-En Tsai et al. and C. W. Liu, International Electron Devices Meeting (IEDM), 2021.

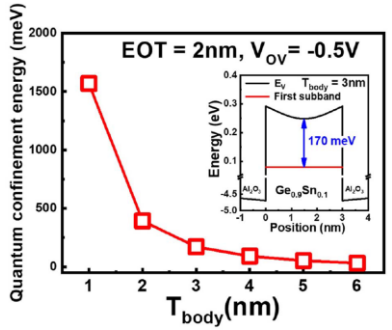
2021 IEDM Roger A. Haken Best Student Paper Award

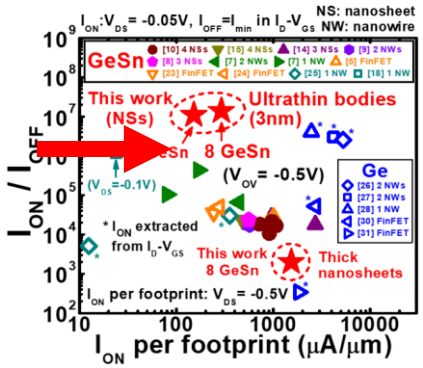
"Highly Stacked GeSn Nanosheets by CVD Epitaxy and Highly Selective Isotropic Dry Etching," IEEE Transactions on Electron Devices, 2022.

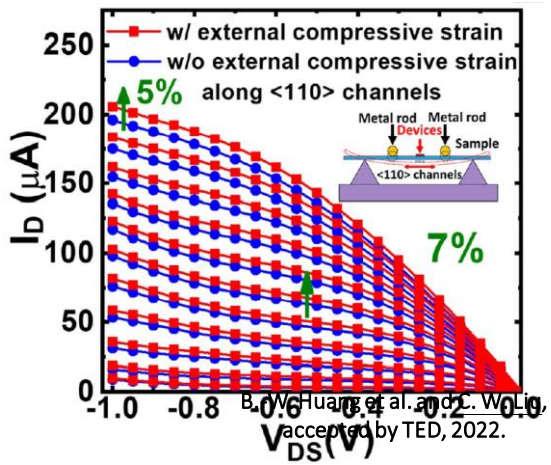


C.-E. Tsai et al. and C. W. Liu, IEDM, 2021.









B.-W. Huang et al. and C. W. Liu, accepted by TED, 2022.

- **The 8 stacked GeSn ultrathin bodies (~3nm) have record I_{ON}/I_{OFF} of $1.4x10^7$ at V_{DS}= -0.05V among GeSn/Ge 3D pFETs.**
- **T_{body} ↓ ➔ Quantum confinement energy ↑ ➔ I_{OFF} ↓**
- **Mechanical bending with external compressive strain ➔ I_{ON} ↑**

要教的學生

懂	⇒做(學以致用，**ideal case) Transistor**
不懂	⇒做(邊做邊學，**team work) MRAM**

用腦 : physics/design

用手: experiment/ technology/modules

手腦並用: integration /CTO/CEO

手腦都不用: investor/ entrepreneur

Student Awards: (In Chinese and English)

2022

- 指導學生李嘉洋 (Jia-Yang Lee) 獲得國立臺灣大學重點科技研究學院 (GSAT) 2022菁英博士生獎學金
- 指導學生Rachit Dobhalt獲得國立臺灣大學重點科技研究學院 (GSAT) 2022菁英博士生獎學金
- 指導學生周韜 (Tao Chou) 獲得國立臺灣大學重點科技研究學院 (GSAT) 2022菁英博士生獎學金
- 指導學生周韜 (Tao Chou) 獲得台積電2022年博士獎學金
- 指導學生鄭群議(Chun-Yi Cheng)獲得2022 VLSI-TSA (*International Symposium on VLSI Technology, Systems and Application*) 最佳學生論文獎(Best Student Paper Award)
- 指導學生劉亦浚(Yi-Chun Liu)獲得2022 SNDCT (*Symposium on Nano-Device Circuits and Technologies*) 學生論文競賽特優獎
- 指導學生鄒亞叡(Ya-Jui Tsou)獲得2022 SNDCT (*Symposium on Nano-Device Circuits and Technologies*) 學生論文競賽特優獎
- 指導學生蔡仲恩(Chung-En Tsai)獲得2022 SNDCT (*Symposium on Nano-Device Circuits and Technologies*) 學生論文競賽優等獎
- 指導學生杜建德(Chien-Te Tu)獲得2022 SNDCT (*Symposium on Nano-Device Circuits and Technologies*) 學生論文競賽優等獎
- 指導學生邱日照(Jih-Chao Chiu)獲得2022 SNDCT (*Symposium on Nano-Device Circuits and Technologies*) 學生論文競賽入圍獎
- 指導學生蔡仲恩(Chung-En Tsai) 獲得110學年度Dialog戴樂格半導體獎勵學生優良研究成果獎
- 指導學生鍾嘉哲(Chia-Che Chung) 獲得110學年度Dialog戴樂格半導體獎勵學生優良研究成果獎
- 指導學生杜建德(Chien-Te Tu) 獲得110學年度Dialog戴樂格半導體獎勵學生優良研究成果獎
- 指導學生林鑫成(Hsin-Cheng Lin) 獲得110學年度Dialog戴樂格半導體獎勵學生優良研究成果獎
- 指導學生陳韋任(Wei-Jen Chen) 獲得110學年度Dialog戴樂格半導體獎勵學生優良研究成果獎
- 指導學生黃柏崴(Bo-Wei Huang) 獲得110學年度Dialog戴樂格半導體獎勵學生優良研究成果獎
- 指導學生杜建德(Chien-Te Tu)獲得2022 TSIA(PhD student award)博士研究生半導體獎
- 指導學生葉俊宏(Chun-Hung Yeh)、李承澤(Cheng-Tse Lee) 獲得111年「臺大1975級電機系系友科技研究創新獎」
- 指導學生劉亦浚(Yi-Chun Liu)、鄭群議(Chun-Yi Cheng)、謝宛軒(Wan-Hsuan Hsieh) 獲得111年「臺大1975級電機系系友科技研究創新獎」
- 指導學生蔡仲恩(Chung-En Tsai)、鄭群議(Chun-Yi Cheng)、黃柏崴(Bo-Wei Huang) 獲得111年「臺大1975級電機系系友科技研究創新獎」

Student Awards: (In Chinese and English)

2021

- 指導學生蔡仲恩(Chung-En Tsai)獲得2021 IEDM (*International Electron Devices Meeting*)最佳學生論文獎(Best Student Paper Award)
- 指導學生邱日照(Jih-Chao Chiu)獲得2021 IEDMS (*International Electron Devices & Materials Symposium*)最佳論文獎(Best Paper Award)
- 指導學生林詩雅(Shih-Ya Lin)獲得1th SNDCT (*Symposium on Nano-Device Circuits and Technologies*)學生口頭論文簡報獎特優獎
- 指導學生鄒亞叡(Ya-Jui Tsou)獲得1th SNDCT (*Symposium on Nano-Device Circuits and Technologies*)學生口頭論文簡報獎入圍獎
- 指導學生邱日照(Jih-Chao Chiu)獲得1th SNDCT (*Symposium on Nano-Device Circuits and Technologies*)學生論文海報競賽獎入圍獎
- 指導學生林鑫成(Hsin-Cheng Lin) 獲得台積電2021年博士獎學金
- 指導學生陳韋任(Wei-Jen Chen) 獲得台積電2021年博士獎學金
- 指導學生黃柏崴(Bo-Wei Huang) 獲得台積電2021年博士獎學金
- 指導學生鍾嘉哲(Chia-Che Chung)獲得台積電2021實習競賽總決賽第三名(TSMC 2021 Intern Final Competition, 3rd place)。
- 指導學生鍾嘉哲(Chia-Che Chung)通過台積電2021 DTP部門實習競賽決賽(Top 7)。
- 指導學生林鑫成(Hsin-Cheng Lin)通過台積電2021 DTP部門實習競賽決賽(Top 7)。
- 指導學生李明軒(Ming-Xuan Lee)晉級台積電2021 PID部門實習競賽複賽
- 指導學生陳韋任(Wei-Jen Chen) 獲得臺大110年學士班學生論文優良獎 (NTU Bachelor Thesis Award)
- 指導學生黃柏崴(Bo-Wei Huang) 獲得臺大110年學士班學生論文院長獎 (NTU Bachelor Thesis Award)
- 指導學生黃柏崴(Bo-Wei Huang) 獲得2021臺大電機系大學部精專獎參獎(NTUEE Undergraduate Innovation Award, 3rd place)
- 指導學生鄒亞叡(Ya-Jui Tsou)獲得2021 TSIA(PhD student award)博士研究生半導體獎
- 指導學生蔡仲恩(Chung-En Tsai)獲得2021 TSIA(PhD student award)博士研究生半導體獎
- 指導學生黃郁翔(Yu-Shiang Huang) 獲得108學年度電子所最佳博士論文獎(Best Ph.D. thesis award)
- 指導學生鄒亞叡(Ya-Jui Tsou) 獲得110年「臺大1975級電機系系友科技研究創新獎」

IEDM Best Student Paper Award Winners (since 2012)

Year	Winner
2021	Chung-En Tsai, Yi-Chun Liu, Chien-Te Tu, Bo-Wei Huang, Sun-Rong Jan, Yu-Rui Chen, Jyun-Yan Chen, Shee-Jier Chueh, Chun-Yi Cheng, Chia-Jung Tsen, Yichen Ma, and C. W. Liu, "Highly Stacked 8 $Ge_{0.9}Sn_{0.1}$ Nanosheet pFETs with Ultrathin Bodies (~3nm) and Thick Bodies (~30nm) Featuring the Respective Record I_{ON}/I_{OFF} of $1.4x10^7$ and Record I_{ON} of 92μA at $V_{OV}=V_{DS}$= -0.5V by CVD Epitaxy and Dry Etching" (National Taiwan University)
2020	K. Sumita et al., "Subband Engineering by Combination of Channel Thickness Scaling and (111) Surface Orientation in InAs-On-Insulator nMOSFETs" (University of Tokyo)
2019	Markus Jech et al., "First-Principles Parameter-Free Modeling of n- and p-FET Hot-Carrier Degradation" (Technische Universitaat Wien)
2018	Wenjie Lu et al., "First Transistor Demonstration of Thermal Atomic Layer Etching: InGaAs FinFETs with sub-5 nm Fin-width Featuring in-situ ALE-ALD" (Massachusetts Institute of Technology)
2017	Felix Eltes et al., "A Novel 25 Gbps Electro-optic Pockels Modulator Integrated on an Advanced Si Photonic Platform" (IBM Research – Zurich)
2016	Roman Koerner et al., "The Zener-Emitter: A Novel Superluminescent Ge Optical Waveguide-Amplifier with 4.7 dB Gain at 92 mA Based on Free-Carrier Modulation by Direct Zener Tunneling Monolithically Integrated on Si" (University of Stuttgart/Philips U-L-M Photonics)
2015	Xiao Yu et al., "Experimental Study on Carrier Transport Properties in Extremely-Thin Body Ge-on-Insulator (GOI) p-MOSFETs with GOI Thickness down to 2nm" (The University of Tokyo)
2014	Jianqiang Lin et al., "Novel Intrinsic and Extrinsic Engineering for High-Performance High-Density Self-Aligned InGaAs MOSFETs: Precise Channel Thickness Control and Sub-40-nm Metal Contacts" (Massachusetts Institute of Technology)
2013	Umberto Celano et al., "Conductive-AFM Tomography for 3D Filament Observation in Resistive Switching, Devices" (IMEC)
2012	Han Wang et al., "Large-Scale 2D Electronics Based Single-Layer MoS2 Grown by Chemical Vapor Deposition" (Massachusetts Institute of Technology)

My honors with my students

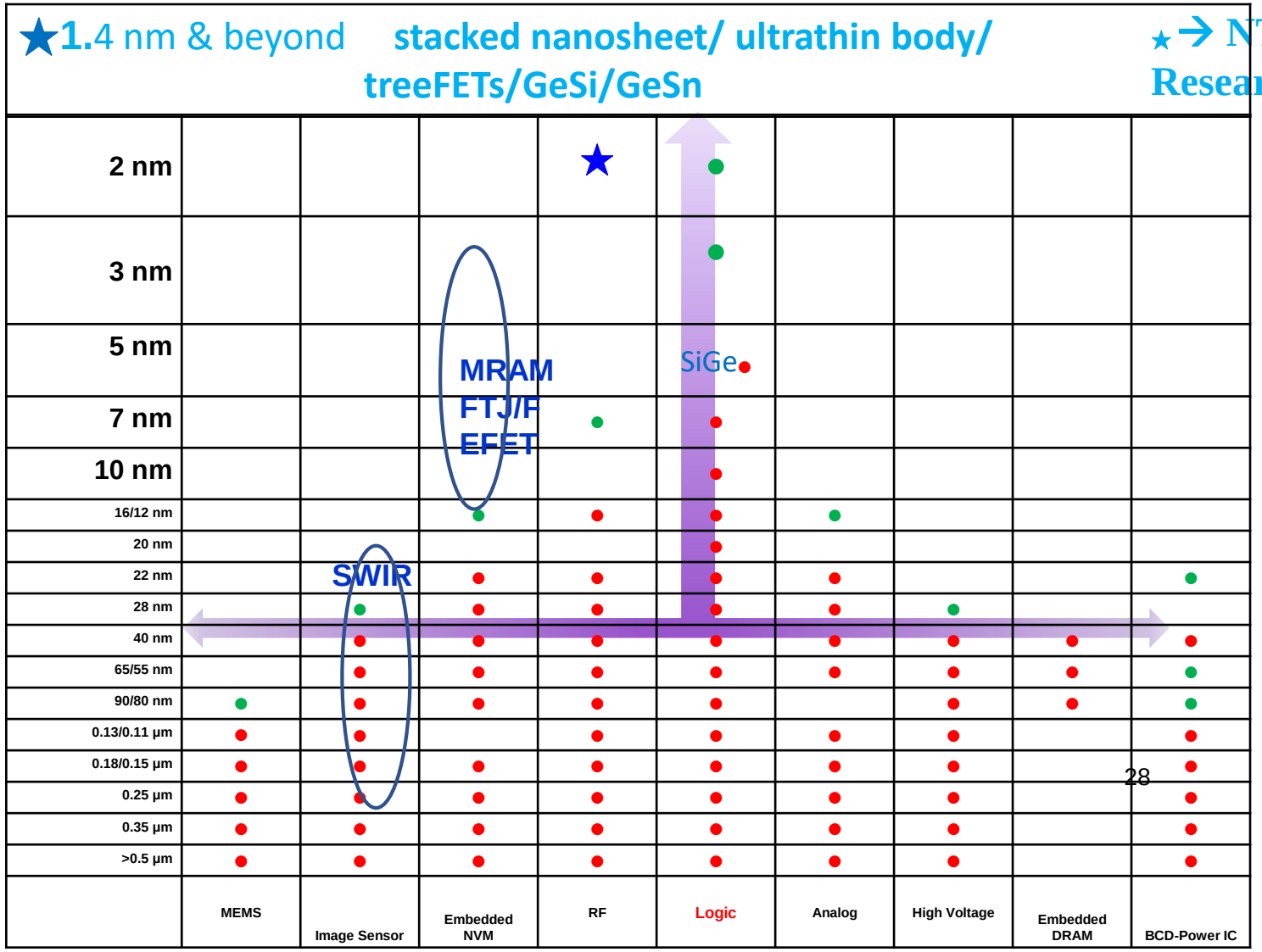
1. 2022 VLSI-TSA (*International Symposium on VLSI Technology, Systems and Application*) Best Student Paper Award (advisor)
2. 2021 International Electron Device Meeting (IEDM) Roger A. Haken Best Student Paper Award (advisor) IEDM Roger A. Haken Best Student Paper Award — IEDM (ieee-iedm.org)
3. 2021 Pan Wen Yuan Foundation Outstanding Research Award (潘文淵文教基金會研究傑出獎)
4. 2021 Best Paper Advisor Award, 1th SNDCT (*Symposium on Nano-Device Circuits and Technologies*)傑出論文指導教授獎
5. 2018 IEEE Fellow
6. 2018 Macronix Chair Professor (旺宏講座)
7. 2018 國立台灣大學特聘教授 (Distinguished Professor)
8. 2017 Micron Chair Professor (美光科技講座)

2021 4 VLSI +1IEDM
(2020 3 VLSI +IEDM)

- Chia-Che Chung, Bo-Wei Huang, Hsin-Cheng Lin, H. H. Lin, M.-T. Yang, Y. H. Hwang, Michael Huang, and **C. W. Liu**, "Thermal SPICE and Neural Networks with Physics Consistency to Simulate Complex FinFET Circuitry," ***Design Automation Conference (DAC) WIP Sessions, 2021*.**
- **(highlight paper)**Yi-Chun Liu, Chien-Te Tu, Chung-En Tsai, Yu-Rui Chen, Jyun-Yan Chen, Sun-Rong Jan, Bo-Wei Huang, Shee-Jier Chueh, Chia-Jung Tsen, and **C. W. Liu**, "First Highly Stacked $Ge_{0.95}Si_{0.05}$ nGAAFETs with Record I_{ON} = 110 µA (4100 µA/µm) at V_{OV}=V_{DS}=0.5V and High $G_{m,max}$ = 340 µS (13000 µS/µm) at V_{DS}=0.5V by Wet Etching," ***Symposia on VLSI Technology and Circuits (VLSI), 2021.***
- Chung-En Tsai, Yu-Rui Chen, Chien-Te Tu, Yi-Chun Liu, Jyun-Yan Chen, and **C. W. Liu**, "First Demonstration of Multi-V_T Stacked $Ge_{0.87}Sn_{0.13}$ Nanosheets by Dipole-Controlled ALD WN_xC_y Work Function Metal with Low Resistivity and Thermal Budget ≤ 400 ° C," ***Symposia on VLSI Technology and Circuits (VLSI), 2021.***
- **(highlight paper)**Ya-Jui Tsou, Kai-Shin Li, Jia-Min Shieh, Wei-Jen Chen, Hsiu-Chih Chen, Yi-Ju Chen, Cho-Lun Hsu, Yao-Min Huang, Fu-Kuo Hsueh, Wen-Hsien Huang, Wen-Kuan Yeh, Huan-Chi Shih, Pang-Chun Liu, **C. W. Liu**, Yu-Shen Yen, Chih-Huang Lai, Jeng-Hua Wei, Denny D. Tang, and Jack Yuan-Chen Sun, "First Demonstration of Interface-Enhanced SAF Enabling 400°C-Robust 42 nm p-SOT-MTJ Cells with STT-Assisted Field-Free Switching and Composite Channels," ***Symposia on VLSI Technology and Circuits (VLSI), 2021.***
- H.L. Chiang, J.F. Wang, T.C. Chen, T.W. Chiang, C. Bair, C.Y. Tan, L.J. Huang, H.W. Yang, J.H. Chuang, H.Y. Lee, K. Chiang,K.H. Sheng, Y.J. Lee, R. Wang, **C. W. Liu**, T. Wang, X. Bao, E. Wang, J. Cai, C.T. Lin, H. Chuang, H.S.P. Wong, M.F. Chang, "Cold MRAM as a Density Booster for Embedded NVM in Advanced Technology," ***Symposia on VLSI Technology and Circuits (VLSI), 2021.***

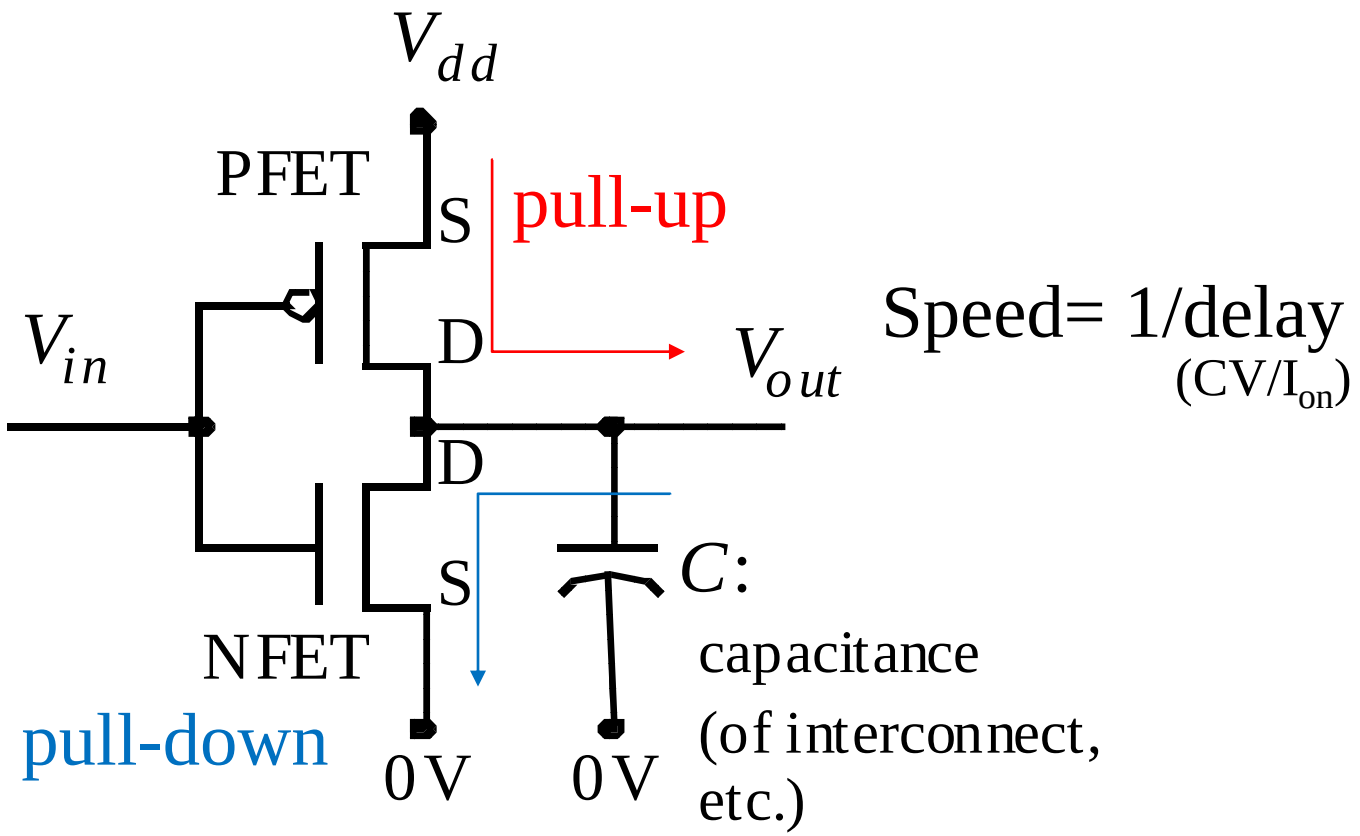
Tsmc Technology Portfolio

● → Available
● → In Development
★ → NTU Research



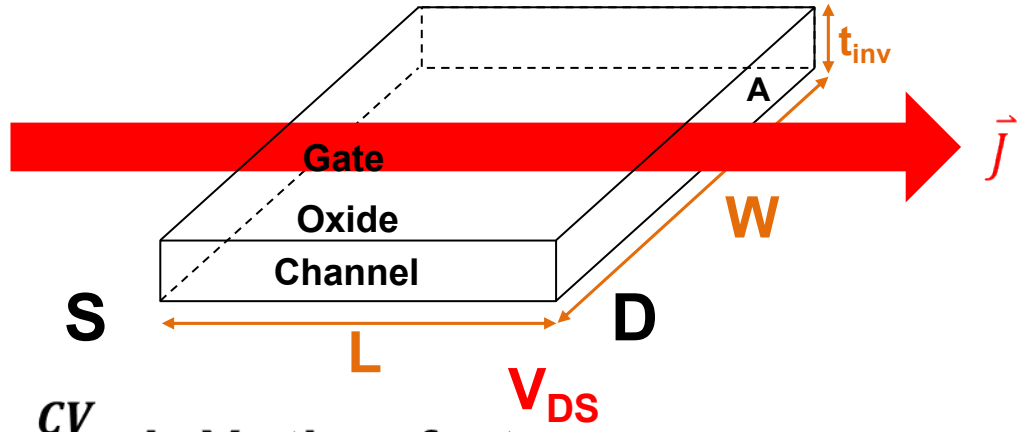
- More on Backend transistor (IGZO)/ Si photonics/ DRAM

CMOS (Complementary MOS) Inverter



A CMOS inverter is made of a PFET pull-up device and a NFET pull-down device. V_{out} = ? if V_{in} = 0 V.

CMOS current equation



- Speed = $\frac{1}{\tau}$, $\tau = \frac{CV}{I}$, I↑ V↓ then fast
- When $V_{DS} > V_G - V_T$:

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_T)^2 \times \text{stacking number(floor number)}$$

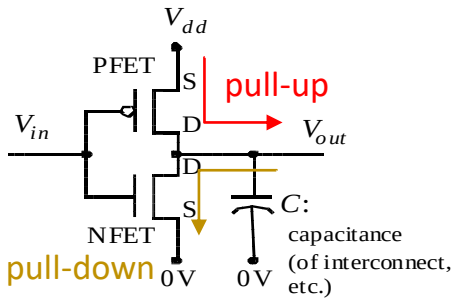
μ_n: High mobility 90nm

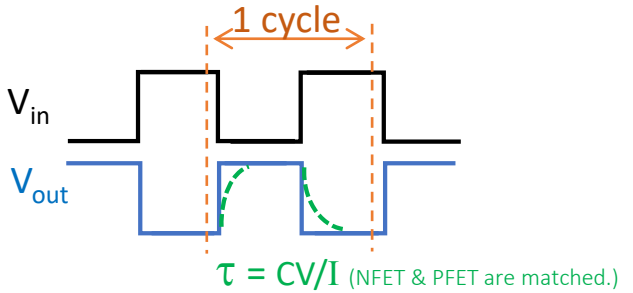
C_{ox}: HK material 45nm $\frac{\varepsilon_{ox}}{t_{ox}} = \frac{\varepsilon_{HK}}{t_{HK}} = \frac{\varepsilon_{ox}}{EOT}$

$\frac{W}{L}$: FinFET 16nm

stacking number(floor number): Nanosheet 2nm

CMOS (Complementary MOS) Inverter

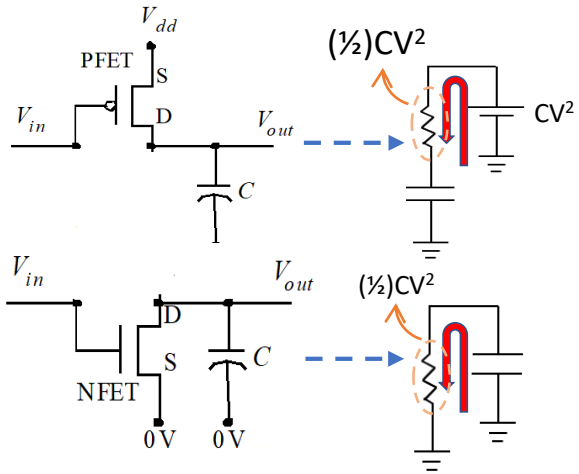




Speed= 1/delay

(CV/I_{on})

1 cycle:
H→L
:
(PFET turn on)



L→H :
(NFET turn on)

(½)CV² + (½)CV² =CV²

$$P_{dynamic} = (CV^2/T) = CV^2f$$

Modern Semiconductor Devices for Integrated Circuits (C. Hu)

A CMOS inverter is made of a PFET pull
NFET pull-down device. V_{out} = ? if V_{in} =

EE: Large I_{on} and small V_{dd}

- 要馬兒好又要馬兒不吃草

Let me know if you are interested in

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