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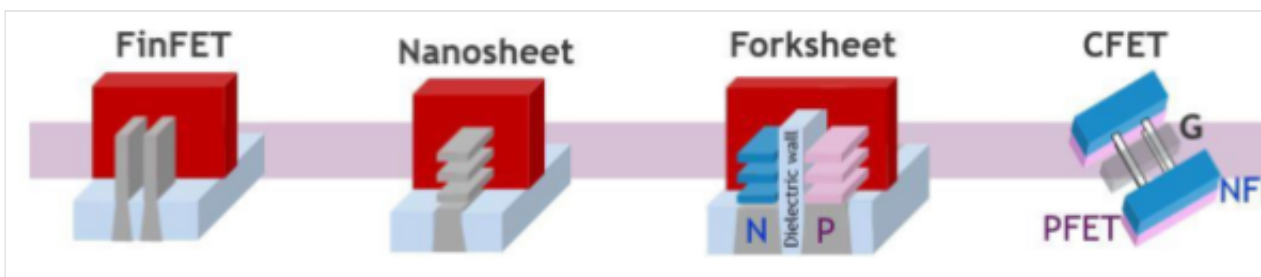
TSMC Commits to Nanosheet Technology at 2 nm Node

By [Alan Patterson < https://www.eetimes.com/author/alan-patterson/>](https://www.eetimes.com/author/alan-patterson/) 06.06.2022 2

Taiwan Semiconductor Manufacturing Co. (TSMC) has chosen nanosheet technology for production of its next 2 nm node starting in 2025 to help cut energy consumption in high-performance computing (HPC) systems.

The company will follow rivals Samsung and Intel, which plan to roll out their own nanosheet devices as early as this year.

TSMC briefed a handful of news media on its roadmap for the next few years as a preview for its annual technology symposium, which will be held at several global locations in the coming months. The world's leading chip foundry is evaluating other process technologies such as [complementary FET < https://www.eetimes.com/entering-the-nanosheet-transistor-era/2/>](https://www.eetimes.com/entering-the-nanosheet-transistor-era/2/) (CFET) to follow nanosheet, according to Kevin Zhang, TSMC vice president of Business Development.



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From FinFET to nanosheet to forksheet and finally to CFET. (Source: imec) (Click i to enlarge)

CFET is an evolution of nanosheet technology. Instead of stacking either n-type or p-type devices, it places both on top of each other to achieve higher transistor density. TSMC is searching for new transistor architectures that help reduce energy consumption in HPC applications, such as data centers, that are adding significantly to global warming.

“This (CFET) is still at the research phase,” Zhang told EE Times. “This is just one transistor option. I don’t think I can offer you a timeline for when this transistor technology will go into

production.”

Further along TSMC’s technology roadmap are new materials under research like tungsten disulfide. The material provides better conduction and more energy-efficient computation, Zhang said. Also under evaluation is carbon nanotube, a material that moves electrons more efficiently, he added.

“We believe all these new devices and materials will help us to move technology scaling forward,” Zhang said. Energy efficiency and low power consumption have “clearly” become the new benchmark for the future, he noted, as Moore’s Law wanes in significance.

The company will start production of its industry-leading 3 nm node later this year, which will mark the end of the FinFET process technology that provided TSMC a 90% share of the 5 nm business, [according to market research firm Gartner < https://www.eetimes.com/foundrys-31-growth-in-2021-outpaced-overall-chip-industry/>](https://www.eetimes.com/foundrys-31-growth-in-2021-outpaced-overall-chip-industry/). There will be an approximate three-year cadence between 3 nm and 2 nm.

“We do believe 3 nm will be a long node. We will continue to see high-volume demand on that node. But in terms of transition from 3 nm to 2 nm... nanosheet has a unique advantage in terms of further enhancing energy and computational efficiency because of the transistor architecture. We would expect customers with products that require more energy efficiency in terms of computational requirement, they will move to 2 nm first.”

Samsung will be the [first to introduce nanosheet technology < https://www.eetimes.com/samsung-profit-soars-on-memory-chip-demand/>](https://www.eetimes.com/samsung-profit-soars-on-memory-chip-demand/) in the second half of this year at the 3 nm node. That move may be premature, according to Bernstein analyst Mark Li.

“Samsung is the first and is adopting nanosheet now, but that on contrary has scared customers like Qualcomm and Nvidia away to TSMC as these customers worry about execution risks,” Li told EE Times. “Intel’s plan is also earlier than TSMC’s, probably by around one year, but again whether Intel can execute is a separate matter. Commercializing new tech with predictable quality, yield, and hence cost and volume requires a careful judgment on tech readiness and execution capabilities, and that is where TSMC really differentiates.”

Some TSMC customers may stay at 3 nm even longer just to try to harvest more technology benefits, Zhang explained. “3 nm and 2 nm will overlap [and] co-exist for quite some time,” he said.

Migrating foundry customers from FinFET to a new technology like nanosheet will be risky. TSMC has a track record that customers find reassuring, according to Matthew Bryson, senior vice president at Wedbush Securities.

“Recent history certainly favors TSMC, but at the same time, the competitive landscape has changed with Intel willing to invest significantly more than had been the case under the past few administrations and looking to lead with new technology,” Bryson said.

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Alan has worked as an electronics journalist in Asia for most of his career. In addition to EE Times, he has been a reporter and an editor for Bloomberg News and Dow Jones Newswires. He has lived for more than 30 years in Hong Kong and Taipei and has covered tech companies in the greater China region during that time.