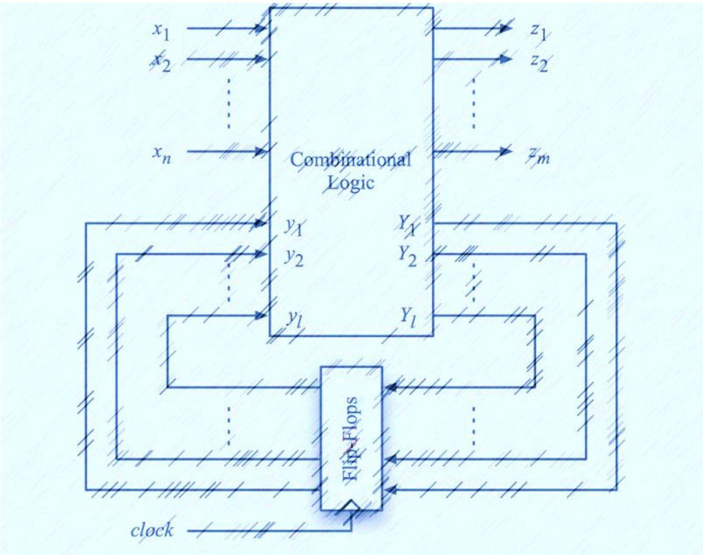
Sequential ATPG

- Introduction
- Time-frame expansion methods
- Simulation-based methods*
- Issues of Sequential ATPG* (not in exam)
- Conclusions



Issues of Sequential ATPG

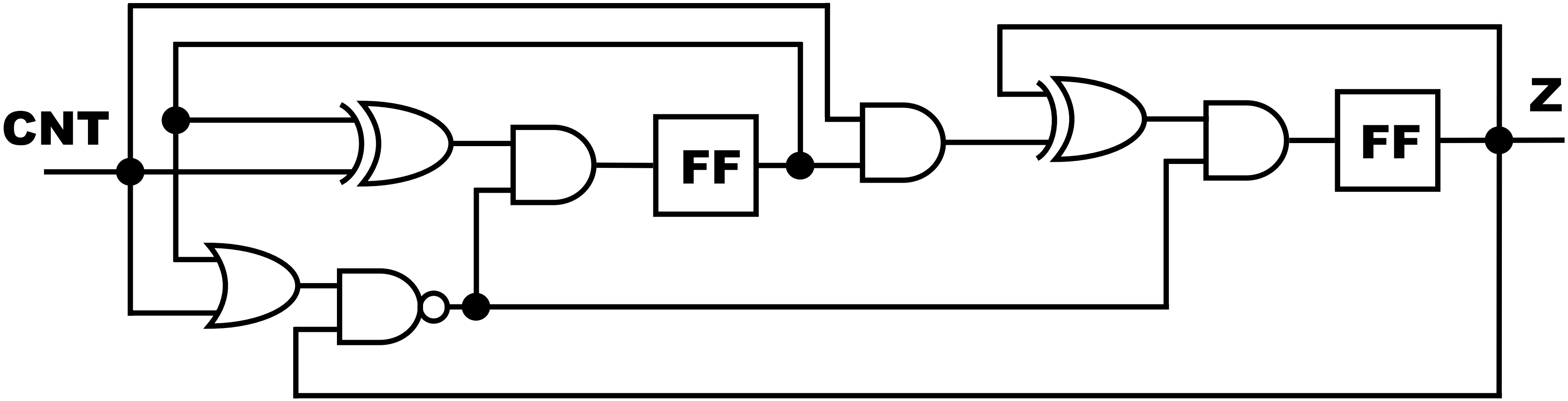
① Ckts. **without initialization** input

② **Potentially detected faults** can escape test

③ **Asynchronous** ckt. requires special attention

① Circuit w/o Initialization Input

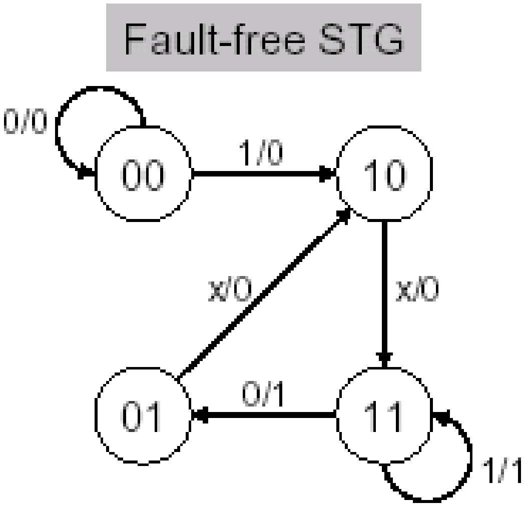
- Example
  - Mod 3 counter (BA Fig. 8.12)
    - 10→ 00→ 01→ 10 → …..

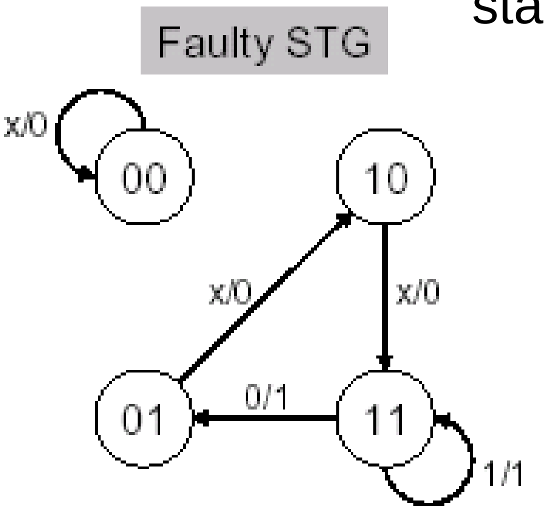


Cannot Find Initialization Sequence

② Potentially Detected Faults

- **DEF: faults that may or may not be detected**
  - Also see Video 5.7
- **Example: detection of fault depends on the power-up states**
  - $Y_1 = xy_1y_2+y_1y_2' + y_1'y_2$ $\underline{(+\ xy_1'y_2'\ )}$ <u>faulty STG missing term</u>
  - $Y_2 = y_1y_2+y_1y_2'$
  - $Z = y_1y_2$

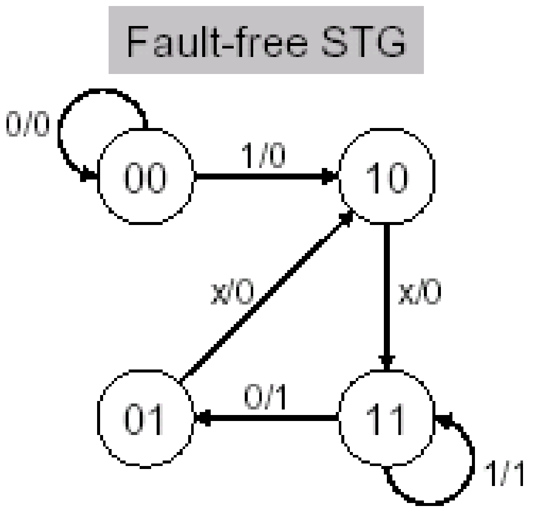




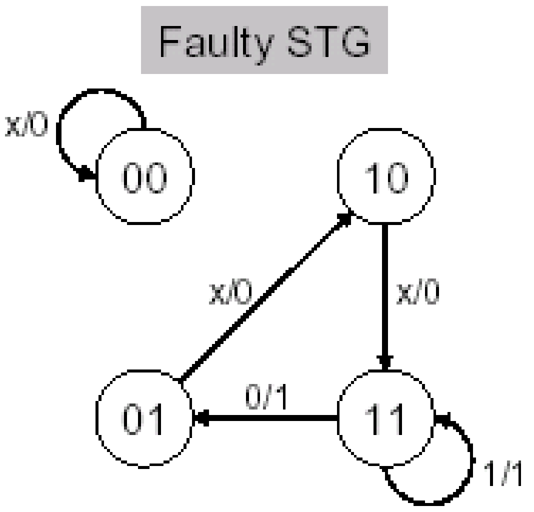
state transition graph

X/Z
(Input/output)
y1y2
(states)

Fault-free STG



Faulty STG



X/Z

- {0 1 1} initializes the circuit to state 11
- Good response to input {0110} is
  - z = 1001

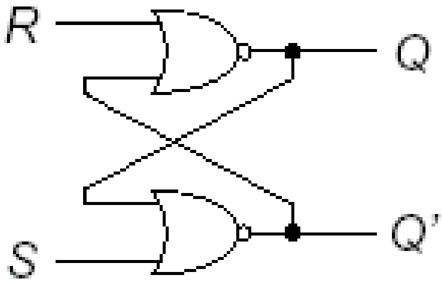
- {0 1 1} cannot initialize circuit
- Response at z to {0110}:
  - Power-up state 00,
    - z = 0000
    - fault detected
  - Power-up state 01,10, or 11
    - z = 1001
    - fault NOT detected

Fault Detection is Uncertain

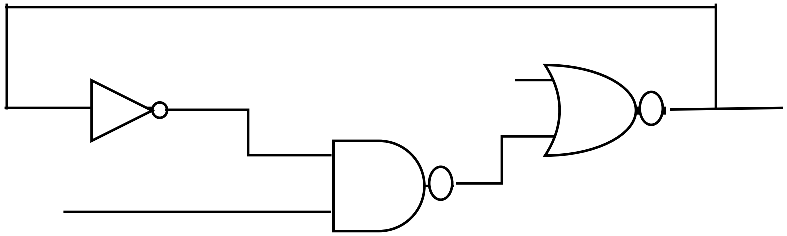
③ Asynchronous Circuits

- No explicit clock. Signals can change asynchronously
- Timing can be difficult to model
  - Test patterns generated may cause *races* and *hazards*
  - Need to verify test sequence with a fault simulator
- Example: Circuits with combinational loop

local feedback



global feedback



QUIZ

Q: Suppose you are a designer. Which of the following circuits you should avoid in order to avoid sequential ATPG?

A) Combinational circuits with feedback loops
B) Non-scan flip-flops without reset pins (video 11.8)
C) Circuits with many different types of flip-flops
D) Circuits with SRAM memories

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- **Issues of Sequential ATPG***
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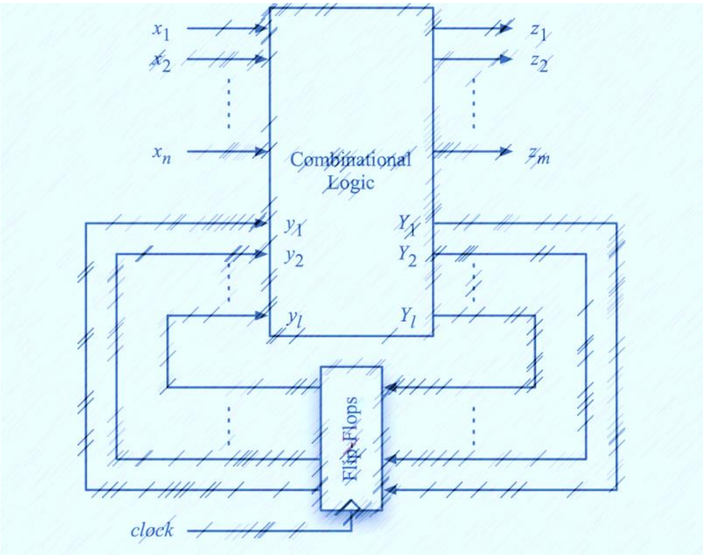

Concluding Remarks

- Sequential ATPG
  - Generate PI patterns, observe PO. No scan allowed
- Benefits
  - Enable at-speed testing
  - Handles partial scan or non-scan circuits
- Problems
  - Low fault coverage, long run time, large memory
- Techniques
  - Time frame expansion (EBT, BACK, Extended-D …)
  - Simulation (CONTEST)
- Current DFT & ATPG Practice
  - Use as much combinational ATPG as possible
  - Use sequential ATPG only when necessary

Sequential ATPG is Difficult. Need DfT! (Ch11)

References

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- [Cheng 88] Cheng, W-T. "The BACK algorithm for sequential test generation," Computer Design: VLSI in Computers and Processors, 1988. ICCD'88., Proceedings of the 1988 IEEE International Conference on. IEEE, 1988.
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- [Kubo 68] H. KUBO "A procedure for generating test sequences to detect sequential circuit failures," NEC Res. & Dev., (Oct. 1968), 69 –78.
- [Marlett 78] Marlett, Ralph A. "EBT: A comprehensive test generation technique for highly sequential circuits," Proceedings of the 15th Design Automation Conference. IEEE Press, 1978.
- [Muth 76] P. Muth"A nine-valued circuit model for test generation," IEEE Trans. Comput., 25 (6), pp. 630–636, 1976.
- [Huffman 53] D. A. Huffman, "The Synthesis of Sequential Switching Circuits," MIT Thesis, 1953.

Commercial Tools

- Mentor Graphics
  - Flextest
- Synoposys
  - Tetramax
- Syntest
  - turboscan

Academic Tools

- Time-Frame Expansion
  - ESSENTIAL [89]
  - FASTEST[89]
  - HITEC [Niermanh & Patel 91]
  - Lee-Reddy [91]
- Genetic Algorithm
  - CRIS [Saab & Abraham 96]
  - GATEST [Rudnick 97]
  - GATTO [96]
  - STRATEGATE [97]