

## Computer-Aided VLSI System Design

### Synthesis HW

**Due in one week**

#### Purpose

In this homework, please synthesize the color transform engine (CTE) that you designed for Verilog HW2.

#### Files needed

- check if you have these files

filename	Description
<i>HW4.pdf</i>	This document
<i>CTE.v</i>	Your Verilog HW2 design
<i>.synopsys_dc.setup</i>	DV setup file (copy from your Lab)
<i>testfixture1.v and testfixture2.v</i>	Testbench (copy from HW2)
<i>pattern_yuv.dat</i> <i>golden_rgb.dat</i> <i>pattern_rgb1.dat</i> <i>pattern_rgb2.dat</i> <i>pattern_rgb3.dat</i> <i>golden_yuv1.dat</i> <i>golden_yuv2.dat</i> <i>golden_yuv3.dat</i>	Test Pattern Files (copy from HW2)
<i>tsmc13.v</i>	Gate-level library for gate level simulation. You can link to the related path (~cvsd/tsmc13.v) to include this file.

Note: Include “tsmc13.v” to your testbench file (`include "tsmc13.v").

#### Problem

A) Please synthesize your Verilog HW2 design using the following environmental settings and constraints.

Tech Library                      ← TSMC0.13

Operating Conditions           ← typical

WireLoad                         ← ForQA

Constraint

Load                                ← 0.05, for all pins (except CLK)

Max area                         ← 0

Max fanout                       ← 8

Max transition  $\leftarrow 1$

#### TIMING

clk  $\leftarrow$  100 MHz, fix hold, and don't touch network

All input pins (except clk)  $\leftarrow$  2 ns input delay.

All output pins  $\leftarrow$  2 ns output delay.

Write your script file for 100 MHz synthesis. Then try to find the maximum frequency that your design can run ("can run" means "slack  $\geq 0$ ").

Write your gate-level netlist as "CTE\_syn.v" and your version 2.1 timing constraint file as "CTE.sdf" for online submission.

You can look over the timing and area reports of 100MHz and then try to find the maximum frequency of your design.

**B)** To verify your synthesized gate-level design is correct, please use the testbench from HW2 to run the simulation on both the RTL and gate-level designs. Use the verification flow like Fig. 1. Show that your synthesized design produces the same output as your RTL design. Please try both "testfixture1.v" and "testfixture2.v" and go through different test patterns.

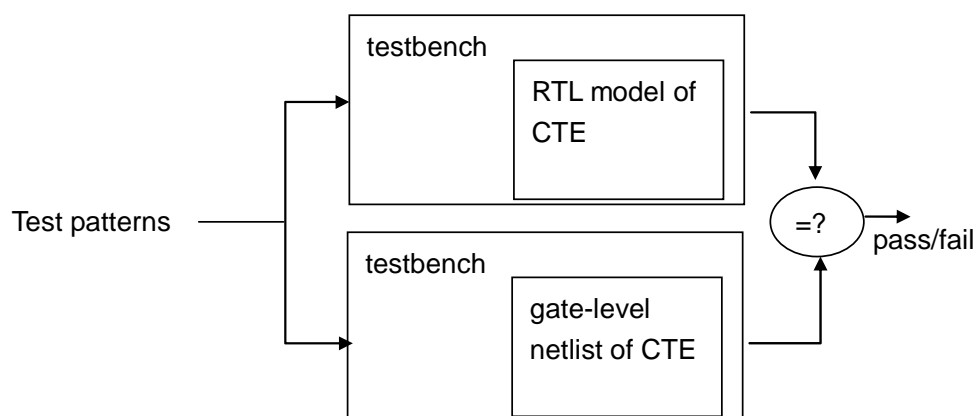


Figure 1. Verification of CTE controller

Note : For gate-level simulation, you may un-mark "`//initial $sdf_annotate ($SDFFILE, CTE);`" in your test bench to use timing information for simulation. Please use sdf 2.1 with file name "CTE.sdf"

#### Online submission:

Please submit a zipped file named *StudentID\_HW4.zip*, including

1. "CTE.v":

Your RTL design.

2. “CTE\_syn.v”:

Your verified gate-level CTE design running at 100MHz.

3. “CTE.sdf”:

Your 2.1 version sdf file.

4. “report.txt”:

Your report file summarizing timing, power, and area data after synthesis.