

# Introduction to Electronic Design Automation

Fall 2008  
National Taiwan University

## Problem Set 2

Due on 4/15/2011

Drop your solution in the instructor's mailbox in EE2 building by 17:00pm

### 1 [Cofactor]

[12 pt] Exercise 6.1.

(Chapter 6 available at

<http://cc.ee.ntu.edu.tw/~jhjiang/instruction/courses/spring11-eda/ls-handout.pdf>)

### 2 [Quantified Boolean Formulas]

[16 pt] For Boolean functions  $f$  and  $g$ , prove or disprove the following statements.

(a)

$$\neg(\exists x.f(x, y)) = \forall x.\neg f(x, y)$$

(b)

$$\forall x, \exists y. f(x, y, z) \Rightarrow \exists y, \forall x. f(x, y, z)$$

(c)

$$\exists x. (f(x, y) \wedge g(x, y)) \neq (\exists x. f(x, y)) \wedge (\exists x. g(x, y))$$

(d)

$$\neg\forall x, \exists z. (f(x, y) \wedge g(x, z)) = \exists x. (\neg f(x, y) \vee \forall z. \neg g(x, z))$$

### 3 [Binary Decision Diagrams]

[12 pt] Exercise 6.8.

### 4 [Circuit-to-CNF Conversion]

[12 pt] Exercise 6.10.

## 5 [Two-level Logic Minimization]

[20 pt] Let

$$\begin{aligned}F &= u'v'xy + u'v'w'y + u'vwy + uvw'y + uvxy + uv'wy, \\D &= u'vw'x'y + uvwx'y + vwy', \\R &= u'v'wx'y + u'vw'xy + uv'w'y + v'y' + w'y',\end{aligned}$$

be the onset, don't-care set, and offset of an incompletely specified function, respectively. Use Quine-McCluskey's method to minimize it in the following steps.

- (a) Generate all prime implicants, and list the Boolean matrix.
- (b) Which prime implicants are essential? Reduce the Boolean matrix based on the prime implicants.
- (c) Reduce iteratively the Boolean matrix using row equality, row dominance, column dominance, and induced  $n$ -ary essential primes until no more reduction is possible. Show intermediate steps.
- (d) Solve the cyclic core, if any, using the independent set heuristic algorithm.

## 6 [Technology Mapping]

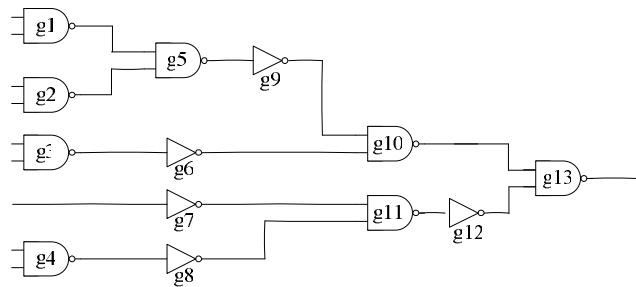
[14 pt]

- (a) Given the subject graph and pattern graphs of Figure 1, apply the DAGON mapping algorithm to find a min-area cover. Show all the optimal costs with their corresponding cell names at every node, and identify the final optimum cover.
- (b) Apply inverter-pair insertion to improve the above technology mapping. Show all the optimal costs with their corresponding cell names at every node, and identify the final optimum cover.

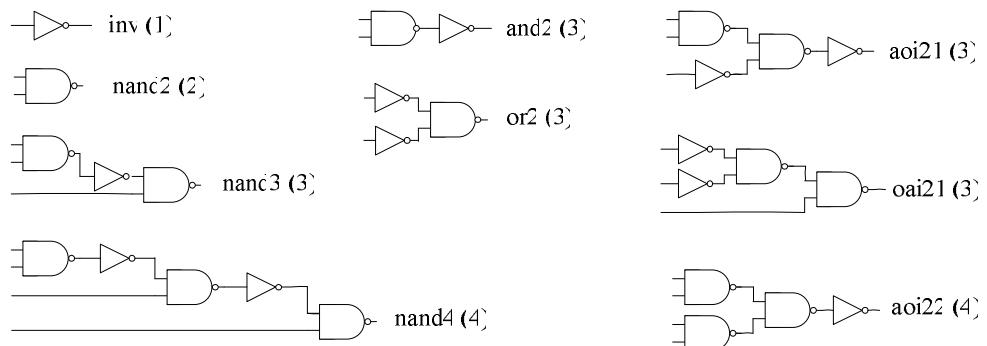
## 7 [Static Timing Analysis]

[14 pt]

- (a) Compute the arrival time, required time, and slack of each node in the netlist of Figure 2. Assume that the arrival time of every primary input is 0, and the required time of every primary output is 8ns.
- (b) Show that the most critical region (with the least slack) must consist of a set of thorough paths from primary inputs to primary outputs.

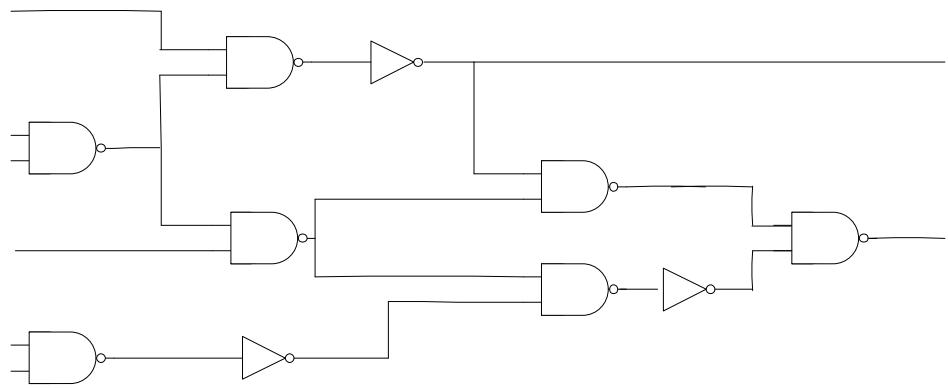


Subject Graph



Pattern Graphs

**Fig. 1.** Subject graph and pattern graphs for technology mapping. The area costs of the pattern graphs are in the parentheses.



**Fig. 2.** A circuit under static timing analysis, where NAND2 and INV are of gate delays 2ns and 1ns, respectively.