Introduction to Electronic Design Automation

Spring 2011
National Taiwan University

Problem Set 3

Due on 05/24/2011 before lecture

1 [BDD Operation]

[10%] Consider the ROBDD AND operation of two functions f and g. Show a family of f and g functions whose ROBDD AND operation is of complexity $O(|F| \cdot |G|)$, for F and G being the ROBDDs of f and g, respectively.

2 [BDD ITE]

[15%] Let

$$f = a(\neg b + c)(\neg c + d) + \neg ac + bd, \text{ and}$$
$$g = \neg b \neg c + \neg bd + \neg c \neg d.$$

(a) Draw the *shared* ROBDDs of functions f and g, respectively, with variable ordering $a < b < c < d$, that is, a on top and d at bottom.
(b) Compute the ROBDD H of $h = f \oplus g$ using the recursive ITE operation.
(c) Compute the ROBDD of $f(g(b, c, d), b, c, d)$ using the recursive ITE operation.

3 [SAT Solving]

[15%] Given the CNF formula

$$(a+\neg b+c)(a+b+\neg c)(\neg a+b+\neg c)(a+b+c)(\neg a+c+d)(\neg a+c+\neg d)(\neg b+\neg c+\neg d)(a+\neg b+\neg c),$$

apply the following decision procedures for SAT solving

(a) exhaustive search,
(b) exhaustive search with implication, and
(c) exhaustive search with implication and conflict-based learning,

with decision precedence $a > b > c > d$ and assignment precedence false > true. Show intermediate steps with decision trees, implication graphs, and/or learned clauses.

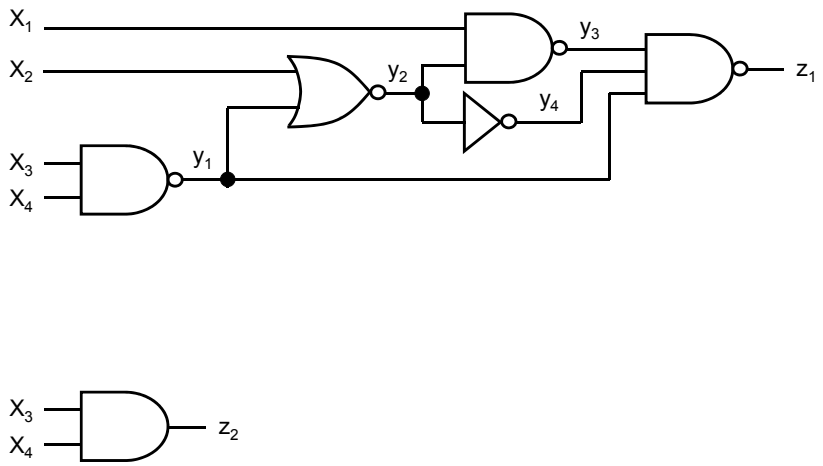

Fig. 1. Two netlists under combinational equivalence checking.

4 [Combinational Equivalence Checking]

[20%] Given two circuits as shown in Figure 1, apply combinational equivalence checking on them. Build the miter structure and translate the equivalence checking problem to a satisfiability problem. Write the CNF formula in the DIMACS format[1]. (Note that you may need to rename the signals as numbers to fit the DIMACS CNF format.) Run a SAT solver on your .cnf file. Print out your .cnf file and the SAT result. (A solver is downloadable, e.g., from `http://minisat.se/`.)

5 [Reachability]

[15%] Given two finite state machines (FSMs) M_1 and M_2, let their product machine be $M_{1\times 2}$. Assume the reachable state sets of M_1, M_2, and $M_{1\times 2}$ be R_1, R_2, and $R_{1\times 2}$, respectively.

[1] **DIMACS CNF format** is widely accepted as the standard format for Boolean formulas in CNF. Benchmarks listed on satlib.org, for instance, are in the DIMACS CNF format.

An input file starts with comments (each line starts with "c"). The number of variables and the number of clauses is defined by the line:

```
p cnf #variables #clauses
```

Each of the next lines specifies a clause: a positive literal is denoted by the corresponding number, and a negative literal is denoted by the corresponding negative number. The last number in a line should be zero. For example,

```
c A sample .cnf file.
p cnf 3 2
1 -3 0
2 3 -1 0
```

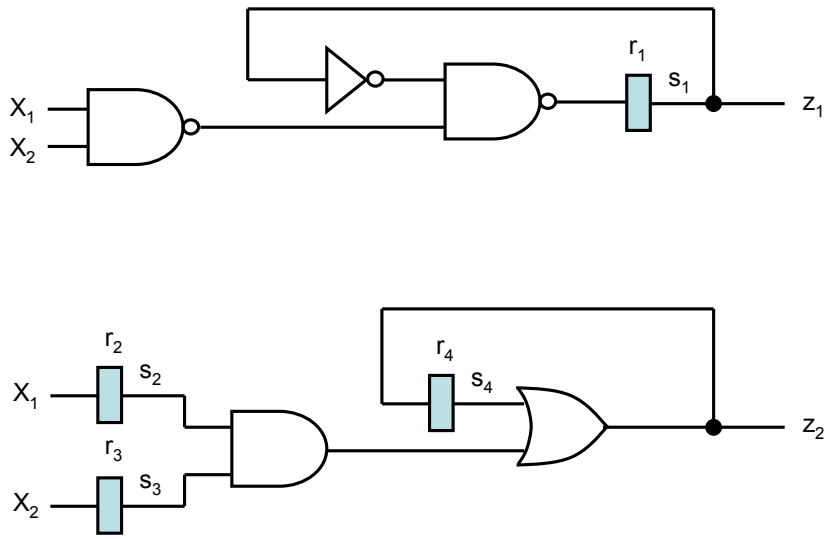

Fig. 2. Two netlists under sequential equivalence checking.

(a) Show by examples of M_1 and M_2 such that $R_{1\times 2} \subset R_1 \times R_2$.
(b) Show by examples of M_1 and M_2 such that $R_{1\times 2} = R_1 \times R_2$.
(c) Is $R_1 \times R_2 \subset R_{1\times 2}$ possible? Why or why not?

6 [Sequential Equivalence Checking]

[25%] Given two sequential circuits C_1 and C_2 of Figure 2, perform sequential equivalence checking with the following steps.

(a) Write down the transition functions and output functions of C_1 and C_2. Suppose all the registers are of initial value 0; write down the characteristic functions of the initial states of C_1 and C_2.
(b) What are the transition and output functions of the product machine $C_{1\times 2}$ of C_1 and C_2? What is the initial state of $C_{1\times 2}$?
(c) Write down the Boolean expression for the transition relation T of $C_{1\times 2}$.
(d) Perform reachability analysis using transition relation T and write down the reached state set in every iteration (in a characteristic function). What is the reachable state space of $C_{1\times 2}$ (in a characteristic function)?
(e) Conclude the equivalence between C_1 and C_2 using the information of reachable states.