Introduction to Electronic Design Automation

Spring 2014
National Taiwan University

Problem Set 2

Due on 2014/04/23
Please drop your solution in the instructor's mail box at EE2 building by 18:00

1 [Cofactor]

[10%] Exercise 6.1.

(Chapter 6 available on course webpage)

2 [Quantified Boolean Formulas]

[15%] Given two arbitrary Boolean functions f and g, please justify which directions ($\Leftarrow$, $\Rightarrow$, or both) of the following arrows $\Leftrightarrow$ hold generally.

(a)

$$\forall x, \exists y. f(x, y, z) \Leftrightarrow \exists y, \forall x. f(x, y, z)$$

(b)

$$\exists x. (f(x, y) \rightarrow g(y, z)) \Leftrightarrow (\forall x. f(x, y)) \rightarrow g(y, z)$$

(c)

$$\exists x. (f(x, y) \vee g(x, y)) \Leftrightarrow (\exists x. f(x, y)) \vee (\exists z. g(z, y))$$

(d)

$$\exists x, \forall y. (f(x, y) \wedge g(x, y)) \Leftrightarrow (\exists x, \forall y. f(x, y) \wedge \exists x, \forall y. g(x, y))$$

(e)

$$\neg(\forall x, \exists y. (\neg f(x, y, z) \vee g(x, y, z))) \Leftrightarrow \exists x, \forall y. (f(x, y, z) \wedge \neg g(x, y, z))$$

3 [Application of Quantified Boolean Formula]

[15%] Exercise 6.5.

4 [Binary Decision Diagrams]

[15%] Exercise 6.8.

5 [Two-level Logic Minimization]

[15%] Given an incompletely specified function over variables a, b, c, d, e, f with onset minterms

$$\{000001, 000111, 001011, 001100, 001111, 100001,$$
$$100011, 101011, 101111, 111011, 111100\}$$

and don't care set minterms

$$\{011110, 110010, 110110, 111010\},$$

apply the Quine-McCluskey procedure to minimize it. Identify all essential prime implicants and find all minimum sum-of-products expressions. Show intermediate results of your derivation.

6 [Static Timing Analysis]

[20%] Consider the circuit of Figure 1 for timing analysis.

(a) (5%) Find all possible topological orders of the logic gates.
(b) (10%) Compute the *arrival time*, *required time*, and *slack* of every net. Assume the required times for the primary outputs are 9 ns. Identify critical path(s) with slacks ≤ 1 ns.
(c) (5%) Given a sequential circuit for static timing analysis, how do you determine the arrival time and required time at the output and input of a register, respectively?

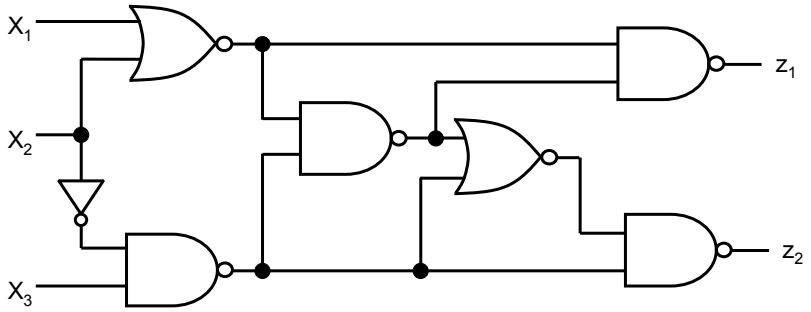

Fig. 1. A circuit under timing analysis. Assume the arrival times for all of the primary inputs are 0, the gate delay of an inverter is 1ns, a NAND gate is 2ns, and the gate delay of a NOR gate is 3ns.)

7 [Technology Mapping]

[10%] Given the subject graph and pattern graphs of Figures 2 and 3, respectively, apply the DAGON mapping algorithm to find a min-area cover. Show all the optimal costs with their corresponding cell names at every node, and identify the final optimum cover.

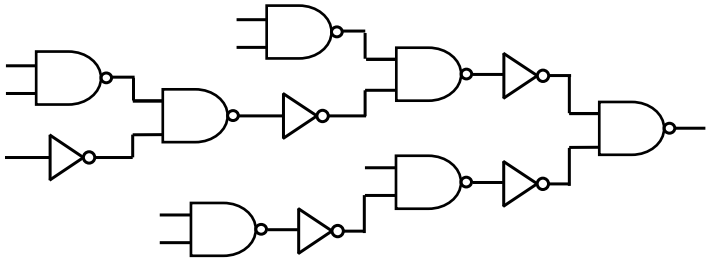

Fig. 2. Subject graph

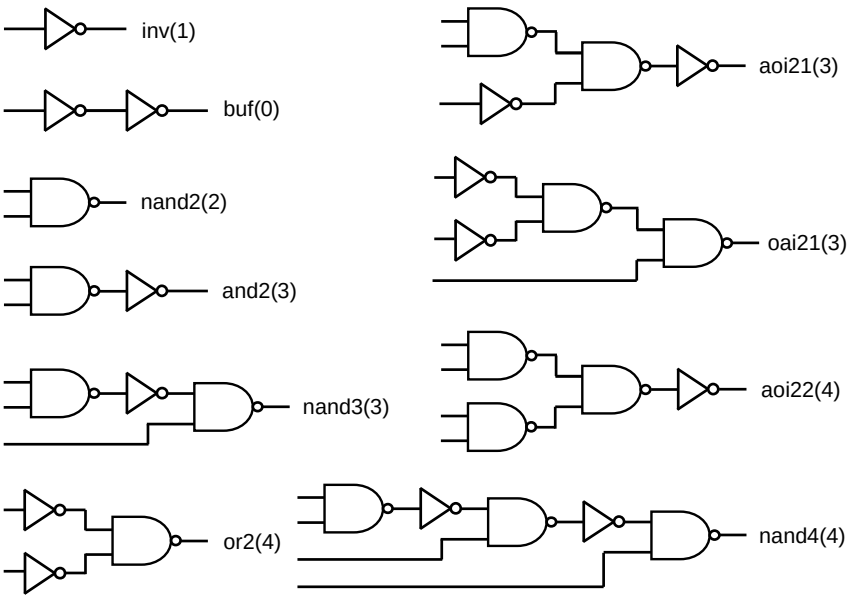

Fig. 3. Pattern graphs.