Clock and Data Recovery

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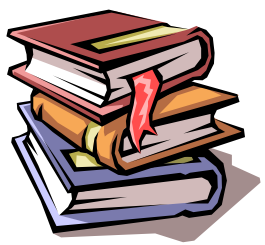

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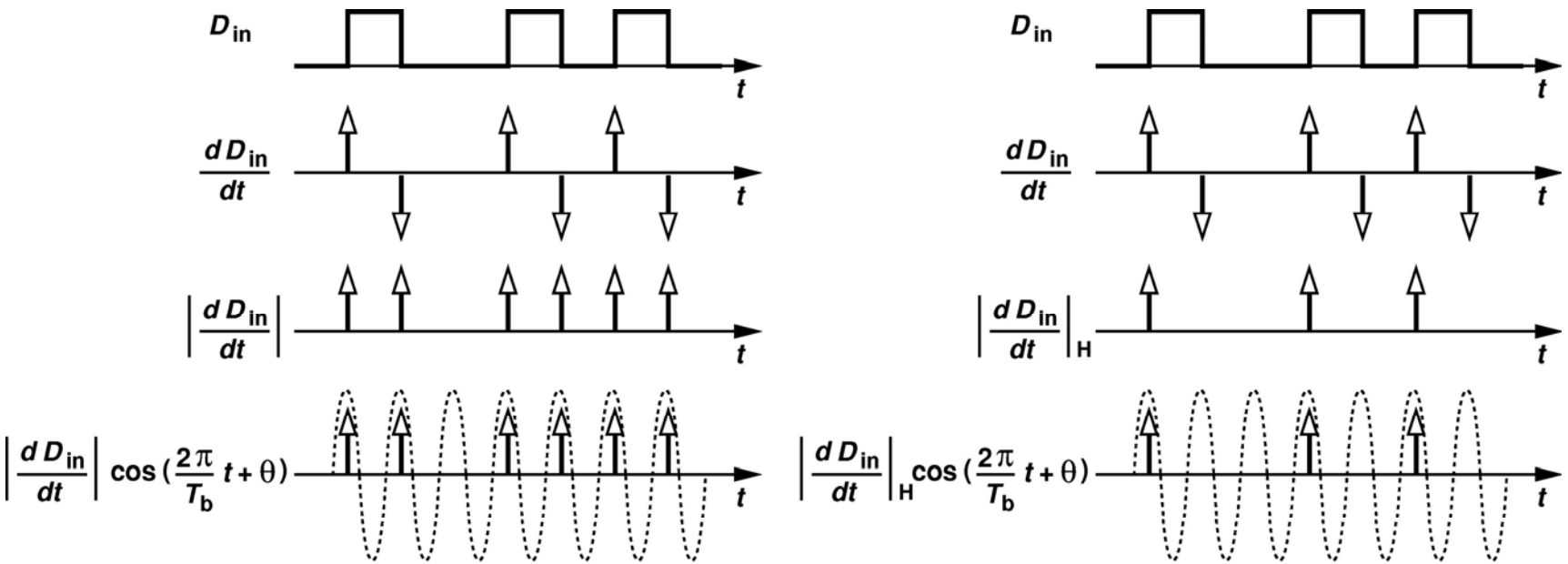
Outline

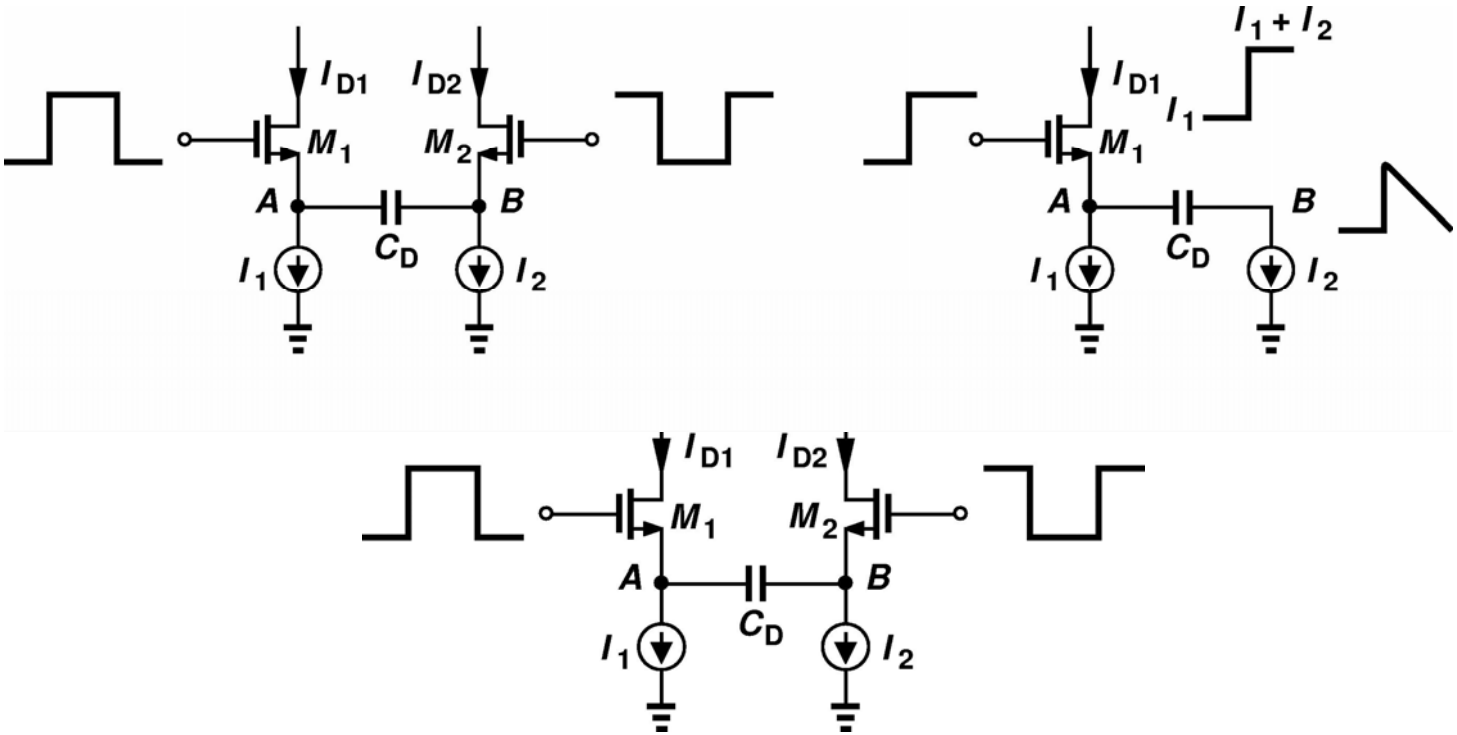
- General Considerations
- Linear Phase Detector
- Binary Phase Detector
- CDR Architecture

Edge Detection

- Extracting clock from NRZ data is not trivial at all, since its spectrum contains no power at the frequency of data rate.
- A circuit detecting the data transition is essential for clock recovery.

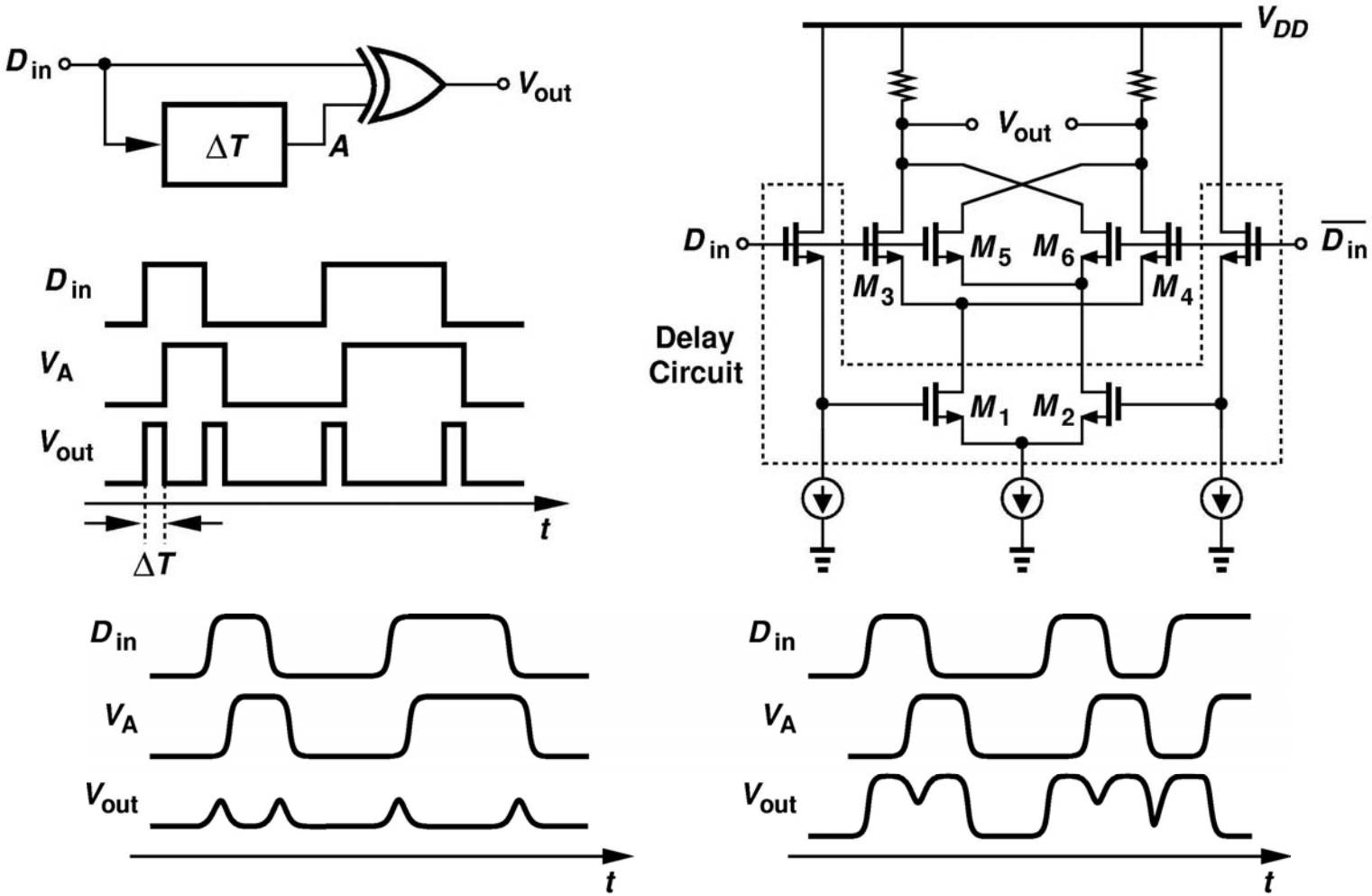


CMOS Realization of Edge Detectors



- Gilbert cell with capacitive degeneration may achieve differentiation and rectification at high speed.

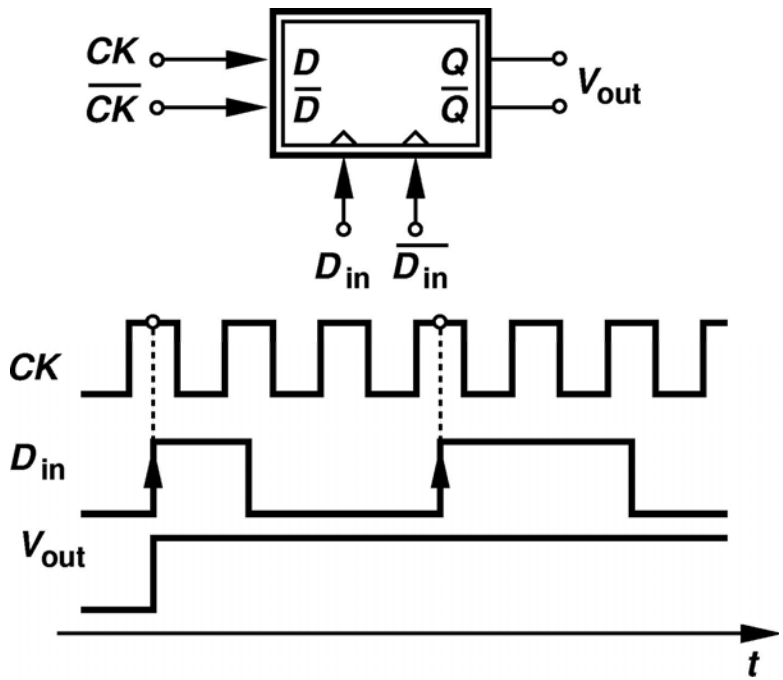
Alternative Solution for Edge Detection

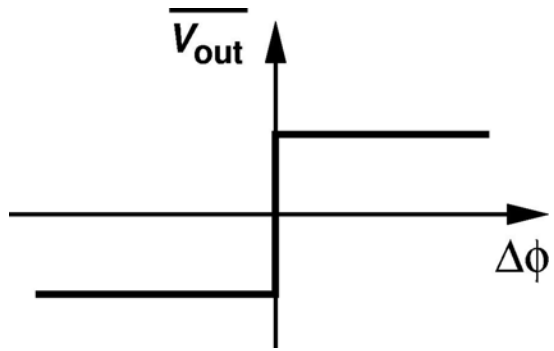


- Proper delay must be set to obtain clear pulses.
- PVT variation matters.

Phase Detection

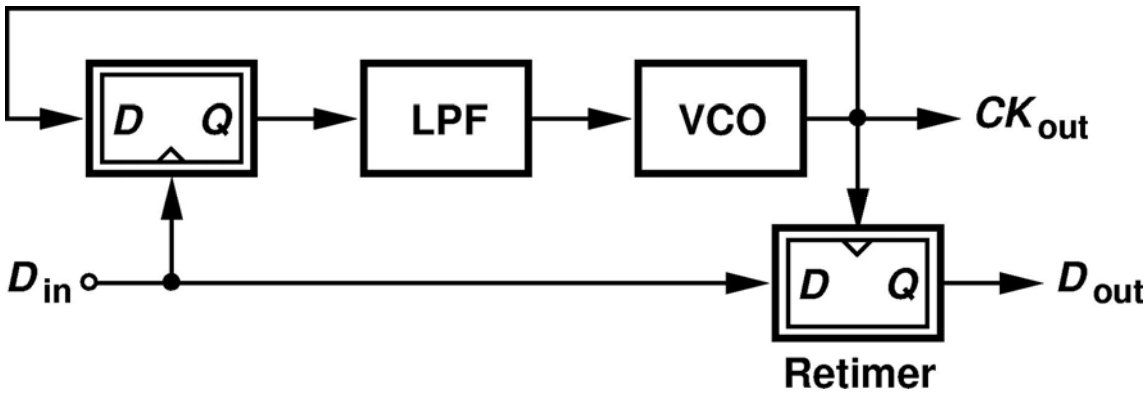
- A more efficient way is to detect the data transition and determine whether it is early or late with respect to its corresponding clock phase.





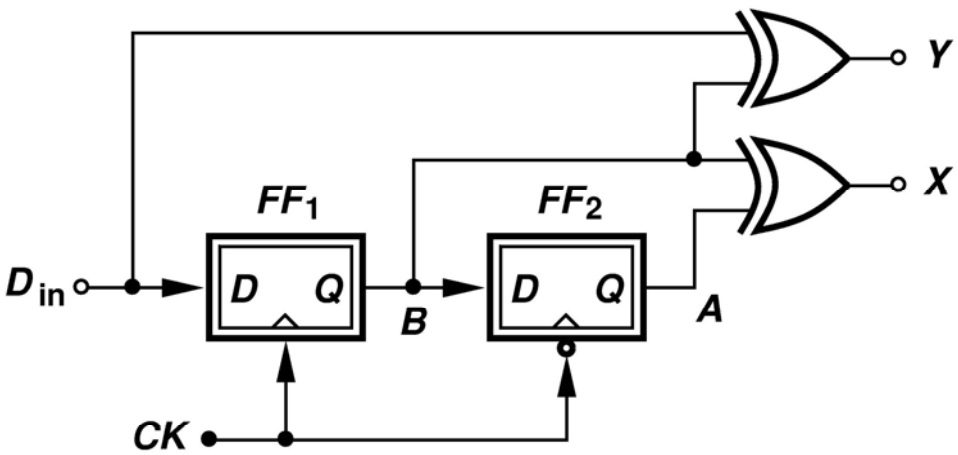
- Finite acquisition range (Why?)
- Binary characteristic

Simple CDR with Single-FF Phase Detector

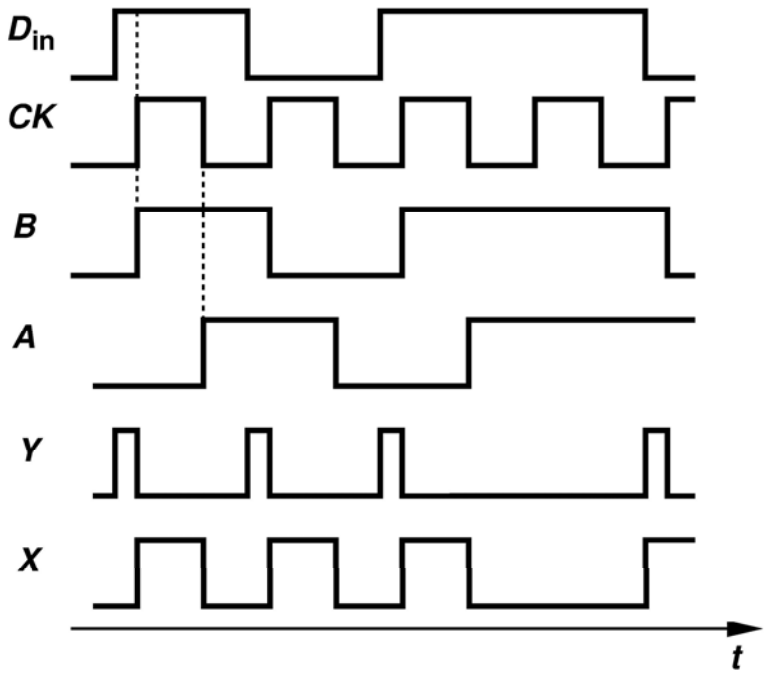


- **Drawbacks:**
  - **Continue to increase or decrease the VCO control voltage even when no data edge is present $\Rightarrow$ large jitter.**
  - **Large skews may cause improper sampling.**
  - **Finite capture range (lack of frequency acquisition loop).**

Hogge Phase Detector

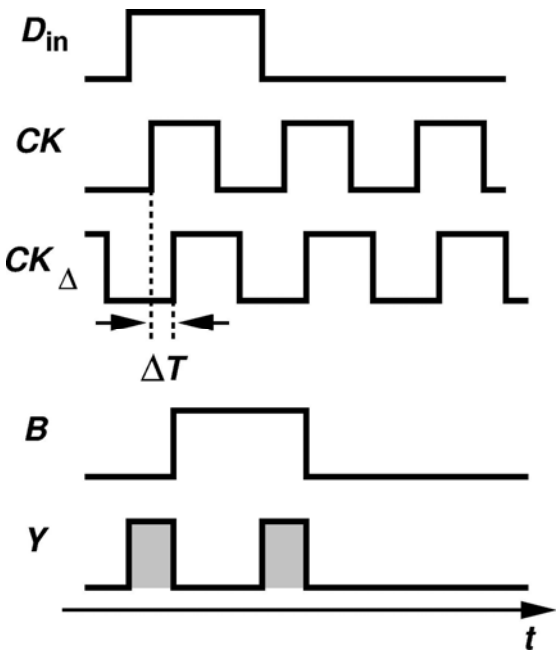


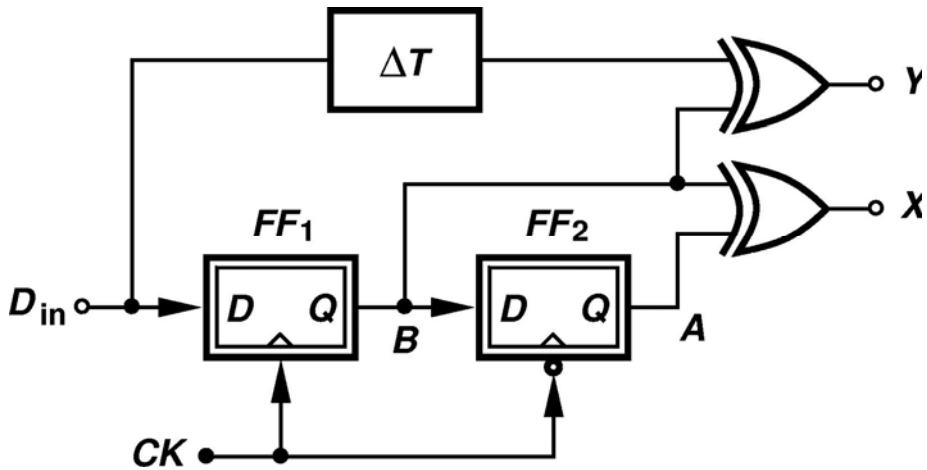
[Hogge, ’85]



- Linear operation.
- Complete pulses must be generated within approximately 1/4 of a bit period.
- Suitable for low to moderate frequency.

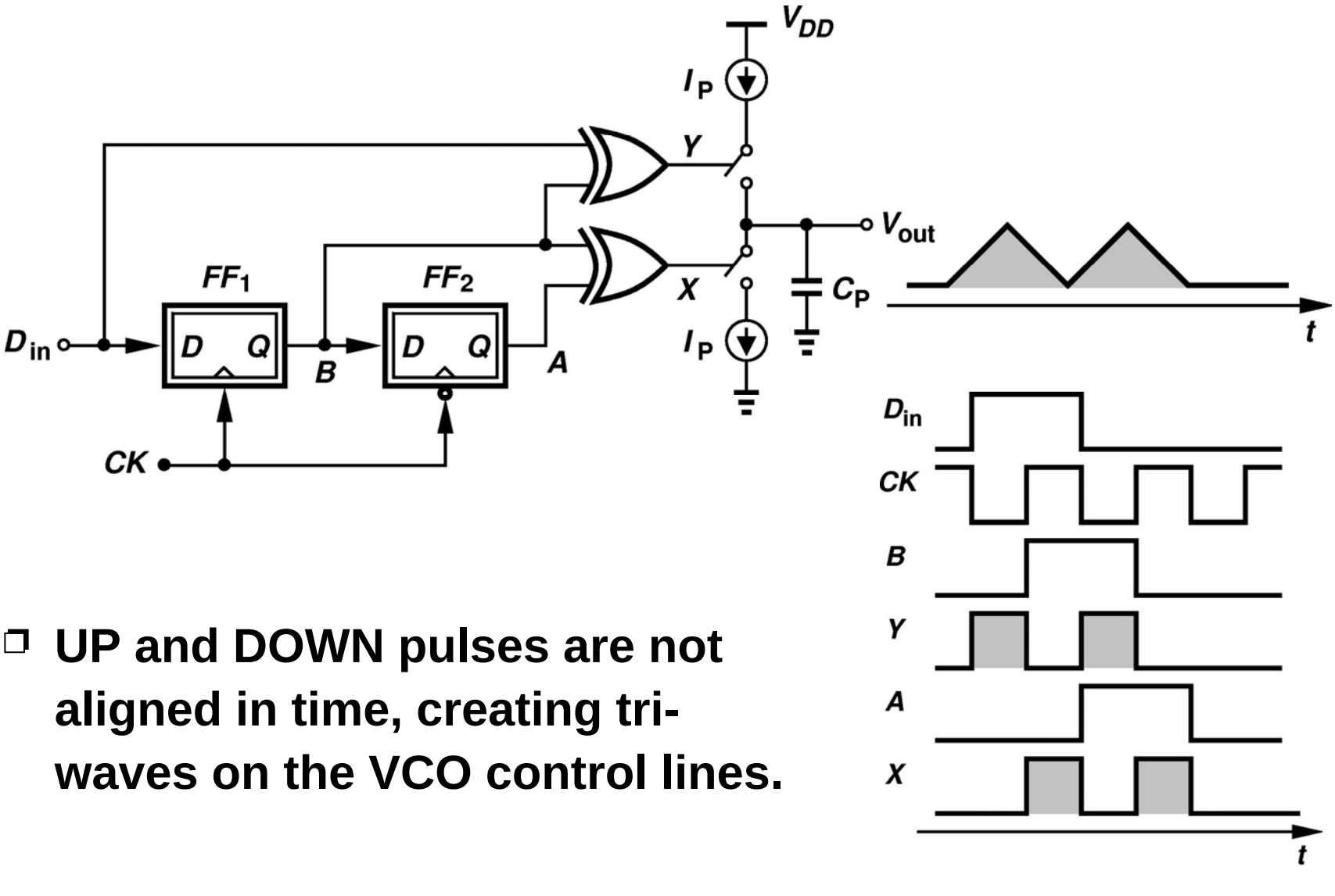
Non-idealities of Hogge Phase Detector





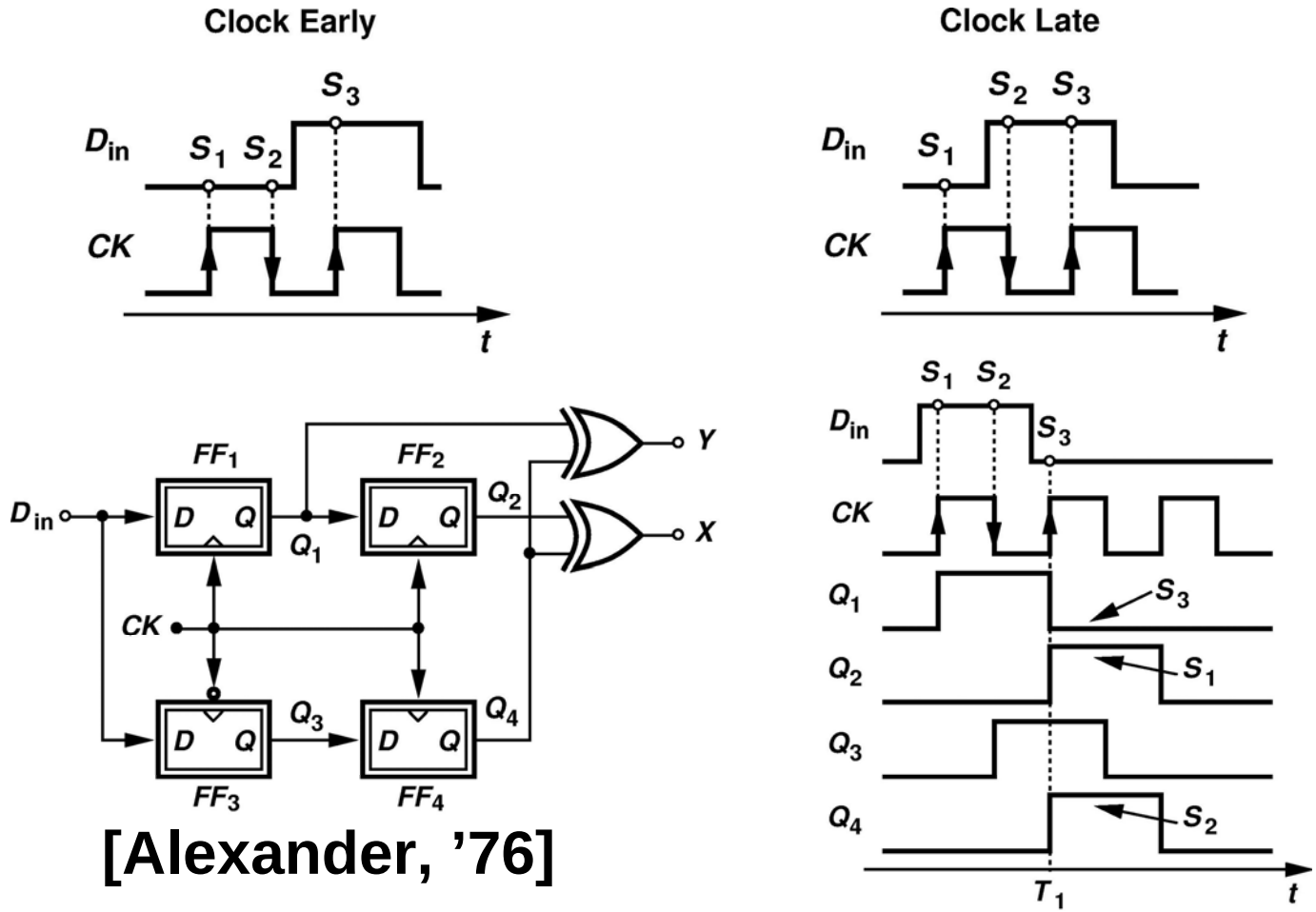
- FF delay requires compensation.
- ΔT may not track the FF delay well across a wide range of temperature and supply variations.
- Generating a delay of several tens of picoseconds is not easy in terms of power and/or area.

Tri-Wave Issue



- **UP and DOWN pulses are not aligned in time, creating tri-waves on the VCO control lines.**

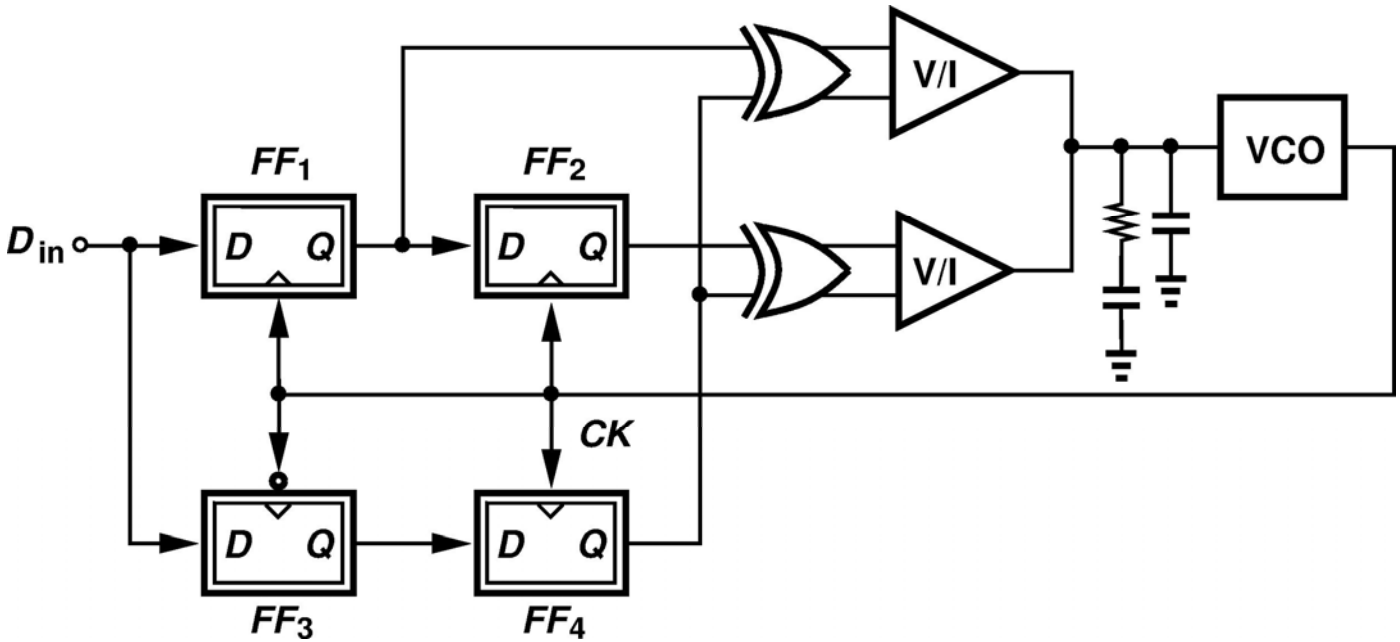
Alexander (Bang-Bang) Phase Detector



[Alexander, ’76]

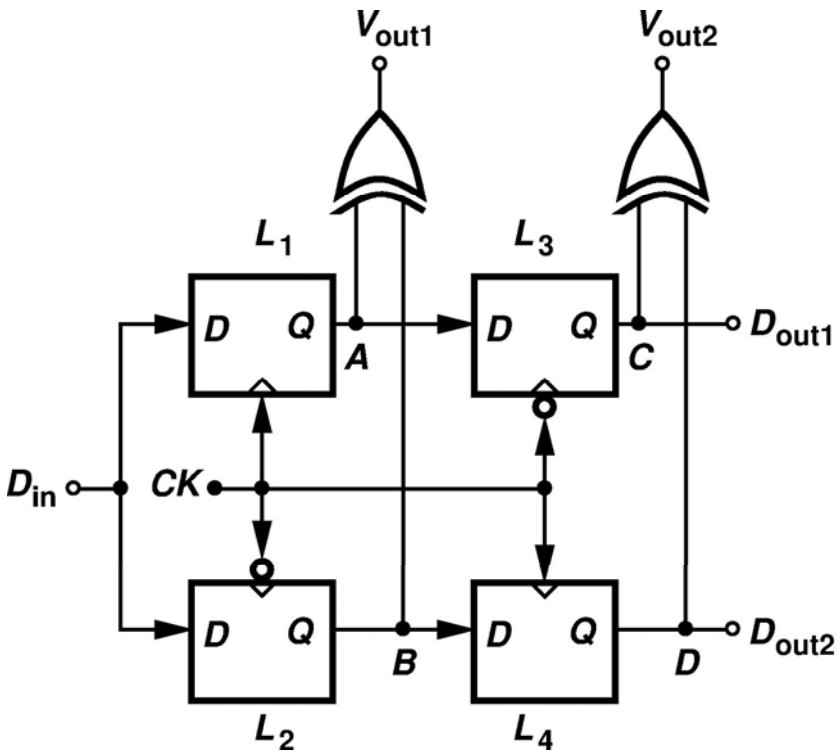
- Binary operation simplifies the phase comparison and increases the speed.
- Abruptly toggling between two states rather than gently waggling around zero.

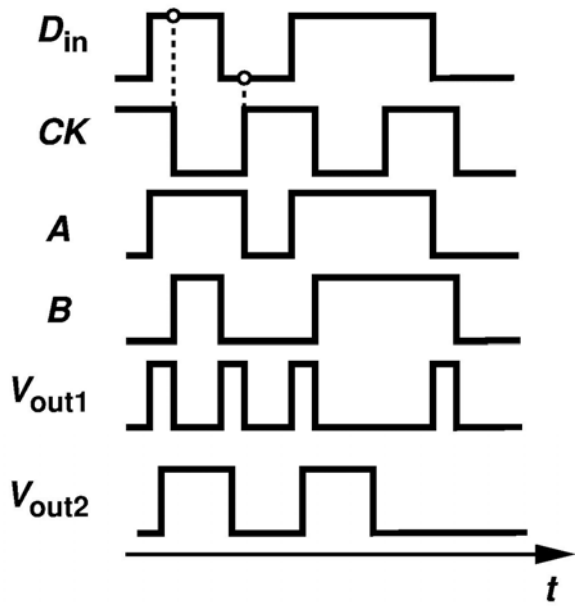
Complete CDR using Alexander PD



- Both Hogge and Alexander PDs provide automatic data retiming and tri-state output (i.e., no net current during long runs).
- Both Hogge and Alexander PDs have only limited capture range and require frequency acquisition loop.

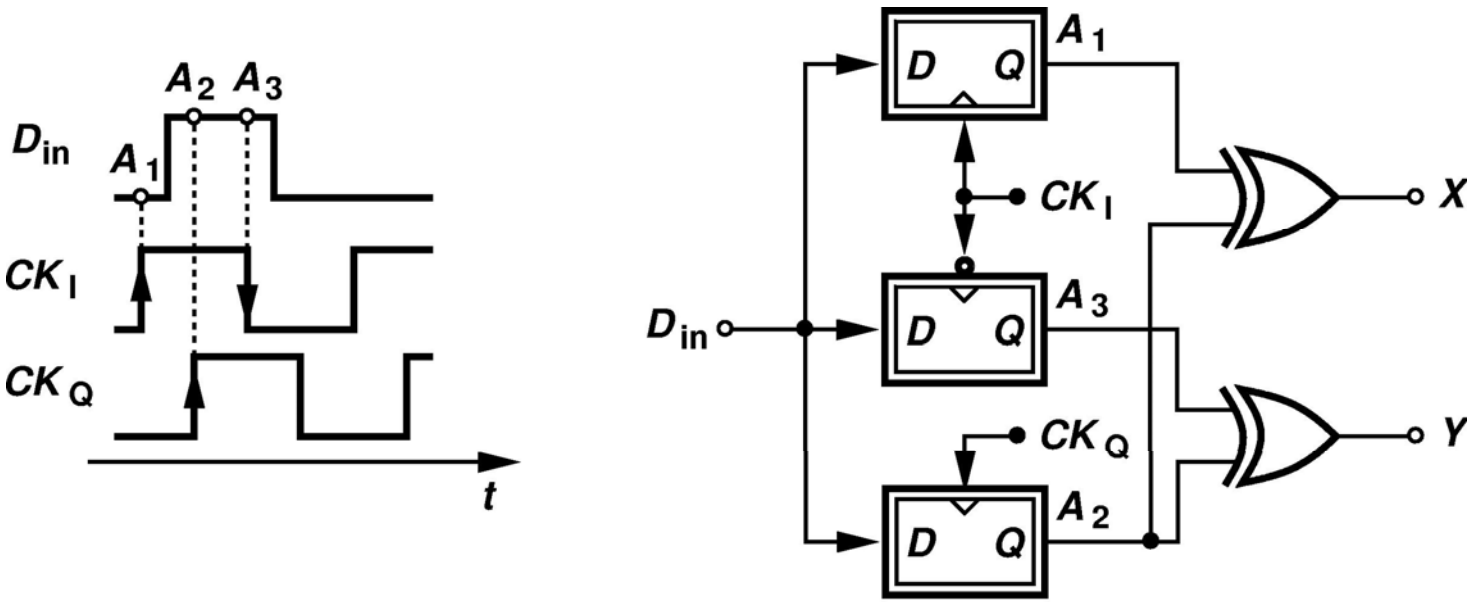
Half-Rate Hogge Phase Detector





- C ⊕ D serves as a reference.
- Clock duty cycle plays crytical roles (must be 50%).

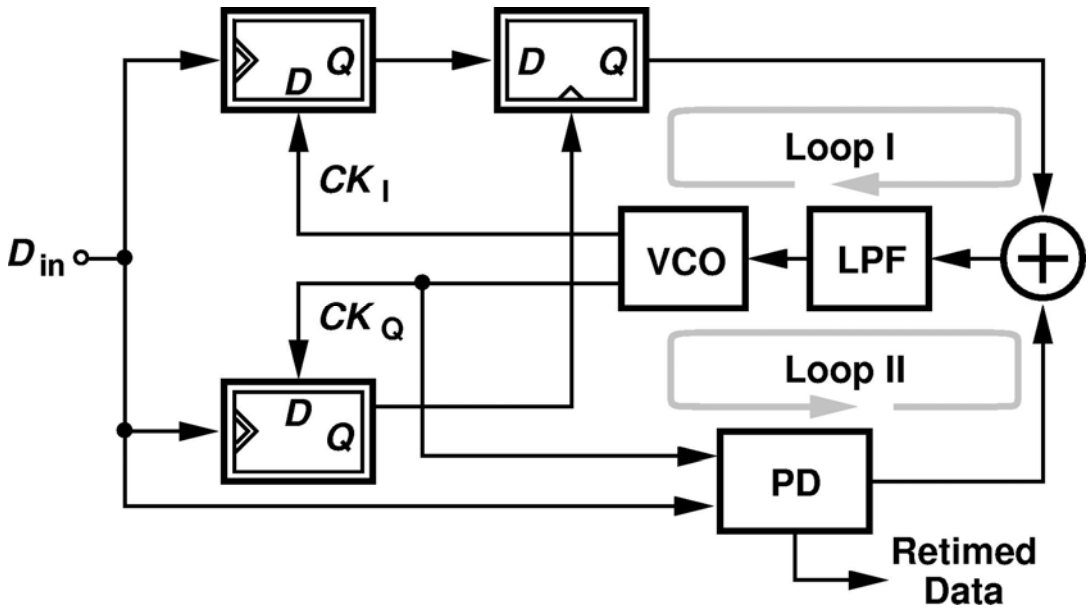
Half Rate Alexander Phase Detector



- Clock with quadrature phases is a must.
- Many other ways to implement sub-rate CDRs (how about quarter rate?)

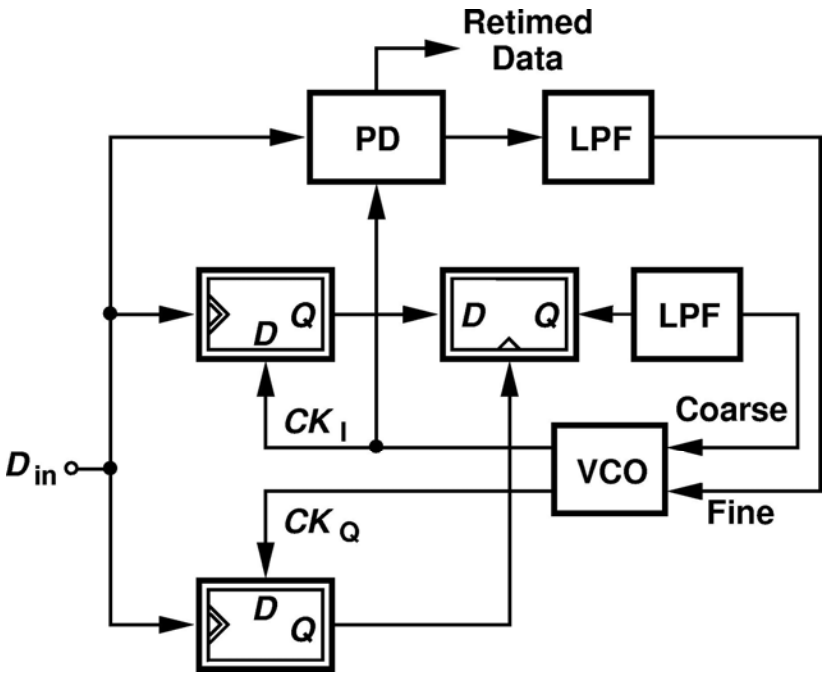
CDR Architecture

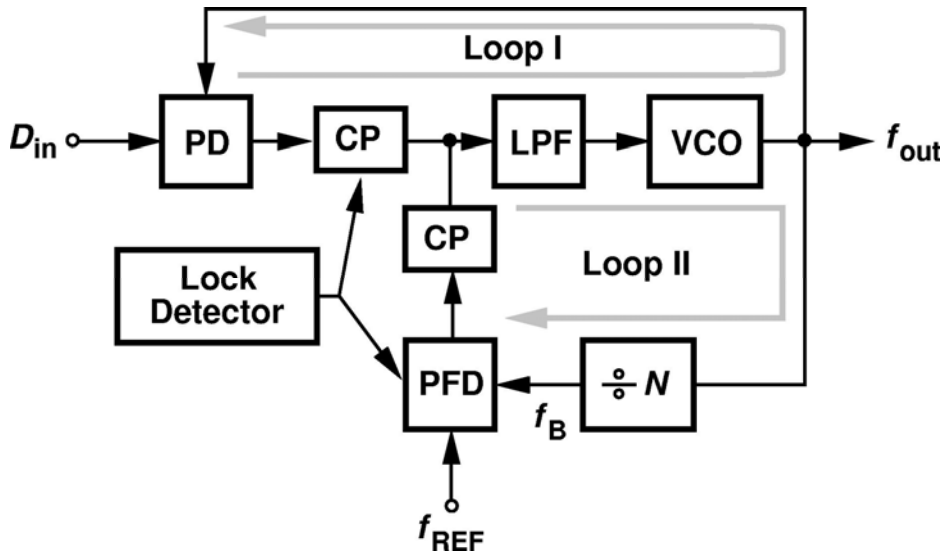
- For most CDRs, the acquisition range is roughly equal to the loop bandwidth, which is about 1/1000 of the data rate.
- Such a small range mandates the use of additional frequency acquisition loop.



- One set of system parameters must satisfy two loops.

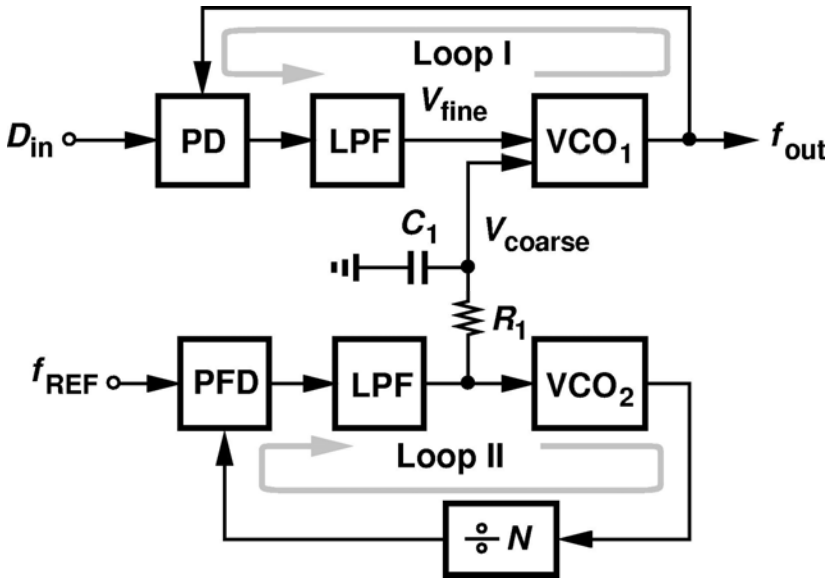
Alternative CDR Architectures

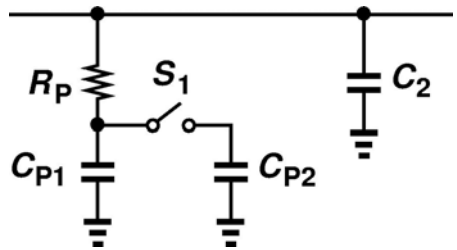




- FD loop pushes the oscillation frequency to roughly-right position.
- PD loop then takes over to lock the phase.
- Lock detector is required to shut down the FD upon lock.

Alternative CDR Architectures

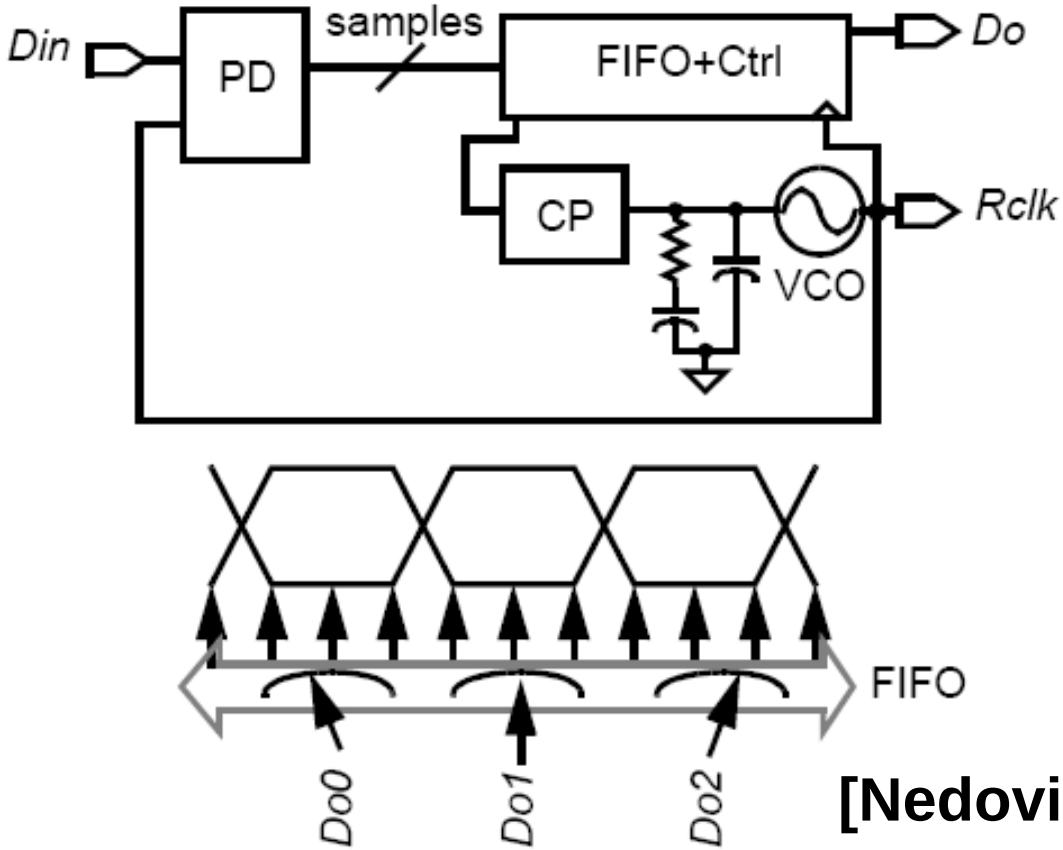




Adjustable Parameters

- **Proper logic and timing control is required for a smooth switching.**
- **But after all, it is the PD loop that determines the performance in lock.**

Case Study – 40Gb/s Over-Sampling CDR



[Nedovic, ISSCC07]

- **3x over sampling.**
- **Quarter-rate VCO.**