Biography (Yao-Wen Chang)

Citation Record Overview:

- Ranked **No. 1 Worldwide** in the augural **EDA Halll of Fame** (283 papers for top-conference, DAC and ICCAD, and top-journal, IEEE TCAD and ACM TODAES, publications); seven out of the 113 researchers on the list were Phil Kaufman Award recipients (a.k.a. the Nobel Prize in EDA), and only seven Taiwanese researchers were listed, including two Academicians, Academia Sinica
- Ranked **No. 1 Worldwide for Recent Five-Year Citations among 40K+ researchers** in the Hardware and Architecture Domain of the Microsoft Academic Search Database (from 2010 till 2011 before the system was retired)
- **ScholarGPS ranks him 4th Worldwide (out of 13103 researchers; top 0.03%) in lifetime EDA impact and honors him as the only non-US Highly Ranked Scholar (only seven Highly Ranked Scholars in EDA worldwide) in 2026,** the only Taiwan-affiliated scholar listed in the top 0.5%.
- Top-2% Scientists by Stanford University: 2026 ranking: Single Year: 74 out of 21,014 researchers **(0.35%)** in the SubField "Computer Hardware & Architecture" (No. 1 in Taiwan); Career Data: 163 out of 21,014 researchers **(0.78%)** in the SubField "Computer Hardware & Architecture" **(No. 1 in "Computer Hardware & Architecture" in Taiwan)**
- Google Scholar: Citations = 13284, H-index: 59 **(Ranked No. 1 in EDA in Taiwan)**



Yao-Wen Chang received a B.S. degree from National Taiwan University (NTU), Taipei, Taiwan, in 1988, and M.S. and Ph.D. degrees from the University of Texas at Austin in 1993 and 1996, respectively, all in computer science.

Dr. Chang is a **Fellow of the ACM (2020), the CIEE (2025), and the IEEE (2013)**. He is a **Past President** of the IEEE Council on Electronic Design Automation (CEDA) after serving as the first non-US/-European CEDA president in 2020/2021. He currently serves as **the IEEE Fellow Search Committee Chair of the IEEE CEDA** and served on the 9-member Selection Committee of **the IEEE Robert N. Noyce Medal** (the highest honor/a.k.a. the Nobel Prize in semiconductors) in 2022, 2023, and 2024, where he championed two final recipients.

He is a Distinguished Professor of the Dept. of Electrical Engineering at NTU after serving as the Dean of the College of Electrical Engineering and Computer Science 2018-2024. He was Deputy Vice President for Academic Affairs of NTU 2016-2018, Director of the Center for Teaching and Learning Development of NTU 2016-2018, Founding Director of the Digital Learning Center of NTU 2017-2018, Associate Dean of the College of EECS 2012-2016, and the Director of the Graduate Institute of Electronics Engineering 2010-2013. Dr. Chang was a visiting professor at Waseda University in Japan 2005--2010 and a visiting scholar at the Computer Science and Artificial Intelligence Laboratory (CSAIL) of Massachusetts Institute of Technology (MIT) in 2014.

His current research interests lie in electronic design automation. He has co-authored one textbook

on Electronic Design Automation (934 pages; Elsevier/Morgan Kaufmann, 2009) and one research book on routing (Springer, 2007), 20 U.S. patents and 7 R.O.C. patents, and about 400 ACM/IEEE conference/journal papers in these areas (**107 papers in ACM/IEEE DAC [#1 worldwide]**, **87 papers in IEEE/ACM ICCAD [#2 worldwide]**, and 92 papers in IEEE TCAD [#4 worldwide]), including highly cited works on floorplanning, placement, routing, design for manufacturability, and FPGA. He ranked No. 1 worldwide in the EDA Hall of Fame with the most DAC+ICCAD+TCAD+TODAES publications in April 2026 (then 283 papers in total; now 298 papers). **The EDA design tools developed by his team have been successfully commercialized twice. Both times were acquired by Synopsys,** the World's largest EDA company, making it one of the very few successful cases in Taiwan. His NTUplace3 placer was renamed in 2008 to the popular Laker Custom Placer of SpringSoft, acquired by the #1 EDA vendor, Synopsys, in 2012 for USD 400M+. His NTUplace4 received three championships at top EDA contests and is the core engine of the leading macro placer, MaxPlace, by Maxeda, which was acquired by Synopsys in 2023. His weighted-average wirelength model for circuit placement has been adopted by Google's AlphaChip (used for Google's TPU and Axion chip designs; Analysts at D.A. Davidson estimated the broader TPU market at US$4.8 billion to US$35.8 billion), NVIDIA's AutoDMP, and newly developed academic placers, such as NTUplace (NTU), ePlace/RePlace (UCSD), DREAMPlace (UT-Austin and Peking University), FuzhouPlace (Fuzhou University and Fudan University), etc. His B*-tree has become a classic topic in textbooks; it is listed as a core skill required for circuit layout design engineers by major international companies (such as Huawei) and is utilized in inhouse tools (e.g., Intel AI Lab) as well as by the winning teams of the last five relevant international EDA competitions.

Dr. Chang's research work has been reported more than ten times by EE Times; he was cited **"a microelectronics pioneer in EDA"** in 2013, and his team was praised as **"The Best and Brightest Worldwide: The best engineering minds on the planet"** in 2015, both by EE Times. Before the system retired, he was ranked #1 worldwide among 40K+ researchers by the Microsoft Academic Search Database for Recent Five-Year Citations in the Hardware and Architecture Domain 2010-2011 (the system was retired in February 2011). ScholarGPS ranks him 4th Worldwide (out of 13103 researchers; top 0.03%) in lifetime EDA impact and honors him as the only non-US Highly Ranked Scholar (only seven Highly Ranked Scholars in EDA worldwide) in 2026, the only Taiwan-affiliated scholar listed in the top 0.5%. He is among World's Top 2% Scientists named by Stanford University for both career-long and single-year categories; 2026 ranking: Single Year: 74 out of 21,014 researchers **(0.35%)** in the SubField "Computer Hardware & Architecture" (No. 1 in Taiwan); Career Data: 163 out of 21,014 researchers **(0.78%)** in the SubField "Computer Hardware & Architecture" **(No. 1 in "Computer Hardware & Architecture" in Taiwan).**

He has received 14 Best Paper Awards (including **the 2025 ICCAD, 2017 DAC,** 2010 ICCD, and 1995 ICCD Best Paper Awards), the 2007 ICCAD Professor Margarida Jacome Memorial Award, and the 2020 ASP-DAC Prolific Author Award. **His first-place Best Paper Awards from the two premier conferences in the EDA field, ICCAD in 2025 (1,078 submissions) and DAC in 2017 (approximately 700 full-paper submissions), makes him the only scholar in Taiwan to win first places in these conferences in their 63-year and 44-year histories, respectively.** Besides the best paper awards, he has received 20+ Best Paper Award Nominations from top conferences, including DAC (6 times), ICCAD (6 times), and ISPD (5 times). Dr. Chang received four awards at the 50th

ACM/IEEE DAC in 2013 for **the DAC Prolific Author** (now **107 papers, the all-time #1 prolific author**), **the Longest Publication Streak** (now 29 years from 1999 to now, #1 worldwide, still running), etc. **He is a 1st-place winner of eight major EDA Contests and has received 24 top-3 contest awards.**

He has been an NTU **Lifetime Distinguished Teacher** since 2020 after receiving two NTU distinguished teaching awards **(the highest honor for the top 1% of teachers, twice for ten years total)**, nine NTU excellent teaching awards (nine years), and one inaugural excellent teaching award from National Chiao Tung University, for a total of 20 years in teaching. He has also received many research awards, including the 2021 Academic Award from the Ministry of Education, the 2022 Distinguished Research Fellow (highest honor), three Distinguished Research Awards (2007, 2010, and 2013), and the 2004 Dr. Wu Ta You Memorial Award, all from the National Science and Technology Council (NSTC) of Taiwan, the IBM Faculty Awards (2010, 2012, and 2013), Google Gifts (2023 and 2024), the 2022 Y. Z. Hsu Science Chair Professorship, the 2020 Distinguished Research Award from the Pan Wen Yuan Foundation, 2017 TECO Award, the 2018 Micron Teacher Award, the 2023 Electrical Engineering Medal **(the highest honor)** and the 2009 Distinguished EE Professor from the Chinese Institute of Electrical Engineering, the 2004 MXIC Young Chair Professorship from the MXIC Corp, and the 2015 MXIC Chair Professorship from NTU.

He has served as IEEE CEDA President (2020/2021), President-elect (2018/2019), and Vice President of Conferences (2016/2017) and Technical Activities (2014/2015). Dr. Chang has been an associate editor of IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), IEEE Transactions on VLSI Systems (TVLSI), IEEE Design & Test of Computers, etc. He has served as the steering committee/general/program chair of ISPD **(first in Asia)**, general/program chair of ICCAD **(the only one in Taiwan)**, program chair of ASP-DAC and FPT, and on the IEEE CEDA, DAC, and ICCAD Executive Committees, the ASP-DAC Steering Committee, and the technical program committees of all major EDA conferences. He is a recipient of the 2026 IEEE CEDA Distinguished Service Award (**the 8th recipient to receive this CEDA's highest service honor and the 1st non-US/-European recipient**), the 2015 IEEE CEDA Outstanding Service Award, and the 2012 ACM Recognition of Service Award. He has played a significant role in the EDA development, serving as the **chair** of the EDA Consortium of Taiwan's Ministry of Education and **the founding chair** of Taiwan's CAD Contest 1999-2001, which has become the world's most popular CAD Contest at ICCAD since 2012, attracting over 200 teams and 600+ participants every year recently. He was interviewed by IEEE Design & Test, the flagship magazine of the IEEE CEDA, in the June 2025 issue, due to his outstanding contributions and impact on the global EDA field, making him the first Taiwanese scholar to be featured in this magazine.

He is currently an independent board director of MediaTek Inc. (the World's 5th IC Design House in 2025, after NVIDIA, Broadcom, Qualcomm, and AMD**)** and has served as an independent board director of Genesys Logic, Inc, a technical consultant of MediaTek, RealTek, and Faraday Technology. **He is a co-founder of Maxeda Technology, acquired by Synopsys in 2023.** He has collaborated with over 20 companies on R&D projects, with over NTD 170M in industry-academia collaborations, generating over NTD 18M in technology licensing (MediaTek requested to

license the WA wirelength model for over NTD 30M in 2026, still in process). He holds 20 U.S. patents and 7 R.O.C. patents, 15 of which have been licensed to industry.

Citations:

EE Times Citation (5/15/2013): "Taiwan: Microelectronics expertise widens" "Taiwan's success so far has been in large part due to electronic design automation (EDA) expertise, where it has only been outperformed by the U.S. for the last five years -- as measured by number of research papers its presented at the IEEE's Design Automation Conference (DAC) and International Conference on Computer Aided Design (ICCAD). **(Yao-Wen) Chang is typical at NTU, a microelectronics pioneer in EDA**, due to receive four separate awards at DAC 2013's 50th anniversary celebration next month,…"

EE Times Citation (by Colin Johnson on 4/6/2015): "**The Best and Brightest Worldwide:** The best engineering minds on the planet compete each year in the ACM's ISPD design contest, which was **won this year by the National Taiwan University**."

EDACafe Citation (11/20/2007): 'International Conference on Computer Aided Design (ICCAD) Witnesses Global Expansion Through Asian Leadership and Participation': "ICCAD 2007 saw increasing participation of leading researchers…, with particular emphasis on Taiwan… This year's CADathlon featured students from NTU as winners of both the 1st and 2nd places,… the 1st time a non-US team won the champion and the 1st time the top two teams came from the same institution… These outstanding wins are the result of multiple initiatives driven from Taiwan... **Professor Yao-Wen Chang,** who chairs the Design Automation and Test sub-initiative, leveraged the CADathlon to evaluate the effectiveness of local VLSI and SoC education programs, aimed at cultivating graduate students to meet the strong demand of the semiconductor industry in Taiwan… ICCAD accepted 16 papers from Taiwan… 2nd worldwide… NTU received 2 best paper award candidates…1 memorial award… **a first for any single institution at ICCAD**."

EE Times Citation (4/17/2008): 'Future of Chip Design Revealed at ISPD': "**how the Taiwanese beat both the US and Europeans in the ISPD Global Routing Contest…"**

張耀文簡傳

張耀文於 1988 年獲得臺灣大學資訊工程學士，並分別於 1993 年和 1996 年獲得德州大學奧斯汀校區電腦科學碩士和博士學位。現為臺灣大學特聘教授 (2011起)。曾擔任臺灣大學電機資訊學院院長 (2018-2024)、副教務長和教學發展中心主任 (2016-2018)、臺灣大學數位學習中心創始主任(2017-2018)、臺灣大學電機資訊學院副院長 (2012-2016)、電子所所長(2010-2013)、副所長(2008-2010)和臺灣大學技轉組組長(2007-2008)、美國麻省理工學院訪問學者(2014)、日本早稻田大學客座教授(2004-2010) 和 IBM T. J. Watson Research Center 研究員(Research Staff Member, 1994)。

張耀文的研究為半導體被稱為晶片之母的電子設計自動化(Electronic Design Automation，EDA)，旨在提升晶片設計的品質。研究成果深刻改變EDA樣貌，成為業界設計工具核心引擎和教科書內容，分別於2013和2020年榮膺**IEEE與ACM Fellow** (首年申請即獲晉升，為2013年IEEE Council on EDA (CEDA)晉升Fellow的第一名)，2025年由中國電機工程學會主動遴選為會士。2013年被電資領域最重要媒體EE Times譽為「**a microelectronics pioneer in EDA**」，2015年團隊被譽為「**The Best and Brightest Worldwide**」。多年國際社群服務，協助臺灣領航EDA發展，**於2020/2021年擔任EDA最重要國際組織IEEE CEDA首位非歐美的總裁，2024年起獲邀擔任IEEE CEDA 的 IEEE Fellow Search Committee 主席，於2022-2024年獲邀擔任 IEEE 總會的 IEEE Robert N. Noyce Medal (a.k.a. 半導體最高榮譽/半導體諾貝爾獎) 遴選委員會委員(共有九名)**，三年任期間協助(championed)兩位最終獲獎者。也是亞洲唯一擔任過兩個頂尖國際會議ICCAD**(台灣唯一)**和ISPD**(亞洲首位)**主席的學者，大幅提升臺灣的影響力。由於其傑出和創新的貢獻 (例如，首創ISPD的Lifetime Achievement Award和其相關系列活動)，獲頒**2026 IEEE CEDA Distinguished Award (CEDA 最高服務榮譽為，為第八位獲獎者，也是非歐美的首位獲獎者)**，2015 IEEE CEDA Outstanding Service Award和2012 ACM Service Award。

合著有專書兩本 (Morgan Kaufmann 出版的934頁EDA教科書等)、20個美國專利和7個中華民國專利(其中15項授權或先期技轉給業界使用)，約400篇的ACM/IEEE期刊和會議論文。**他名列2026年4月首次公布的EDA名人堂全球第一名**(頂尖會議DAC和ICCAD和頂尖期刊TCAD和TODAES共計發表283篇(現發表298篇))，終身和單年全球前2%頂尖科學家(史丹福大學研究資料)，ScholarGPS 將他列為全球終身 EDA 影響力排名第 8 位（前 0.06%），是唯一進入前 0.5% 的台灣學者。其近五年論文引用數曾名列微軟Academic Search Database 的 Hardware & Architecture 領域全球超過四萬名學者中的第一名(2010/2011; 此系統於2011年2月關閉)。他榮獲14項最佳論文獎（包括2025年ICCAD、2017年DAC、2010年ICCD和1995年ICCD最佳論文獎）、2007年ICCAD Margarida Jacome教授紀念獎和2020年ASP-DAC多產作者獎(台灣第一)。他在EDA領域兩大頂級會議---2025年ICCAD（1078篇投稿）和2017年DAC（約700篇全文投稿）---均榮獲第一名最佳論文獎，使他成為台灣唯一在這兩大會議63年和44年歷史上均獲此殊榮的學者。他榮獲第五十屆 DAC 四項研究紀錄獎，包含第五個十年2004-2013全球最多論文獎；現為**DAC 63年史上最多產論文作者，累計發表107篇DAC論文**; DAC論文發表連續長度第一名，目前29年(1999年迄今)；**ACM/IEEE EDA競賽24次獲前三名，有八次冠軍；**超過20次ACM/IEEE 會議最佳論文獎提名，包含 DAC 6 次 (+ 5篇 Best-in-

Track 論文)、ICCAD 6 次 (+ 5篇 Best-in-Track 論文)、TCAD 2 次和ISPD 5 次。FPGA Switch Module 的研究論文曾列 ACM TODAES 期刊第二高研究引用論文長達二十餘年。其於2000年發表的B*-tree平面規劃(floorplanning)表示法和2011年發表的weighted-average (WA)電路擺置(placement)導線模型，當年皆獲DAC最佳論文獎提名，現為學術界和產業界晶片布局設計工具最有效常用的技術，為近年所有相關EDA競賽冠軍所採用的方法(五次floorpalnning和四次placement競賽)。B*-tree 成為教科書的經典內容、表列於國際大廠(例如，華為)招募電路布局設計工程師所需備的核心技術、設計工具(Intel AI Lab等)和最近五次相關floorplanning 國際競賽冠軍隊伍所採用的方法。WA擺置導線模型為當今最佳技術，獲多家公司和學界團隊採用，例如 Google 的 AlphaChip (用於其TPU和Axion晶片設計；Analysts at D.A. Davidson估計 TPU 市場價值約48億至358億美元)、NVIDIA 的 AutoDMP、NTUplace (臺灣大學)、ePlace/RePlace (UCSD)、DREAMPlace (UT-Austin和北京大學)、FuzhouPlace (福州大學和復旦大學)和最近四次placement競賽等。

張教授曾獲多項教學與研究獎，包含臺灣大學教學傑出獎(top 1% 最高榮譽，兩次十年，2020年起為**終身傑出教師**)、優良教學獎(九次)和旺宏電子講座教授 (2015)、教育部學術獎(2021)、科技部研究傑出獎(三次獲滿九年；2007, 2010-2013, 2013-2016)和特約研究員(兩期六年獲滿；2016-2019, 2019-2022)/傑出特約研究員(2023)、2023年中國電機工程學會電機工程獎章(**學會最高榮譽**)和2009年傑出電機工程教授獎、有庠科技講座「資通訊科技講座」(2022)、潘文淵文教基金會傑出研究獎(2020)、東元獎 (2017)、IBM Faculty Awards (三次；2010, 2012, 2013)、Google Gifts (2023和2024)、美光優良教師獎(2018)等。

除曾任IEEE CEDA總裁外，他也曾擔任候任總裁(2018/2019)、技術活動副總裁(2014/2015)和會議副總裁(2016/2017)、IEEE 總會 Ad Hoc Committee 委員和 Smart Cities 指導委員(Steering Committee)。張教授為台灣首位頂尖期刊IEEE TCAD 副編輯 (2008-2013)。 其在1999年起擔任教育部教改計畫EDA競賽主席和EDA聯盟召集人，創辦各項影響深遠的EDA競賽和學術推廣活動，領導台灣團隊在國際舞台上發光發熱，大幅提升台灣的國際影響力和知名度。例如，其於1999年創辦的EDA競賽，現已成為在 ICCAD 舉辦的國際最大EDA競賽，近年每年吸引超過200 個國際團隊參賽；其所帶領的EDA 課程改進計畫，已衍生出受國際學界和業界歡迎和採用的934頁EDA教科書；其於2005年起推動的EDA頂尖國際會議論文倍增計畫，使台灣於2006--2023年間每年在最頂尖EDA國際會議 DAC 和 ICCAD 的合併論文發表數名列全球前三名，而臺灣大學在近二十年來有十四年皆為全球各機構第一名；其於2007年推動的CADathlon 培訓計畫，已使台灣成為ACM CADathlon Contest的最大贏家，台灣共計獲得十二屆冠軍，其中臺灣大學獲得九屆，遠超過其他各校。由於他對全球EDA領域的傑出貢獻和影響，他最近接受的採訪刊登在IEEE CEDA旗艦雜誌《IEEE Design & Test》2025年6月刊上，使他成為首位在該雜誌上被專訪的台灣學者。

張教授和業界互動密切，**現任聯發科技獨立董事**，曾任創惟科技獨立董事、智原科技、瑞昱半導體和聯發科技技術顧問。**其團隊所開發的EDA設計工具，已經兩次商品化成功，兩次皆為EDA國際第一大廠Synopsys (新思科技)所併購，為國內極少數的成功案例。**其NTUplace3電路擺置器於2008年成為思源科技的暢銷工具Laker Custom Digital Placer，對其在2012年以新臺幣122億售予Synopsys有重要貢獻；NTUplace4擺置器為史上唯一三大EDA競賽冠軍，為

2015年合創至達科技MaxPlace的核心引擎，當今頂尖電路擺置工具，至達於2020年起獲利，並獲瑞鼎和聯發科投資，於2023年為Synopsys併購。他曾與20多家公司合作進行研發項目，產學合作總額超過1.7億新台幣，技術授權收入超過1800萬新台幣(聯發科技於2026年3月向臺大提出超過3000萬台幣技轉WA擺置導線模型)。

Curriculum Vitae

Name: Yao-Wen Chang
Gender: Male
Date of Birth: March 22, 1966
Nationality: Taiwan
Email: ywchang@ntu.edu.tw
URL: http://cc.ee.ntu.edu.tw/~ywchang

Work Address: Dept. of Electrical Engineering
National Taiwan University
Taipei 106, Taiwan
Tel: +886-2-33663556
Home Address: 24F-5, No. 218, Sec. 2, South Fushing Road
Taipei 106, Taiwan

Educational Background

9/15/1984－6/15/1988 National Taiwan University, College of Engineering
Department of Computer Science and Information Engineering
B.S. degree in Engineering, 6/15/1988

8/20/1991－5/20/1993 The University of Texas at Austin
Department of Computer Sciences
M.S. degree in Computer Sciences, 5/22/1993 (GPA: 3.9/4.0)

8/20/1993－8/22/1996 The University of Texas at Austin
Department of Computer Sciences
Ph.D. in Computer Sciences, 8/22/1996 (GPA: 4.0/4.0)
Dissertation: Architecture and CAD for Field-Programmable Gate Arrays
Dissertation advisor: Professor Martin D. F. Wong

Employment Record

7/16/1988－5/31/1990 2nd Lieutenant, Taiwan Army, Compulsory Military Service

8/1/1990－7/31/1991 Research Assistant, Institute of Information Science, Academia Sinica, Taiwan

7/15/1992－8/22/1996 Research/Teaching Assistant, Department of Computer Sciences, the

	University of Texas at Austin, U.S.A.
5/20/1994－8/19/1994	Summer Intern (Research Staff Member), VLSI Design Group, IBM T. J. Watson Research Center, New York, U.S.A.
8/ 1/1996－7/31/2001	Associate Professor, Department of Computer and Information Science, National Chiao Tung University, Hsin-Chu, Taiwan.
8/ 1/2001－7/31/2004	Associate Professor, Department of Electrical Engineering and Graduate Institute of Electronics Engineering, National Taiwan University, Taipei, Taiwan
8/ 1/2004 to 7/31/2011	Professor, Department of Electrical Engineering and Graduate Institute of Electronics Engineering, National Taiwan University, Taipei, Taiwan
10/1/2007 to 12/31/2008	Division Head, Division of Technology Transfer, Office of Research and Development, National Taiwan University
1/ 1/2005 to 12/31/2010	Visiting Professor, Graduate Institute of Information, Production, and Systems, Waseda University, Japan
1/ 1/2009 to 7/31/2010	Deputy Director, Graduate Institute of Electronics Engineering, National Taiwan University, Taipei, Taiwan
8/1/2010 to 7/31/2013	Director (Chairman), Graduate Institute of Electronics Engineering, National Taiwan University, Taipei, Taiwan
2/ 1/2014 to 7/8/2014	Visiting Scholar, Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Massachusetts, USA
1/1/2015 to 12/31/2015	MXIC Chair Professor, National Taiwan University, Taipei, Taiwan
8/1/2012 to 8/18/2016	Associate Dean, College of Electrical Engineering and Computer Science, National Taiwan University, Taipei, Taiwan
8/19/2016 to 7/31/2018	Deputy Vice President for Academic Affairs & Director of the Center for Teaching and Learning Development & Director of the Digital Learning Center (2017-2018), National Taiwan University, Taipei, Taiwan
8/1/2018 to 7/31/2024	Dean, College of Electrical Engineering and Computer Science, National Taiwan University, Taipei, Taiwan

8/1/2018 to 7/31/2024 Director, Center of Electronic and Information Technology, National Taiwan University, Taipei, Taiwan

8/ 1/2011 to present Distinguished Professor, Department of Electrical Engineering and Graduate Institute of Electronics Engineering, National Taiwan University, Taipei, Taiwan

Current Employer and Position

Distinguished Professor, Department of Electrical Engineering and Graduate Institute of Electronics Engineering, National Taiwan University

Independent Board Director, MediaTek Inc. (World's 5th IC Design House in 2025)

Field of Specialization

Electronic Design Automation, VLSI Physical Design, Heterogeneous Integration, Design for Manufacturability/Reliability, AI for EDA & EDA for AI, Optimization

Academic and Professional Awards

A. Professional Society Awards

- IEEE CEDA Distinguished Service Award, 2026 (**CEDA's highest service honor; the 8th (the 1st non-US/-European) recipient**)
- CIEE Fellow, 2025.
- ACM Fellow, 2020 (for contribution to algorithmic electronic design automation)
- IEEE Fellow, 2013 (*for contribution to physical design and manufacturability*)
- IEEE CEDA Outstanding Service Award, 2015 (*for outstanding service as the general chair of IEEE/ACM ICCAD'14*
- ACM Recognition of Service Award, 2012 (*for serving as the general chair of ACM ISPD'11*)

B. Best Paper Awards (1-4: ACM/IEEE BPA)

1. **IEEE/ACM International Conference on Computer-Aided Design (ICCAD William J. McCalla Best Paper Award (Backend)),** title: Semidefinite programming-based decoupling capacitor placement for power distribution network optimization, October 2025 **(First-place BPA out of 1078 submissions: Received unanimous perfect scores from all seven Best Paper Committee members); the first in Taiwan in its 44-year history**
2. **ACM/IEEE Design Automation Conference (DAC)**, title: Toward optimal legalization for mixed-cell-height circuit designs, June 2017 **(First-place BPA out of about 700 submissions) ; the first in Taiwan in its 64-year history**

3. IEEE International Conference on Computer Design (ICCD), title: Provably good OPC modeling and its applications to interconnect optimization, October 2010
4. IEEE International Conference on Computer Design (ICCD), title: FPGA global routing based on a new congestion metric, October 1995
5. VLSI Design/CAD Symposium, title: Standard-cell-aware learning-guided adaptive weighting for analytical mixed-size placement, August 2026 (First-Place BPA in the EDA, Test, and Embedded System Category)
6. VLSI Design/CAD Symposium, title: Pre-assignment routing for performance optimization in high-speed 2.5D/3D packaging, August 2025 (First-Place BPA in the EDA, Test, and Embedded System Category)
7. VLSI Design/CAD Symposium, title: Thermal-aware optical-electrical co-routing algorithm for networks-on-chip, August 2021
8. VLSI Design/CAD Symposium, title: Toward optimal unified RDL routing algorithms for 2.5D IC packages, August 2018
9. VLSI Design/CAD Symposium, title: An effective RDL routing algorithm for the InFO WLCSP technology, August 2016 (Best Feature Paper Award)
10. VLSI Design/CAD Symposium, title: A detailed-routability-driven analytical placer considering technology and region constraints, August 2015
11. VLSI Design/CAD Symposium, title: ECO timing and mask-cost optimization with Redundant wires, August 2010
12. VLSI Design/CAD Symposium, title: Coupling-constrained dummy fill for density gradient minimization, August 2008
13. VLSI Design/CAD Symposium, title: BioRoute: A network-flow based routing algorithm for digital microfluidic biochips, August 2007
14. VLSI Design/CAD Symposium, title: Simultaneous buffer-insertion/-sizing and wire-sizing formulae with applications to interconnect-driven floorplanning, August 2000

C. Conference Research Achievement Awards: Celebration for the 50th anniversary of the ACM/IEEE DAC in 2013

- ACM/IEEE DAC Prolific Author Award at the 50th ACM/IEEE Design Automation Conference (DAC): DAC 40 Club: Has published 40 or most papers at DAC (top-10 worldwide in history); **now 107 papers (all-time #1 prolific author)**
- ACM/IEEE DAC Long (12+ years) Publication Streak at the 50th DAC: For having one of the ten longest DAC publication streaks (15 consecutive DAC conferences 1999-2013; top-5 worldwide in history); **now 29 years (#1 worldwide; 1999-now) & still running**
- ACM/IEEE DAC First Most Papers in Fifth Decade at the 50th DAC: For being the most prolific author for DAC's fifth decade (34 papers in the 5th decade, #1 worldwide); **still the 1st Most Prolific Author in the 6th Decade with 50 papers from 2014 to 2023**
- ACM/IEEE DAC Prolific Author in a Single Year at the 50th DAC: At least 6 DAC papers in a single year (7 DAC papers in 2012 and 2013 each; the only researcher with over three-year records); also 7 papers in 2020 and 2022 each, 8 papers in 2023, and 6 papers in 2025 and

2026 **(the researcher with the most multiple-year record; 7 times)**

D. **ASP-DAC Prolific Author Award**（Celebration for the 25th anniversary of the IEEE/ACM ASP-DAC in 2020; First Place in Taiwan)

E. **World's No. 1, EDA Hall of Fame, 2026** (283 papers in top conferences, DAC and ICCAD, and top journals, IEEE TCAD and ACM TODAES; 298 papers now)

F. ScholarGPS ranks him 8th globally (top 0.06%) in lifetime EDA impact, the only Taiwan-affiliated scholar listed in the top 0.5%, 2026

G. World's Top 2% of Scientists for both Career-long and Single-year Categories (Surveyed by Stanford University)

H. Conference Memorial Award

- Professor Margarida Jacome Memorial Award (with Travel Grant) at the 2007 IEEE/IEEE International Conference on Computer-Aided Design (ICCAD'07), for the paper "BioRoute: A network flow-based routing algorithm for digital microfluidic biochips"
  - ➢ Only two out of 508 submissions received this award

I. International Contest Awards (received the most EDA contest awards worldwide, including eight champions)

1. 2nd Place at the CAD Contest @ ICCAD (Problem B: Power and Timing Optimization Using Multibit Flip-Flop) jointly sponsored by the IEEE CEDA and the Ministry of Education of Taiwan, 2025 (88 participating teams)
2. **1st Place** at the CAD Contest @ ICCAD (Problem B: Power and Timing Optimization Using Multibit Flip-Flop) jointly sponsored by the IEEE CEDA and the Ministry of Education of Taiwan, 2024 **(81 participating teams)**
3. **1st Place** at the CAD Contest @ ICCAD (Problem B: 3D Placement with Macros) jointly sponsored by the IEEE CEDA and the Ministry of Education of Taiwan, 2023 **(74 participating teams)**
4. 2nd Place in the Security Closure of Physical Layouts Contest hosted by ACM International Symposium on Physical Design (ISPD), 2022.
5. 4th Place (Honorable Mention) at the Wafer Scale Physics Modeling Contest hosted by ACM International Symposium on Physical Design (ISPD), 2021.
6. 4th Place (Honorable Mention) at the CAD Contest @ ICCAD (Problem B: Routing with Cell Movement) jointly sponsored by the IEEE CEDA and the Ministry of Education of Taiwan, 2020.
7. 4th Place (Honorable Mention) at the Wafer-Scale Deep Learning Accelerator Contest hosted

by ACM International Symposium on Physical Design (ISPD), 2020.

8. 2nd Place at the CAD Contest @ ICCAD (Problem B: System-level FPGA Routing with Timing Division Multiplexing Technique) jointly sponsored by the IEEE CEDA and the Ministry of Education of Taiwan, 2019.
9. 2nd Place at the Initial Detailed Routing Contest hosted by ACM International Symposium on Physical Design (ISPD), 2019.
10. 3rd Place at the CAD Contest @ ICCAD (Problem A: Smart EC: Program-Building for Name Mapping) jointly sponsored by the IEEE CEDA and the Ministry of Education of Taiwan, 2018.
11. 3rd Place at the CAD Contest @ ICCAD (Problem B: Obstacle-Aware On-Track Bus Routing) jointly sponsored by IEEE CEDA and the Ministry of Education of Taiwan, 2018.
12. 3rd Place at the Initial Detailed Routing Contest hosted by ACM International Symposium on Physical Design (ISPD), 2018.
13. 2nd Place at the CAD Contest @ ICCAD (Problem B: Net Open Location Finder with Obstacles) jointly sponsored by the IEEE CEDA and the Ministry of Education of Taiwan, 2017.
14. 2nd Place at the CAD Contest @ ICCAD (Problem C: Multi-Deck Standard Cell Legalization) jointly sponsored by the IEEE CEDA and the Ministry of Education of Taiwan, 2017.
15. 2nd place at the 2017 ACM FPGA Placement Contest hosted by ACM International Symposium on Physical Design (ISPD), 2017.
16. **1st place** at the 2015 ACM Blockage-Aware Detailed Routability Driven Placement Contest hosted by ACM International Symposium on Physical Design (ISPD), 2015.

    - *'The Best and Brightest Worldwide' by R. Colin Johnson of EE Times (4/6/2015): "The best engineering minds on the planet compete each year in the ACM's ISPD design contest, which was won this year by the National Taiwan University"*

17. **1st Place** at the CAD Contest @ ICCAD (Category: Legalization and Detailed Placement), jointly sponsored by the IEEE CEDA and the Ministry of Education of Taiwan, 2013.
18. 3rd Place at the CAD Contest @ ICCAD (Category: OPC Mask Optimization), jointly sponsored by IEEE CEDA and the Ministry of Education of Taiwan, 2013.
19. 3rd Place at the inaugural CAD Contest @ ICCAD (Category: Placement), jointly sponsored by the IEEE CEDA and the Ministry of Education of Taiwan, 2012.
20. 3rd Place at the inaugural CAD Contest @ ICCAD (Category: DFM on Hot-spot Detection) jointly sponsored by the IEEE CEDA and the Ministry of Education of Taiwan, 2012.
21. **1st Place** at the inaugural ACM/IEEE Routability-Placement Contest hosted by ACM/IEEE Design Automation Conference (DAC), 2012.
22. **1st Place** at the ACM Discrete Gate Sizing Contest hosted by ACM International Symposium on Physical Design (ISPD), 2012.
23. 4th Place (Honorable Mention) at the Routability-Driven Placement Contest hosted by ACM International Symposium on Physical Design (ISPD), 2011.

24. **1st Place** at the inaugural PATMOS Timing Analysis Contest sponsored by IEEE CEDA and hosted by IBM and INESC-ID, 2011.
25. 3rd Place at the ACM High-Performance Clock Network Synthesis Contest hosted by ACM International Symposium on Physical Design (ISPD), 2010.
26. **1st Place** at the ACM Clock Network Synthesis Contest hosted by ACM International Symposium on Physical Design (ISPD), 2009 (scores for the top-3 performers: 2.43 (NTU), 2.71, 3.29; the smaller, the better)
27. 2nd Place at the ACM Global Routing Contest hosted by ACM International Symposium on Physical Design (ISPD), 2008.
28. 3rd Place at the ACM Placement Contest hosted by ACM International Symposium on Physical Design (ISPD), 2006.

J. Research Awards

1. **Electrical Engineering Medal**, Chinese Institute of Electrical Engineering (CIEE; **the CIEE highest honor**), 2023 (one of the youngest recipients)
2. **Distinguished Research Fellow, National Science and Technology Council (formerly Ministry of Science and Technology), 2023**
3. Google Gifts, 2023, 2024
4. Y. Z. Hsu Science Chair Professorship (Information and Communication), 2022.
5. **Academic Award, The Ministry of Education, 2021**
6. Special Research Fellow, Ministry of Science and Technology, 2016-2019 & 2019-2022
7. Distinguished Research Award, The Pan Wen Yuan Foundation, 2020.
8. TECO Award, 2017
9. Distinguished Research Award of Mistry of Science and Technology (MoST), Taiwan, for research excellence, 2007-2010, 2010-2013, 2013-2016
10. MXIC Chair Professorship (National Taiwan University), MXIC, 2015
11. IBM Faculty Awards, 2010, 2012, 2013
12. Distinguished EE Professorship, CIEE, 2009
13. First-Class Principal Investigator Award (formerly Distinguished Research Award) of National Science Council, Taiwan, for distinguished research, 2005, 2006 (the only two years that granted this award)
14. Dr. Wu Ta You Memorial Award of National Science Council, Taiwan, 2004
15. MXIC Young Chair Professorship, MXIC, 2005
16. Research Achievement Award, National Taiwan University, 2004

K. Teaching Awards

- **Lifetime Distinguished Teacher (2020)** with two Distinguished Teaching Awards **(twice for 10 years, the highest honor for the top 1% of teachers)**, National Taiwan University, 2012 -- 2017 (five years), 2020 – 2025 (five years)

- Excellent Teaching Award (for top-5% [before 2008]/-9% professors), National Taiwan University, 2004, 2005, 2007, 2008, 2009, 2010, 2011, 2018, 2019 (9 times), one of the most in the Department of EE
- Micron Teacher Award, 2018
- Excellent Teaching Award, National Chiao Tung University, 2000 (inaugural award)
- Excellent Teaching Material Award, Ministry of Education, 2001

L. ACM/IEEE Best Paper Nominations

1. 2020 IEEE/ACM ASP-DAC; title: Unified redistribution layer routing for 2.5D IC packages
2. 2018 IEEE/ACM ICCAD; title: Analytical solution of Poisson's equation and its application to VLSI global placement **(best paper award runner-up)**
3. 2015 *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD);* title: TSV-aware analytical placement for 3D IC designs based on a novel weighted-average wirelength model **(best paper award runner-up)**
4. 2013 ACM ISPD; title: Simultaneous OPC- and CMP-aware routing based on accurate closed-form modeling
5. 2012 ACM ISPD; title: Graph-based subfield scheduling for electron-beam photomask fabrication **(best paper award runner-up)**
6. 2011 ACM/IEEE DAC; title: TSV-aware analytical placement for 3D IC Design **(best paper award runner-up)**
7. 2010 IEEE/ACM ICCAD; title: Native-conflict-aware wire perturbation for double patterning technology
8. 2009 *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD);* title: NTUplace3: An analytical placer for large-scale mixed-size designs with preplaced blocks and density constraints
9. 2009 IEEE/ACM ICCAD; title: Voltage-drop aware analytical placement by global power spreading for mixed-size circuit designs (13 out of 435 submissions)
10. 2008 ACM/IEEE Design Automation Conference (DAC); title: Predictive formulae for OPC with applications to lithography-friendly routing, June 2008 (14 out 653 submissions)
11. 2008 ACM International Symposium on Physical Design (ISPD); title: Metal-density driven placement for CMP variation and routability, March 2008
12. 2007 IEEE/ACM International Conference on Computer-Aided Design (ICCAD); title: Novel wire density driven full-chip routing for CMP variation control, November 2007 (9 out 508 submissions)
13. 2007 ACM/IEEE Design Automation Conference (DAC); title: An integer linear programming algorithm for flip-chip routing, June 2007 (15 out 659 submissions)
14. 2007 ACM International Symposium on Physical Design (ISPD); title: X-architecture placement based on effective wire models, March 2007
15. 2007 ACM International Symposium on Physical Design (ISPD); title: Efficient obstacle-avoiding rectilinear Steiner tree construction, March 2007

16. 2005 ACM/IEEE Design Automation Conference (DAC); title: Multilevel full-chip routing for the X-based architecture, June 2005 (14 out 735 submissions)
17. 2004 IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC); title: Temporal floorplanning using 3D-subTCG. January 2004 (8 out of 291 submissions)
18. 2003 ACM Transactions on Design Automation of Electronic Systems; title: Rectilinear block placement using B*-trees (5 nominees)
19. 2002 IEEE/ACM International Conference on Computer-Aided Design (ICCAD); title: A novel framework for multilevel routing considering routability and performance, November 2002
20. 2001 IEEE International Conference on Computer Design (ICCD); title: Generic ILP-based approaches for dynamically reconfigurable FPGA partitioning, October 2001
21. 2000 ACM/IEEE Design Automation Conference (DAC); title: B*-trees: A new representation for non-slicing floorplans, June 2000

M. Best-in-Track Papers

1. 2024 IEEE/ACM ICCAD; title: Efficient high-fidelity two-dimensional warpage modeling for advanced packaging analysis
2. 2020 ACM/IEEE DAC: title: An efficient EPIST algorithm for global placement with non-integer multiple-height cells
3. 2020 ACM/IEEE DAC: title: Time-division multiplexing based system-level FPGA routing for logic verification
4. 2019 IEEE/ACM ICCAD; title: Timing-aware fill insertions with design-rule and density constraints
5. 2018 IEEE/ACM ICCAD; title: Analytical solution of Poisson's equation and its application to VLSI global placement
6. 2018 ACM/IEEE DAC; WB-trees: a meshed tree representation for FinFET-based analog layout designs
7. 2017 IEEE/ACM ICCAD; title: Mixed-cell-height detailed placement considering complex minimum-implant-area constraints
8. 2017 IEEE/ACM ICCAD; Clock-aware placement for large-scale heterogeneous FPGAs
9. 2016 ACM/IEEE DAC; title: QB-trees: towards an optimal topological representation with applications to analog layout designs
10. 2006 IEEE/ACM ICCAD; title: A high quality analytical placer considering preplaced blocks and density constraint

N. **Publicity Papers** (DAC'22 is the only year with this promotion)

1. 2022 ACM/IEEE DAC; title: Y-architecture-based flip-chip routing with dynamic programming-based bend minimization
2. 2022 ACM/IEEE DAC; title: Flexible chip placement via reinforcement learning

O. Supervision Awards

- Supervisor for the 2nd-Place team, 2023 ACM CADathlon at ICCAD, November 2023 (Students: Y.-C. Chen and C.-H. Hsieh)
- Supervisor for the 1st-Place team, 2012 ACM CADathlon at ICCAD, November 2012 (Students: Hung-Chih Ou and Po-Ya Hsu)
- Supervisor for the 1st-Place winner, 2012 ACM/SIGDA Student Research Competition; the first non-US winner, June 2012 (Students: Shao-Yun Fang)
- Supervisor for the Silver Award winner, 2012 TSMC Outstanding Student Research Award, July 2012 (Students: Shao-Yun Fang)
- Supervisor for the 1st-Place team, 2007 ACM CADathlon at ICCAD; the first non-US team to win this contest, November 2007 (Students: Zhe-Wei Jiang and Tung-Chieh Chen)
- Lam Thesis Awards, 2002, 2003, 2005, 2007, 2010, 2012, 2025
- CIEE Annual Thesis Awards, 1st places (years 2007, 2009, 2010, 2011, 2014, 2016, 2017, 2021), 2nd places (1998, 2012, 2018, 2025), 3rd places (2002, 2005)
- TICD Annual Ph.D. Dissertation Awards: 2010, 2013, 2014, 2015, 2016, 2017, 2022 (*participated in these six years and received the only one EDA award in each of these years*)
- IC/CAD Contests hosted by the Ministry of Education from 2003 to 2010: 1st place award 特優 (10 pieces), 2nd place 優等 (8), 3rd place 佳作 (16); ***received the most awards***
- Domestic Contests for the CAD Contest @ ICCAD from 2014 to 2022: 1st place award 特優 (6 pieces), 2nd place 優等 (8 pieces)

Academic and Professional Activities

A. Professional Societies

- **Chair, IEEE CEDA's IEEE Fellow Search Committee,** 2025--present
- **President & President-elect, IEEE Council on EDA (CEDA), 2020/2021, 2018/2019**
  - The first non-US/-European president-elect & president of the IEEE CEDA
- **IEEE Robert N. Noyce Medal Selection Committee (a.k.a. the Nobel Prize in semiconductors),** 2022/2023/2024
- Chair, IEEE CEDA Nominations and Appointments Committee, 2022/2023
- IEEE Consumer Technology Society Publication Board, 2021/2022
- IEEE Ad Hoc Committee, 2020/2021
- IEEE Smart Cities Steering Committee, 2020/2021
- Chair, Strategy Committee, IEEE CEDA, 2018/2019
- Vice President of Conferences (& Chair, Conference Committee), IEEE Council on EDA (CEDA), 2016/2017
  - In charge of 20 financially and 12 technically sponsored conferences and related conference policies and activities
- Vice President of Technical Activities (& Chair, Technical Activities Committee), IEEE Council on EDA (CEDA), 2014/2015
  - In charge of CEDA worldwide chapters, distinguished lectures, contests, workshop

- Award Committee, IEEE CEDA, 1/2015 – 12/2017
  - Review all CEDA awards and IEEE Fellow elevations
- Secretary General, Taiwan Professional and Organizational Development Network in Higher Education (TPOD), 10/2016 – 7/2018
- Executive Committee Member (Secretary), IEEE CEDA, 1/2012—12/2013
- IEEE CEDA Conference Committee Member, 1/2010—12/2011
- ACM/SIGDA Physical Design Technical Committee Member, 10/2006—12/2010
- ACM/SIGDA Pioneering Award Committee, 2020, 2023
- Member of the Board of Governors, Chinese Institute of Electrical Engineering (CIEE), Taiwan, 1/2018—12/2024
- Member of the Board of Governors, Taiwan IC Design Society, Taiwan, 8/2004—7/2012
- Life Member, ACM
- Life Member, Chinese Institute of Electrical Engineering (CIEE)
- Life Member, Taiwan IC Design Society (TICD)

B. Journal Editorship

- IEEE Transactions on VLSI Systems (TVLSI), 1/2015—12/2023
- IEEE Design and Test of Computers, 1/2012—12/2014, 1/2016-2022 (interview editor)
- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 1/2008 -- 12/2013
- IET Computers & Digital Techniques, 6/2014—12/2016
- Journal of Information Science and Engineering (JISE), 1/2007—12/2012

C. Organizing/Executive Committees

- Executive Committee, ACM/IEEE Design Automation Conference (DAC), 2022, 2023
- IEEE/ACM International Conference on Computer-Aided Design (ICCAD): 2012 Technical Program Committee (TPC) Vice Chair, 2013 TPC Chair, 2014 General Chair, 2015 Past Chair
  - *The **only ICCAD conference chair from Taiwan**; ICCAD is a premier conference in EDA, ranked #3 among the 102 conferences listed in the Hardware & Architecture Domain of the Microsoft Academic Search Database*
- ACM International Symposium on Physical Design (ISPD): 2008 Publicity Chair, 2009 Publication Chair, 2010 Technical Program Committee Chair, 2011 General Chair
  - *The **first ISPD chair from Asia**; ISPD is a premier conference in physical design (PD), ranked #4 among the 102 conferences listed in the Hardware & Architecture Domain of the Microsoft Academic Search Database; initiated in 2011 a commemorative session and a party to pay tributes to the pioneers in PD (see Figure 1 for an EE Times article on this initiative)*
- ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC): 2011 Technical Program Committee Vice Chair, 2012 Technical Program Committee Chair
- Steering Committee, ACM International Symposium on Physical Design (ISPD), 2012 Steering Committee Chair, 2013—now Steering Committee Members
- Executive Committee, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2008—2010, 2012—2015

- Steering Committee, ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC), 2008—2015
- Program Committee Co-Chair, IEEE Field-Programmable Technology (FPT), 2008



Figure 1: (left) Serving as the ICCAD'14 general chair; (right) EE Times article on the commemorative program initiated by Yao-Wen Chang, the ISPD'11 general chair

D. Technical Program Committees

1. ACM/IEEE Design Automation Conference (DAC), 2007, 2008
2. IEEE/ACM International Conference on Computer Aided Design (ICCAD), 2004, 2005, 2006, 2012, 2013
3. ACM International Symposium on Physical Design (ISPD), 2006, 2007, 2008 (Publicity Chair), 2009 (Publication Chair), 2010 (Technical Program Committee Chair), 2011 (General Chair)
4. ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC), 2003, 2004, 2005, 2006, 2007 (Subcommittee chair), 2008 (Subcommittee Chair), 2010 (Subcommittee Chair), 2011 (Technical Program Committee Vice Chair), 2012 (Technical Program Committee Chair), 2013
5. ACM Great Lake Symposium on VLSI (GLSVLSI), 2007, 2008
6. ACM/IEEE Design Automation and Test Conf. in Europe (DATE), 2005, 2006, 2007
7. IEEE International Conference on Computer Design (ICCD), 2004, 2005, 2006
8. IEEE International Conf. on Field Programmable Logic and Applications, 2008, 2009

9. IEEE International Conference on Field-Programmable Technology (FPT), 2006, 2007, 2008 (Program Committee Chair), 2009
10. IEEE/TSA International Symposium on VLSI Design, Automation & Test (VLSI-TSA-DAT), 2006, 2007, 2008 (Subcommittee Co-Chair), 2009 (Subcommittee Co-Chair).
11. IEEE International SOC Conference (SOCC), 2006, 2007 (Subcommittee Co-Chair).
12. IEEE Industrial Electronics Conference (IECON), 2007 (Subcommittee Chair)
13. IEEE Asia and Pacific Conference on Circuits and Systems (APCCAS), 2004.

E. **Best Paper/Most Influential Paper/Thesis Award Selection Committee**

- ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC), Yokohama, Japan, 2007, 2011 (Chair)
- IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2011, 2012 (Chair), 2024
- ACM International Symposium on Physical Design (ISPD), 2012 (Chair), 2013-2025
- ACM/IEEE Design Automation Conference (DAC), 2013, 2014, 2015, 2019, 2026 (Most Influential Paper Award)
- EDAA Outstanding Dissertations Award, 2009, 2011, 2016

F. Invited Technical Talks (Recent 5 Years)

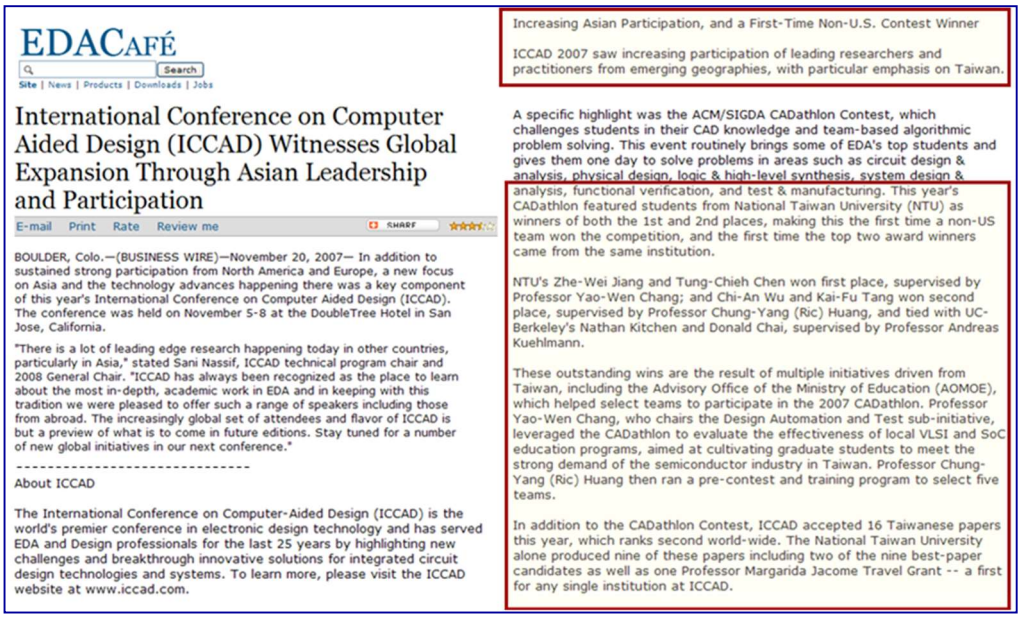
- Invited Speaker, Synopsys, June 2026
- Invited Speaker, University of Tokyo, March 2026
- Panelist, IEEE/ACM ICCAD, November 2025
- Invited Speaker, Kyoto University, November 2025
- 45th Anniversary Master Lecture (Semiconductor Technology), Hsinchu Science Park Administration (4 新竹科學園區管理局 5 周年園慶大師講座(半導體技術)), November 2025.
- Panelist, Indo-Pacific Semiconductor and AI Workshop, Tokyo, Japan, May 2025
- Panelist, IEEE/ACM ASP-DAC, January 2025
- Invited Speaker, A World Semiconductor Scholars' Forum, Buffalo, NY, November 2024
- Invited Speaker, EDA Workshop, Honk Kong, August 2024
- Keynote Speaker, VLSI Design/CAD Symposium, August 2024
- Invited Speaker, ACM/IEEE DAC, June 2024
- Keynote Speaker, ACM ISPD Keynote Speech, March 2024
- Panelist, Taiwan Science & Technology Hub @ Stanford, Stanford University, June 2022
- Keynote Speaker, IEEE/ACM ICCAD, November 2020
- Industry: Anxpert (October 2025), MediaTek (Aug. 2025), Inventec (July & Aug. 2025), TSMC (Global DTP，June 2025), Synopsys (June 2025, November 2023, November 2021), ASUS (May 2025), Delta (Sept. 2024), Win (Dec. 2024), Google (May 2024), Silvaco (November 2023, November 2022, November 2021)

G. **Industry Service** (I was not allowed to serve on any industry board or as a technical consultant between 2009 and February 2024 because of the governmental rule for a university administration officer)

1. **Independent Board Director, MediaTek Inc., May 2024-present**
2. **Co-Founder, Maxeda Technologies, 2015–2023** (through the MOST Germination Program), **acquired by Synopsys in 2023.**
3. Review Committee, Industrial Technology Research Institute (ITRI), Taiwan, 2010-2012
4. Consultant, RealTek Semiconductor Corp., Taiwan, November 2008—October 2009
5. Independent Board Director, Genesys Logic Inc., June 2007--June 2009.
6. Consultant, MediaTek Inc., Taiwan, March 2005--February 2006.
7. Consultant, Faraday Technology Corp., Taiwan, October 2004--September 2005

H. Governmental Service

1. **Chair, The Electronic Design Automation (EDA) / Design Automation and Test (DAT)** Consortia, Advisory Office, Ministry of Education, Taiwan, January 2005--February 2008
   - *Initiated "The DAC/ICCAD Promotion Program" in 2005 to improve Taiwan's publications at the DAC and ICCAD conferences; the number of Taiwan papers was quadrupled in 2008 (see Figure 2 for an EDACafe article on this program); Taiwan became the 2nd player in DAC + ICCAD publications from 2006 to 2014, just next to the USA.*
2. **Principal Investigator, Human Resource Cultivation Division & 4C Electronics Division, National Intelligent Electronics Program,** Taiwan, 2011—2013
3. Consulting Member, Taiwan Semiconductor Research Institute (TSRI), 2024-present
4. Academic Ethics and Integrity Committee, Ministry of Science and Technology, 2017-2019
5. Review Committee, Chip Implementation Center (CIC), Taiwan, 2011--2012.
6. Review Committee, National Science Council, Taiwan, 2004--2008.



EDACAFÉ

Search

Site | News | Products | Downloads | Jobs

International Conference on Computer Aided Design (ICCAD) Witnesses Global Expansion Through Asian Leadership and Participation

E-mail Print Rate Review me

BOULDER, Colo.—(BUSINESS WIRE)—November 20, 2007— In addition to sustained strong participation from North America and Europe, a new focus on Asia and the technology advances happening there was a key component of this year's International Conference on Computer Aided Design (ICCAD). The conference was held on November 5-8 at the DoubleTree Hotel in San Jose, California.

"There is a lot of leading edge research happening today in other countries, particularly in Asia," stated Sani Nassif, ICCAD technical program chair and 2008 General Chair. "ICCAD has always been recognized as the place to learn about the most in-depth, academic work in EDA and in keeping with this tradition we were pleased to offer such a range of speakers including those from abroad. The increasingly global set of attendees and flavor of ICCAD is but a preview of what is to come in future editions. Stay tuned for a number of new global initiatives in our next conference."

About ICCAD

The International Conference on Computer-Aided Design (ICCAD) is the world's premier conference in electronic design technology and has served EDA and Design professionals for the last 25 years by highlighting new challenges and breakthrough innovative solutions for integrated circuit design technologies and systems. To learn more, please visit the ICCAD website at www.iccad.com.

Increasing Asian Participation, and a First-Time Non-U.S. Contest Winner

ICCAD 2007 saw increasing participation of leading researchers and practitioners from emerging geographies, with particular emphasis on Taiwan.

A specific highlight was the ACM/SIGDA CADathlon Contest, which challenges students in their CAD knowledge and team-based algorithmic problem solving. This event routinely brings some of EDA's top students and gives them one day to solve problems in areas such as circuit design & analysis, physical design, logic & high-level synthesis, system design & analysis, functional verification, and test & manufacturing. This year's CADathlon featured students from National Taiwan University (NTU) as winners of both the 1st and 2nd places, making this the first time a non-US team won the competition, and the first time the top two award winners came from the same institution.

NTU's Zhe-Wei Jiang and Tung-Chieh Chen won first place, supervised by Professor Yao-Wen Chang; and Chi-An Wu and Kai-Fu Tang won second place, supervised by Professor Chung-Yang (Ric) Huang, and tied with UC-Berkeley's Nathan Kitchen and Donald Chai, supervised by Professor Andreas Kuehlmann.

These outstanding wins are the result of multiple initiatives driven from Taiwan, including the Advisory Office of the Ministry of Education (AOMOE), which helped select teams to participate in the 2007 CADathlon. Professor Yao-Wen Chang, who chairs the Design Automation and Test sub-initiative, leveraged the CADathlon to evaluate the effectiveness of local VLSI and SoC education programs, aimed at cultivating graduate students to meet the strong demand of the semiconductor industry in Taiwan. Professor Chung-Yang (Ric) Huang then ran a pre-contest and training program to select five teams.

In addition to the CADathlon Contest, ICCAD accepted 16 Taiwanese papers this year, which ranks second world-wide. The National Taiwan University alone produced nine of these papers including two of the nine best-paper candidates as well as one Professor Margarida Jacome Travel Grant -- a first for any single institution at ICCAD.

Figure 2: EDACafe article on the promotion program in Taiwan

7. Principal Reviewer, SBIR, Ministry of Economic Affairs, Taiwan, 2007--2011.

8. ITRI-STC Industry-Academia-Research Collaboration Committee, Taiwan, 2005--2006.
9. Executive Secretary, System-on-Chip (SOC) Consortium, Advisory Office, Ministry of Education, Taiwan, March 2001--December 2004.
10. **Contest Chair, IC/CAD Contest**, The Advisory Office, Ministry of Education, Taiwan, 2000, 2001
    - ***Initiated the annual CAD contest*** *in Taiwan in 2000, which is the 1st EDA research contest in the world and has effectively promoted EDA research and development in Taiwan; helped the domestic contest to become the International CAD contest @ ICCAD in 2012; Taiwan becomes the #1 player in this international contest*

Academic Citations

A. EE Times citations: 11 times on 2/23/1999, 4/15/2008, 4/22/2008, 4/19/2009, 4/2/2010, 4/13/2011, 4/6/2012, 3/25/2013, 5/15/2013, 4/6/2015, 4/6/2017

- EE Times Article "Taiwan: Microelectronics expertise widens" (5/15/2013): "Taiwan is already the number one producer worldwide of notebook PCs, LCD monitors, chip-testing and chip-foundry services," said IEEE Fellow and associate dean of the Electrical Engineering and Computer Science College at NTU, Yao-Wen Chang. "Our microelectronics companies include the number one contract manufacturer, Hon Hoi [Foxconn], the number one chip foundry, TSMC, and the number one maker of notebook PCs and servers, Quanta Computer." **Taiwan's success so far has been in large part due to electronic design automation (EDA) expertise, where it has only been outperformed by the U.S. for the last five years** -- as measured by number of research papers it presented at the IEEE's Design Automation Conference (DAC) and International Conference on Computer Aided Design (ICCAD). **Chang is typical at NTU, a microelectronics pioneer in EDA, due to receive four separate awards at DAC 2013's 50th anniversary celebration next month, all related to his unstoppable stream of DAC research papers presenting deep insights into EDA.**

- **'The Best and Brightest Worldwide'** by R. Colin Johnson (4/6/2015): **"The best engineering minds on the planet compete each year in the ACM's ISPD design contest, which was won this year by the National Taiwan University"**

- "ISPD: Semiconductors aim for 8-nm nodes" (4/6/2012): "**The winner was team from National Taiwan University led by Professor Yao-Wen Chang**."

- IEEE Design & Test of Computers is currently conducting a special series of reports on "**A Series of Influential Scholars in EDA**", which will be published in 2025. **Professor Chang was selected as a featured scholar due to his outstanding contribution and impact on the global EDA field.**



EE Times

Taiwan: Microelectronics expertise widens

R Colin Johnson

5/15/2013 12:14 PM EDT

TAIPEI -- Taiwan is well known as a microelectronics manufacturing powerhouse for innovations "Designed in California" as Apple puts it. Now, however, the island country is making a concerted effort to pioneer its own electronics innovations -- starting at its National Taiwan University (NTU), whose government-sponsored research labs are prepping for home-grown electronics with mass-market appeal.

National Taiwan University's island-wide campuses and government-funded research facilities comprise one percent of the land area on the island nation. SOURCE: NTU

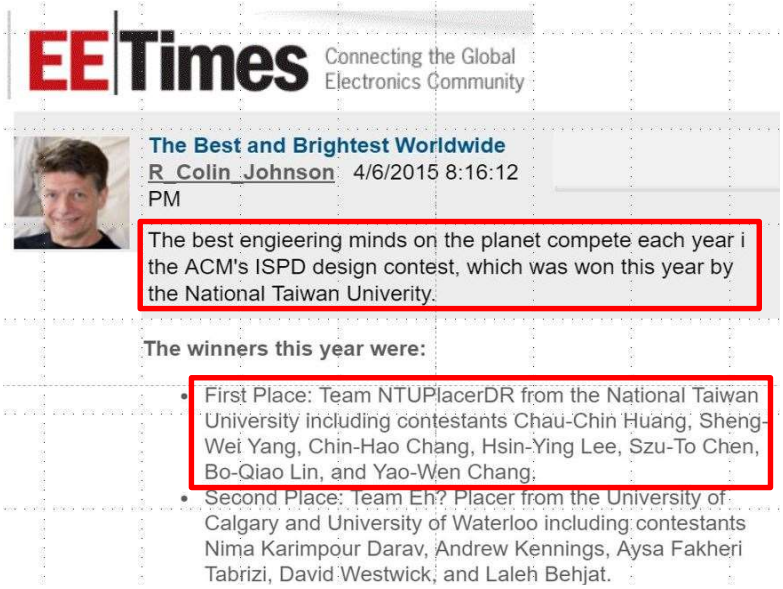
From EDA to KDD

Taiwan's success so far has been in large part due to electronic design automation (EDA) expertise, where it has only been outperformed by the U.S. for the last five years -- as measured by number of research papers its presented at the IEEE's Design Automation Conference (DAC) and International Conference on Computer Aided Design (IC-CAD).

"Taiwan is already the number one producer worldwide of notebook PCs, LCD monitors, chip-testing and chip-foundry services," said IEEE Fellow and associate dean of the Electrical Engineering and Computer Science College at NTU, Yao-Wen Chang. "Our microelectronics companies include the number one contract manufacturer, Hon Hoi [Foxconn], the number one chip foundry, TSMC, and the number one maker of notebook PCs and servers, Quanta Computer."

Chang is typical at NTU, a microelectronics pioneer in EDA, due to receive four separate awards at DAC 2013's 50th anniversary celebration next month, all related to his unstoppable stream of DAC research papers presenting deep insights into EDA. Shao-Yun Fang, his prize student, last year gave an Association for Computing Machinery (ACM) Grand Final Paper, then spent her

Figure 3: EE Times article on National Taiwan University and Yao-Wen Chang



EE Times Connecting the Global Electronics Community

The Best and Brightest Worldwide

R_Colin_Johnson 4/6/2015 8:16:12 PM

The best engieering minds on the planet compete each year i the ACM's ISPD design contest, which was won this year by the National Taiwan Univerity.

The winners this year were:

- First Place: Team NTUPlacerDR from the National Taiwan University including contestants Chau-Chin Huang, Sheng-Wei Yang, Chin-Hao Chang, Hsin-Ying Lee, Szu-To Chen, Bo-Qiao Lin, and Yao-Wen Chang.
- Second Place: Team Eh? Placer from the University of Calgary and University of Waterloo including contestants Nima Karimpour Darav, Andrew Kennings, Aysa Fakheri Tabrizi, David Westwick, and Laleh Behjat.

Figure 4: Senior Editor C. Johnson (Kyoto Prize Winner) of EE Times (4/6/2015): “The Best and Brightest Worldwide: The best engineering minds on the planet compete each year in the ACM's ISPD design contest, which was won this year by the National Taiwan University.”

B. #1 worldwide among 40K+ researchers in latest 5-year citation count in the Hardware & Architecture Domain, Microsoft Academic Search, during December 2010 to February 2011 **(**see Figure 5 from http://academic.research.microsoft.com/; the system was retired in 2011)

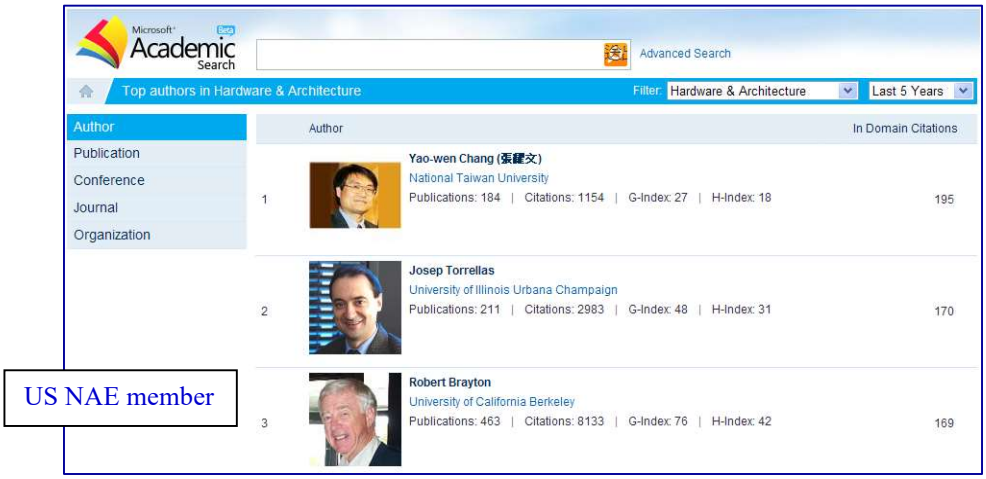


Figure 5: Latest 5-year citation count ranking in Hardware & Architecture Domain, Microsoft Academic Search (December 2010)

C. World's Top 2% Scientists named by Stanford University (Career-long & Single-year).

D. ScholarGPS ranks him 8th globally (top 0.06%) in lifetime EDA impact, the only Taiwan-affiliated scholar listed in the top 0.5%, 2026



Figure 6: EDA contest **champions**. Left to right in the top row: 2012 DAC Placement Contest; 2012 ISPD Discrete Gate Sizing Contest, 2011 IEEE CEDA PATMOS Timing Analysis Contest, 2009 ISPD Clock Network Synthesis; bottom row: 2013 CAD Contest at ICCAD, 2015 ISPD Placement Contest, 2023 CAD Contest at ICCAD (Problem B), and 2024 CAD Contest at ICCAD (Problem B)



Figure 7: 2025 ICCAD William J. McCalla Best Paper Award (1st place out of 1078 submissions); the only best paper award from Taiwan in ICCAD's 44-year history. (Received unanimous perfect scores from all seven Best Paper Committee members.)



Figure 8: 2017 DAC Best Paper Award (1st place out of about 700 papers); the only all-conference best paper award from Taiwan in DAC's 62-year history.



Figure 9: (left) 2015 IEEE CEDA Outstanding Service Award；(right) 2012 ACM Service Award.



Figure 10: IEEE Fellow presentation by the IEEE CEDA President, Professor Donatella Sciuto

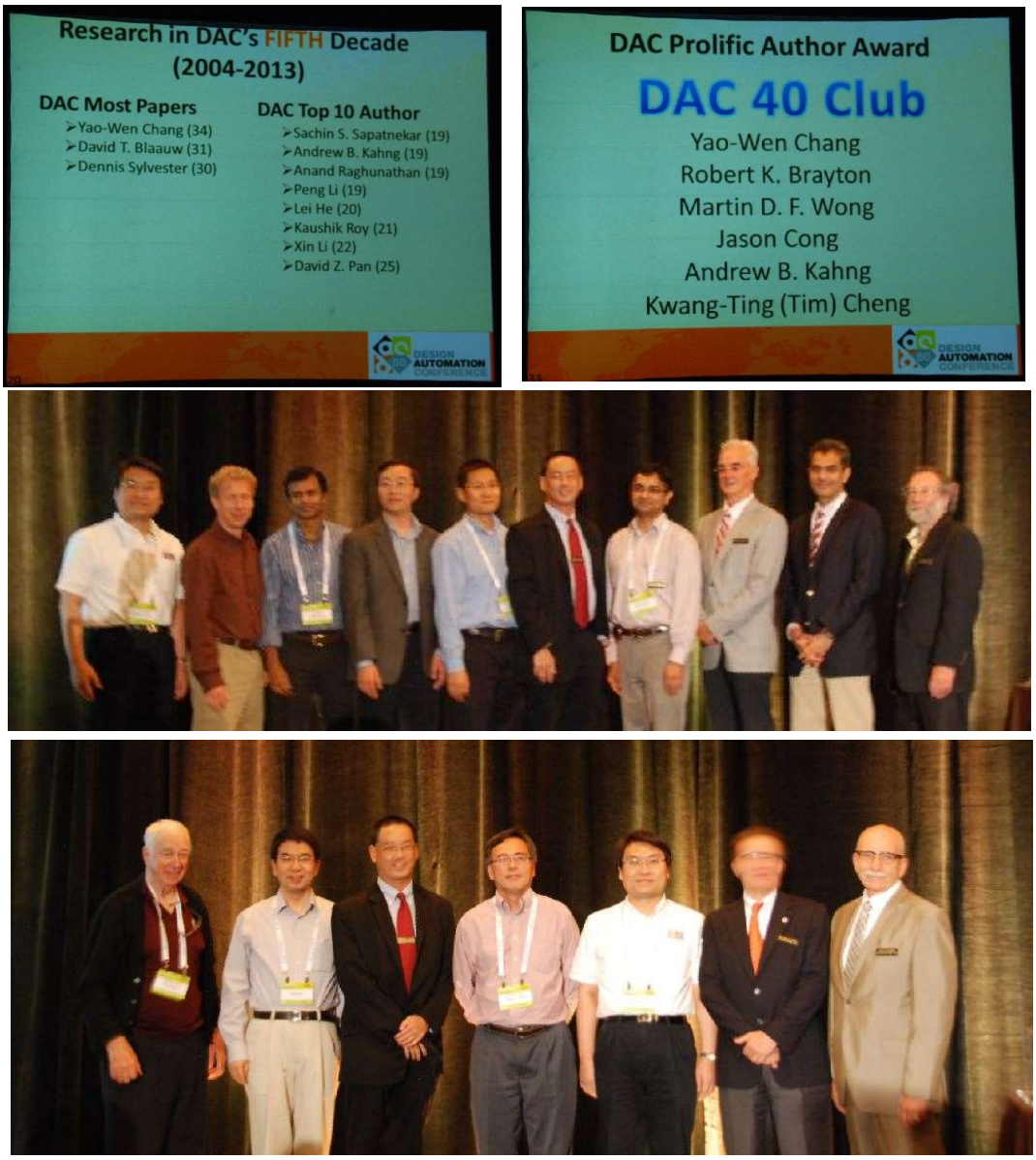


Figure 11: Research achievement award presentation at the 50th ACM/IEEE DAC in 2013. Yao-Wen Chang received four awards (the youngest scholar to receive these four awards; #1 in Asia) (top-left: most (34) papers in the 5th decade, #1 worldwide; top-right: youngest DAC 40 Club member, the only non-US winner; 2nd row: top authors in the 5th decade, ranked from left to right, with Yao-Wen Chang being the #1; 3rd row: 40 Club members & the award presenter (Note that Robert K. Brayton, Jason Cong, and Giovanni De Micheli were Phil Kaufman Award receipts, a.k.a. the Nobel Prize in EDA, and the US NAE members)



Figure 12: (left) IEEE TAB Meeting at Tampa, Florida as the CEDA President-elect, February 2019; (right) IEEE TAB Meeting at Orlando, Florida, February 2020; Photo with IEEE Society/Council presidents (1st from left in the 6th row)



Figure 13: IEEE/ACM ASP-DAC Prolific Author Award in January 2020



Figure 14: (Top Row) TECO Award in 2017; (Left in the Middle Row) Distinguished Research Award from the Pan Wen Yuan Foundation in 2020; (Right in the Middle Row) Academic Award from the Ministry of Education in 2021; (Left in the Bottom Row) Y. Z. Hsu Science Chair Professorship (Information and Communication) in 2022; (Right in the Bottom Row) Distinguished Research Fellow from the National Science and Technology Council (formerly Ministry of Science and Technology) in 2023



Figure 15: Guiding a student to win the first place in the DAC'12 Placement Contest and in the graduate category of the 2012 ACM/SIGDA Student Research Competition)



Figure 16: The student team he supervised launched Taiwan's path to the ACM CADathlon Contest championship in 2007 (won the championship again in 2012 and was the runner-up in 2023); left: ICCAD announcement of the championship in 2012; Right: winners at the 2012 and 2007 competitions

今周刊
王子承 分類 | 科技
1400期
2023-10-18 12:18

獲利穩定還有大咖客戶 EDA新星為何要賣？ 龍頭新思跨海併購 解密台20人新創至達



天下雜誌 CommonWealth Magazine
文—施貝怡・天下雜誌801期
發布時間：2024-06-25

出身公務員家庭的台灣EDA新星　AI研發如何超越Google？

EE Times
News & Analysis

Synopsys to buy SpringSoft for $406 million

Peter Clarke
8/3/2012 10:27 AM EDT

Synopys said it plans to integrate the physical design technology and R&D teams from Springsoft, Ciranova and Magma and thereby offer a higher level of automation in custom implementation tools.

EE Times
Product News

SpringSoft presents IC place-and-route tools

AnneFrancoise PELE
3/15/2010 03:00 PM EDT

PARIS — Taiwanese EDA company SpringSoft Inc. (Hsinchu, Taiwan) announced it has expanded its Laker custom IC design platform with the introduction of Laker Custom Row Placer and Laker Custom Digital Router.

Laker Custom Row Placer uses proprietary automation techniques to achieve incremental selection and placement as well as internal iterations to pack the placement area, SpringSoft said.

It utilizes stacking utilities for datapath-style placement. The row placer also assists routing with features for row snapping and overlap removal as well as diffusion sharing for area minimization, the EDA firm said.

Figure 17: (Top) Business Today (10/18/2023) reported that Maxeda, a joint venture founded in 2015, was acquired by Synopsys, the largest EDA company; CommonWealth Magazine (6/25/2024) reported on Maxeda's technology and Synopsys merger and acquisition; (Bottom left) EE Times report (8/3/2012): SpringSoft was acquired by Synopsys; (Bottom right) EE Times report (3/15/2010): SpringSoft announced Laker Custom Placer (renamed from NTUplace3 developed by our laboratory).

工商時報 COMMERCIAL TIMES

聯發科獨董微調 張耀文入列

2024.04.03 / 03:00 / 工商時報　張珈睿

Figure 18: Professor Chang was appointed an independent board director of MediaTek



EE Times News & Analysis

ISPD: Semiconductors aim for 8-nm node

R. Colin Johnson

4/6/2012 12:35 PM EDT

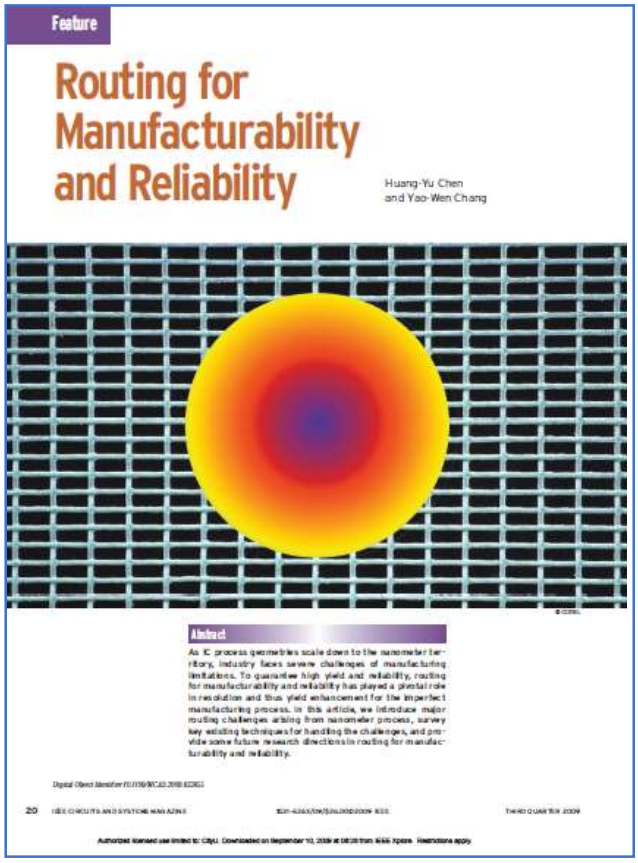
PORTLAND, Ore.—The possible pathways down to the 8-nanometer semiconductor fabrication node were detailed last week at the ACM **International Symposium on Physical Design** (ISPD) in Napa, Calif., albeit through a glass darkly. What's for sure is that the pathway is fraught with engineering peril as three competing technologies tool up for mass production capabilities. However, keynote speaker Burn Lin, a TSMC distinguished Fellow, claimed that one of three alternatives was sure to surmount the downward scaling hurdles to 8-nm design rules.

One of the best paper nominees at this year's ISPD was from professor Yao-Wen Chang's group at National Taiwan University, which addressed the overheating problems of massive e-beam writing processes, achieved by reordering the writing sequence to better control dimensional distortions.

Comments

There was also the annual contest, this year on discrete gate sizing, organized by an Intel team led by research scientist Mustafa Ozdal at Intel Strategic CAD Labs. 32 academic and industrial teams from four different continents entered the contest with 18 teams making it through to the submissions phase. The winner was team from National Taiwan University led by professpr Yao-Wen Chang and his graduate students Kuan-Hsien Ho, Po-Ya Hsu, and Yu-Chen Chen. Second plance went to a team from Universidade Federal do Rio Grande do Sul, Brazil, led by professor Marcelo Johann. And third place went to a joint team of National Tsing-Hua University and Missouri University of Science and Technology led by professors Yiyu Shi and Shih-Chieh Chang.

Figure 19: ebeam research results were reported by EE Times (4/6/2012)



Feature

Routing for Manufacturability and Reliability

Huang-Yu Chen and Yao-Wen Chang

Abstract

As IC process geometries scale down to the nanometer territory, industry faces severe challenges of manufacturing limitations. To guarantee high yield and reliability, routing for manufacturability and reliability has played a pivotal role in resolution and thus yield enhancement for the imperfect manufacturing process. In this article, we introduce major routing challenges arising from nanometer process, survey key existing techniques for handling the challenges, and provide some future research directions in routing for manufacturability and reliability.

Figure 20: Invited feature article "Routing for Manufacturability and Reliability" (September 2009) in *IEEE Circuit and System Magazine*

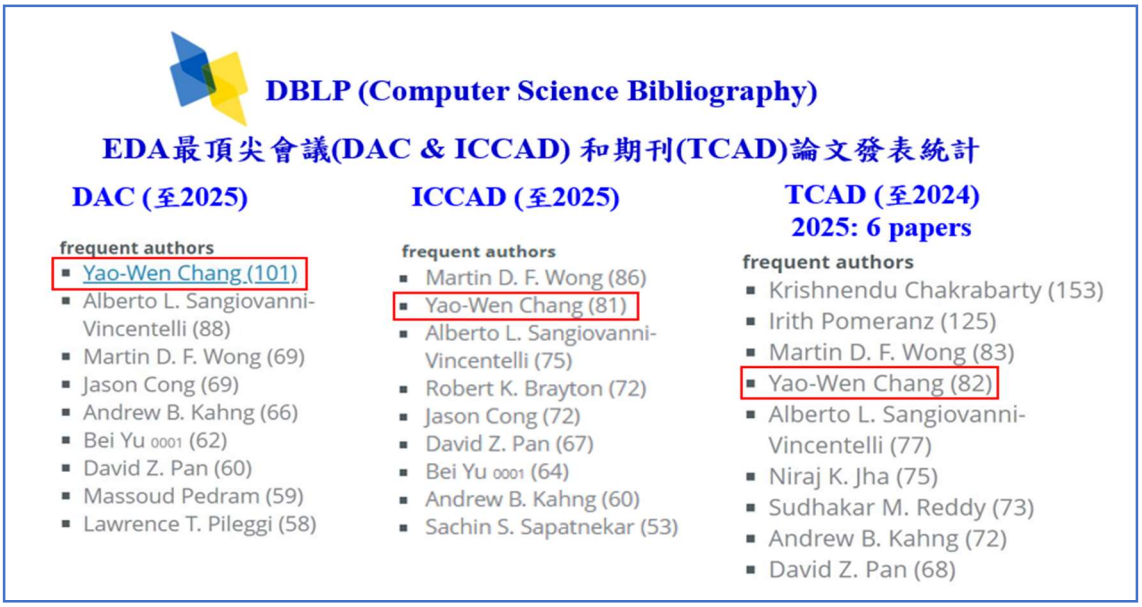
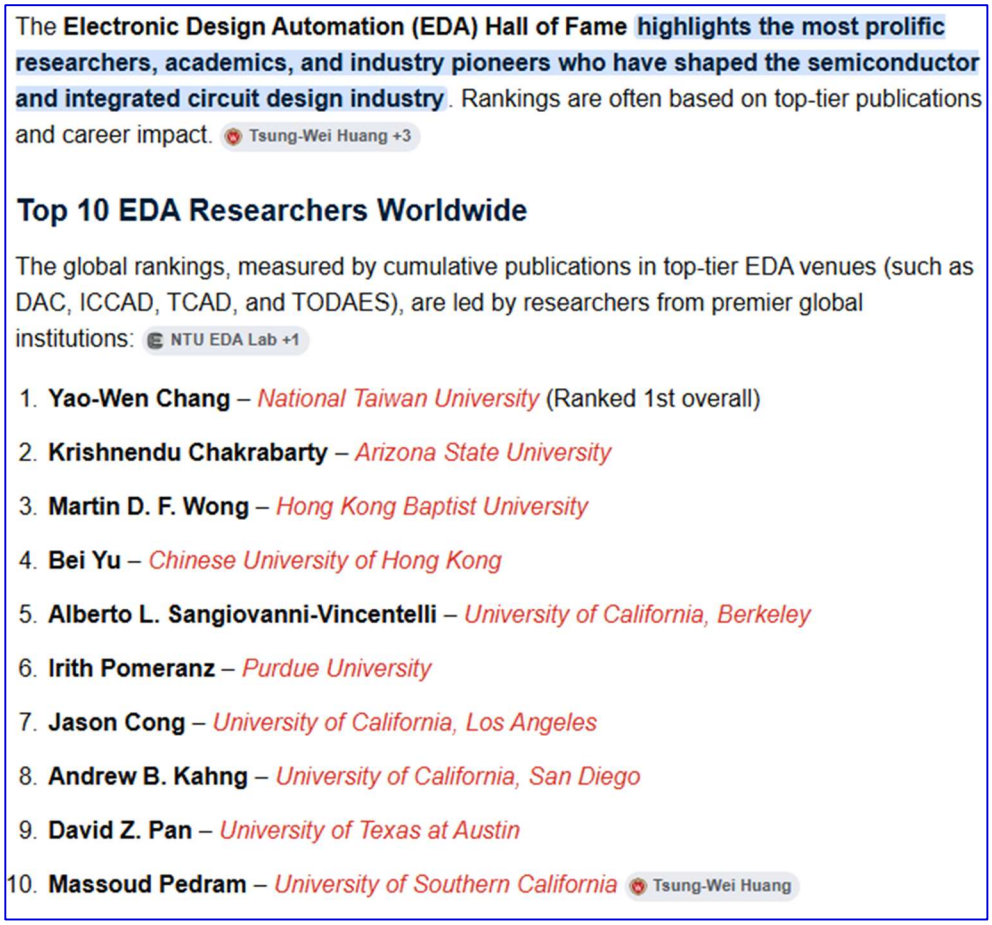


Figure 21: DBLP statistics on the top EDA conference (DAC and ICCAD) and journal (IEEE TCAD) publications (Note that Alberto L. Sangiovanni-Vincentelli, Jason Cong, Lawence T. Pileggi, and Robert K. Brayton were Phil Kaufman Award receipts, a.k.a. the Nobel Prize in EDA), as of 12/2025



Figure 22: 2026 IEEE CEDA Distinguished Service Award



The **Electronic Design Automation (EDA) Hall of Fame highlights the most prolific researchers, academics, and industry pioneers who have shaped the semiconductor and integrated circuit design industry**. Rankings are often based on top-tier publications and career impact. Tsung-Wei Huang +3

Top 10 EDA Researchers Worldwide

The global rankings, measured by cumulative publications in top-tier EDA venues (such as DAC, ICCAD, TCAD, and TODAES), are led by researchers from premier global institutions: NTU EDA Lab +1

1. **Yao-Wen Chang** – *National Taiwan University* (Ranked 1st overall)
2. **Krishnendu Chakrabarty** – *Arizona State University*
3. **Martin D. F. Wong** – *Hong Kong Baptist University*
4. **Bei Yu** – *Chinese University of Hong Kong*
5. **Alberto L. Sangiovanni-Vincentelli** – *University of California, Berkeley*
6. **Irith Pomeranz** – *Purdue University*
7. **Jason Cong** – *University of California, Los Angeles*
8. **Andrew B. Kahng** – *University of California, San Diego*
9. **David Z. Pan** – *University of Texas at Austin*
10. **Massoud Pedram** – *University of Southern California* Tsung-Wei Huang

Figure 23: Top-10 researchers in the EDA Hall of Fame in 2026 (inaugural year)

Publication List

A. **Journal/Magazine Papers (Top EDA journal: IEEE TCAD; published 92 TCAD papers (#4 worldwide**; others: ACM TODAES: 12; IEEE TVLSI: 5; IEEE TC: 3; IEEE D&T: 3; CACM: 1; ACM JETC: 1; IEEE CASM: 1**)**

1. Z.-H. Wu, B.-Y. Huang, Y.-C. Chen, and Y.-W. Chang, "Parallel non-integer multiple-cell-height node remapping," to appear in *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, August 2026.
2. C.-Y. Chiang, Z.-Y. Cai, C.-C. Lan, Y.-J. Chen, Y. Hsu, Y.-W. Chang, and H.-M. Chen, "Scalable GPU-friendly parallelization for sweep-based maze routing," to appear in *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD),* August 2026.
3. C-Y. Ou, Y.-J. Chen, and Y.-W. Chang, "Constraint graph-based irregular PCB legalization considering complex clearance constraints," to appear in *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Early Access, vol. 45, August 2026. (DOI: 10.1109/TCAD.2026.3721418)
4. C.-Y. Li, C.-C. Su, Z.-W. Chen, S.-H. Chen, and Y.-W. Chang, "Multi-objective multi-bit flip-flop placement considering pe-placed cells," to appear in *IEEE Trans. Computer-Aided Design*

of Integrated Circuits and Systems (TCAD), Early Access, vol. 45, March 2026. (DOI: 10.1109/TCAD.2026.3677761)

5. W.-C. Tseng, Z.-Y. Cai, Y.-P. Huang, Y.-H. Lo, Y.-W. Chang, Y. Lu, J. Bai, and B.-C. Tseng, "Rail routing for power distribution networks in advanced multi-layered printed circuit boards," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 44, December 2025. (DOI: 10.1109/TCAD.2025.3649456)
6. W.-Y. Kao, T.-J. Lin, and Y.-W. Chang, "Provably good physically aware WRONoC design for customized and fault-tolerant topologies with parallel switching elements and sequence-based models," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD),* vol. 44, no. 12, December 2025 (early access: DOI: 10.1109/TCAD.2025.3648675)
7. S.-Y. Lo, M. Liu, and Y.-W. Chang, "Efficient high-fidelity warpage modeling for advanced packaging analysis," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 45, No. 5, pp. 2249—2262, May 2026.
8. C.-H. Tsou, S.-Y. Lin, W.-C. Hung, and Y.-W. Chang, "Modern automatic PCB placement with complex constraints," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 45, No. 5, pp. 2152--2163, May 2026.
9. H.-Y. Chang and Y.-W. Chang, "Simultaneous power and signal PCB routing considering complex clearance constraints with arbitrary wire widths," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 45, No. 5, pp. 2141—2151, May 2026.
10. J.-W. Chuang, Z.-H. Wu, B.-Y. Huang, and Y.-W. Chang, "Redistribution layer routing with dynamic via insertion under irregular via structures," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD),* vol. 45, no. 1, pp. 466—479, January 2026.
11. Y.-W. Chang and D. Z. Pan, "Physical design for heterogeneous integration: challenges and opportunities," *IEEE Design & Test (D&T)*, Vol. 42, No. 6, December 2025 **(invited article)**
12. D. Z. Pan, Y.-W. Chang, C.-H. Hsu, and Y. Hsu, "From classical algorithms to AI: evolving trends in VLSI physical design automation," *IEEE Design & Test (D&T),* Vol. 42, No. 6, December 2025 **(invited article)**
13. C. Chen, D. Lin, Q. Liu, H. He, Z. Lin, G. Liu, J. Chen, and Y.-W. Chang, "A matching based escape routing algorithm with variable design rules and multiple constraints," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD),* vol. 44, No. 12, pp. 4765--4778, December 2025.
14. W.-H. Tseng and Y.-W. Chang, "A bridge-based algorithm for simultaneous primal and dual defects compression on topologically quantum-error-corrected circuits," *ACM Trans. Design Automation of Electronic Systems (TODAES)*, Vol. 29, October 2024 (22 pages)
15. Z. Zhu, Y. Mei, K. Deng, H. He, J. Chen, J. Yang, and Y.-W. Chang, "High-performance placement engine for modern large-scale FPGAs with heterogeneity and clock constraints," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 43, no. 3, pp. 956—969, March 2024.
16. J. Chen, W. Zhu, J. Yu, L. He, and Y.-W. Chang, "Analytical placement with 3D Poisson's equation and ADMM based optimization for large-scale 2.5D heterogeneous FPGAs," *ACM Trans. Design Automation of Electronic Systems (TODAES)*, Vol. 28, Issue 5, Article No. 70,

September 2023 (24 pages)
17. P.-W. Huang and Y.-W. Chang, "Routability-driven power/ground network optimization based on machine learning," *ACM Trans. Design Automation of Electronic Systems (TODAES)*, Vol. 28, Issue 4, Article No. 53, May 2023 (27 pages)
18. W.-H. Tseng, C.-H. Hsu, W.-H. Lin, and Y.-W. Chang, "A bridge-based compression algorithm for topological quantum circuits," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD),* vol. 41, No. 12, pp. 5582-5595, December 2022.
19. H.-T. Wen, Y.-J. Cai, Y. Hsu, and Y.-W. Chang, "Via-based redistribution layer routing for InFO packages with irregular pad structures," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD),* vol. 41, No. 12, pp. 5554-5567, December 2022.
20. J. Chen, Z. Huang, Z. Zhu, Z. Peng, W. Zhu, and Y.-W. Chang, "Novel proximal group ADMM for placement considering fogging and proximity effects," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 41, No. 12, pp. 5541-5553, December 2022.
21. Y.-S. Lu, S.-J. Yu, and Y.-W. Chang, "On-chip optical routing with provably good algorithms for path clustering and assignment," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD),* vol. 41, No. 11, pp. 4653-4666, November 2022.
22. J. Chen, Z. Lin, Y. Xie, W. Zhu, and Y.-W. Chang, "Mixed-cell-height placement with complex minimum-implant-area constraints," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 41, No. 11, pp. 4639-4652, November 2022.
23. X. Bai, Z. Zhu, P. Li, J. Chen, T. Lan, X. Li, J. Yu, W. Zhu, and Y.-W. Chang, "Timing-aware fill insertions with design-rule and density constraints," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 41, No. 10, pp. 3529-3542, October 2022.
24. Y.-S. Lu, Y.-L. Chen, S.-J. Yu, and Y.-W. Chang, "Topological structure and physical layout co-design for wavelength-routed optical networks-on-chip," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD),* vol. 41, No. 7, pp. 2237-2249, July 2022.
25. J. Chen, Z. Zhu, L. Guo, Y.-W. Tseng, and Y.-W. Chang, "Mixed-cell-height placement with drain-to-drain abutment and region constraints," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 41, No. 4, pp. 1103-1115, April 2022.
26. J. Chen, Y.-W. Chang, and Y.-Y. Wu, "Mixed-cell-height detailed placement considering complex minimum-implant-area constraints," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD),* Vol. 40, No. 10, pp. 2128-2141, October 2021.
27. C.-H. Hsu, S.-C. Hung, H. Chen, F.-K. Sun, and Y.-W. Chang, "A DAG-based algorithm for obstacle-aware topology-matching on-track bus routing," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD),* Vol. 40, No. 3, pp. 533-541, March 2021.
28. J. Chen, Y.-W. Chang, and Y.-C. Huang, "Analytical placement considering the electron beam fogging effect," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD),* Vol. 40, No. 3, pp. 560--573, March 2021.
29. J. Chen, Z. Zhu, W. Zhu, and Y.-W. Chang, "A robust modulus-based matrix splitting iteration method for mixed-cell-height circuit legalization," *ACM Trans. Design Automation of Electronic Systems (TODAES)*, Vol. 26, No. 2, Article 15, pp. 1-28, February 2021.
30. Z. Zhu, J. Chen, W. Zhu, and Y.-W. Chang, "Mixed-cell-height legalization considering

technology and region constraints," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 39, No. 12, pp. 5128—5141, December 2020.

31. J. Chen, Z. Lin, Y.-C. Kuo, C.-C. Huang, Y.-W. Chang, S.-C. Chen, C.-H. Chiang, and S.-Y. Kuo, "Clock-aware placement for large-scale heterogeneous FPGAs," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 39, No. 12, pp. 5042—5055, December 2020.
32. Y.-H. Su and Y.-W. Chang, "DSA-compliant routing for 2-D patterns using block copolymer lithography," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD),* Vol. 38, No. 2, pp. 267—280, February 2019.
33. C.-C. Huang, H.-Y. Lee, B.-Q. Lin, S.-W. Yang, C.-H. Chang, S.-T. Chen, Y.-W. Chang, T.-C. Chen, and I. Bustany, "NTUplace4dr: a detailed-routing-driven placer for mixed-size circuit designs with technology and region constraints," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 37, Vol. 3, pp. 669--681, March 2018.
34. Z.-W. Lin and Y.-W. Chang, "Provably good max-min-m-neighbor-TSP-based subfield scheduling for electron-beam photomask fabrication," *IEEE Trans. Very Large Scale Integration Systems (TVLSI)*, Vol. 26, No. 2, pp. 378--391, February 2018.
35. Z.-W. Lin and Y.-W. Chang, "Cut redistribution with directed self-assembly templates for advanced 1-D gridded layouts," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 36, No. 12, pp. 2066--2079, December 2017.
36. Y.-W. Chang, "An interview with Professor Chenming Hu, father of 3D transistors," *IEEE Design & Test (D&T)*, Vol. 34, Issue 5, pp. 90-96, October 2017
37. Y.-H. Su and Y.-W. Chang, "Nanowire-aware routing considering high cut mask complexity," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 36, No. 6, pp. 964--977, June 2017.
38. I.-J. Liu, S.-Y. Fang, and Y.-W. Chang, "Overlay-aware detailed routing for self-aligned double patterning lithography using the cut process," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 35, No. 9, pp. 1519–1531, September 2016.
39. Y.-H. Su, Y.-C. Huang, L.-C. Tsai, Y.-W. Chang, and S. Banerjee, "Fast lithographic mask optimization considering process variation," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 35, No. 8, pp. 1345—1357, August 2016.
40. H.-C. Ou, K.-H. Tseng, J.-Y. Liu, I-P. Wu, and Y.-W. Chang, "Layout-dependent-effects-aware analytical analog placement," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 35, No. 8, pp. 1243—1254, August 2016.
41. H.-J. K. Chiang, C.-Y. Liu, J.-H. R. Jiang, and Y.-W. Chang, "Simultaneous EUV flare variation minimization and CMP control by coupling-aware dummification," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 35, No. 4, pp. 598—610, April 2016.
42. I.-J. Liu, S.-Y. Fang, and Y.-W. Chang, "Stitch-aware routing for multiple e-beam lithography," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD),* Vol. 34, No. 3, pp. 471—482, March 2015.
43. K.-H. Ho, H.-C. Ou, Y.-W. Chang, and H.-F. Tsao, "Coupling-aware length-ratio-matching

routing for capacitor arrays in analog integrated circuits," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD),* Vol. 34, No. 2, pp. 161--172, February 2015.

44. H.-C. Ou, H.-C. Chang Chien, and Y.-W. Chang, "Non-uniform multilevel analog routing with matching constraints," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD),* Vol. 33, No. 12, p. 1942—1954, December 2014.
45. M.-K. Hsu, Y.-F. Chen, C.-C. Huang, S. Chou, T.-H. Lin, T.-C. Chen, and Y.-W. Chang, "NTUplace4h: A novel routability-driven placement algorithm for hierarchical mixed-size circuit designs," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD),* Vol. 33, No. 12, pp. 1914—1927, December 2014.
46. S.-Y. Fang, Y.-W. Chang, and W.-Y. Chen, "A novel layout decomposition algorithm for triple patterning lithography," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 33, No. 3, pp. 397—408, March 2014.
47. Y.-K. Ho, H.-C. Lee, P.-W. Lee, Y.-W. Chang, C.-F. Chang, I.-J. Lin, and C.-F. Shen, "Obstacle-avoiding free-assignment routing for flip-chip designs," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 33, No. 2, pp. 224—236, February 2014.
48. H.-Y. Chang, I. H.-R. Jiang, Y.-W, Chang, "ECO optimization using metal-configurable gate-array spare cells," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 32, No. 11, pp. 1722—1733, November 2013.
49. Y.-K. Ho, H.-C. Lee, and Y.-W. Chang, "Escape routing for staggered-pin-array PCBs," in *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 32, No. 9, pp. 1347—1356, September 2013.
50. Y.-W. Chang, "Technical perspective: circuit placement challenges," *Communications of the ACM (CACM)*, Vol. 56, No. 6, p. 104, June 2013. **(Invited article)**
51. M.-K. Hsu, V. Balabanov, and Y.-W. Chang, "TSV-aware analytical placement for 3D IC designs based on a novel weighted-average wirelength model," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 32, No. 4, pp. 497—509, April 2013. **(2014 TCAD best paper runner-up)**
52. S.-Y. Fang, W.-Y. Chen, and Y.-W. Chang, "Graph-based subfield scheduling for electron-beam photomask fabrication," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 32, No. 2, pp. 189—201, February 2013.
53. H.-Y. Chang, H.-R. Jiang, and Y.-W. Chang, "Timing ECO optimization via B'zier curve smoothing and fixability identification," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 31, No. 12, pp. 1857--1866, December 2012.
54. K.-H. Ho, J.-H. Jiang, and Y.-W. Chang, "TRECO: Dynamic technology remapping for timing engineering change orders," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 31, No. 11, pp. 1723--1733, November 2012.
55. M.-K. Hsu and Y.-W. Chang, "Unified analytical global placement for large-scale mixed-size circuit designs," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 31, No. 9, pp. 1366-1378, September 2012.
56. X.-W. Shih and Y.-W. Chang, "Fast timing-model independent buffered clock-tree synthesis,"

IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD), Vol. 31, No. 9, pp. 1393-1404, September 2012.

57. C.-W. Lin, P.-W. Lee, Y.-W. Chang, C.-F. Shen, and W.-C. Tseng, "An efficient pre-assignment routing algorithm for flip-chip designs," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 31, No. 6, pp. 878--889, June 2012.
58. S.-Y. Fang, S.-Y. Chen, and Y.-W. Chang, "Native-conflict-aware wire perturbation for double patterning technology," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 31, No. 5, pp. 703-716, May 2012.
59. Y.-L. Chuang, S. Kim, Y. Shin, and Y.-W. Chang, "Pulsed-latch aware placement for timing-integrity optimization," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 30, No. 12, pp. 1856--1869, December 2011.
60. Y.-L. Chuang, P.-W. Lee, and Y.-W. Chang, "Voltage-drop aware analytical placement by global power spreading for mixed-size circuit designs," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 30, no. 11, pp. 1649 – 1662, November 2011.
61. C.-Y. Lin and Y.-W. Chang, "Cross-contamination aware design methodology for pin-constrained digital microfluidic biochips," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)* pp. 817--828, Vol. 30, No. 6, June 2011.
62. M. P.-H. Lin, H. Zhang, M. D. F. Wong, and Y.-W. Chang, "Thermal-driven analog placement considering device matching," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, pp. 325--336, Vol. 30, No. 3, March 2011.
63. C.-H. Hsu, Y.-W. Chang, and S. R. Nassif, "Simultaneous layout migration and decomposition for double patterning technology," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 30, No. 9, pp. 284--294, February 2011.
64. C.-Y. Lin and Y.-W. Chang, "ILP-based pin-count aware design methodology for microfluidic biochips," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 29, No. 9, pp. 1315--1327, September 2010.
65. C.-H. Hsu, H.-Y. Chen, and Y.-W. Chang, "Multi-layer global routing with via and wire capacity considerations," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 29, No. 5, pp. 685-696, May 2010.
66. K.-H. Ho, Y.-P. Chen, J.-W. Fang, and Y.-W. Chang, "ECO timing optimization using spare cells and technology remapping," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 29, No. 5, pp. 697-710, May 2010.
67. J.-W. Fang and Y.-W. Chang, "Area-I/O flip-chip routing for chip-package co-design considering signal skews," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 29, No. 5, pp. 711-721, May 2010.
68. T.-C. Chen, G.-W. Liao, and Y.-W. Chang, "Predictive formulae for OPC with applications to lithography-friendly routing," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 29, No. 1, pp. 40-51, January 2010.
69. P.-H. Yu, S. Sapatnekar, C.-L. Yang, and Y.-W. Chang, "A progressive-ILP-based routing algorithm for the synthesis of cross-referencing biochips," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 28, No. 9, pp. 1295—1305, September

2009.

70. P.-H. Yu, C.-L. Yang, and Y.-W. Chang, "T-trees: A tree-based representation for temporal floorplanning," *ACM Trans. Design Automation of Electronic Systems (TODAES)*, Vol. 14, Issue 4, August 2009. (28 pages)
71. H.-Y. Chen and Y.-W. Chang, "Routing for manufacturability and reliability," *IEEE Circuits and Systems Magazine (CASM),* pp. 20—31, September 2009 **(Invited Feature Article)**.
72. Y.-W. Chang, Z.-W. Jiang, and T.-C. Chen, "Essential issues in analytical placement algorithms," *IPSJ Transactions on System LSI Design Methodology*, August 2009 **(Invited Paper)**.
73. P.-H. Lin, Y.-W. Chang, and S.-C. Lin, "Analog placement based on symmetry-island and tree formulation," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 28, No. 6, pp. 791—804, June 2009.
74. W.-P. Lee, H.-Y. Liu, and Y.-W. Chang, "Voltage island partitioning and floorplanning under timing constraints," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 28, No. 5, pp. 690--702, May 2009.
75. H.-Y. Chen, S.-J. Chou, S.-L. Wang, and Y.-W. Chang, "A novel wire-density-driven full-chip routing system for CMP variation control," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD),* Vol. 28, No. 1, pp. 193—206, February 2009.
76. J.-W. Fang, C.-H. Hsu, and Y.-W. Chang, "An integer-linear-programming-based routing algorithm for flip-chip designs," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD),* Vol. 28, No. 1, pp. 98—110, January 2009.
77. T.-C. Chen, M. Cho, D. Z. Pan, and Y.-W. Chang, "Metal-density-driven placement for CMP variation and routability," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 27, No. 12, pp. 2145—2155, December 2008.
78. C.-W. Lin, S.-L. Huang, K.-C. Hsu, M.-X. Li, and Y.-W. Chang, "Multilayer obstacle-avoiding rectilinear Steiner tree construction based on spanning graphs," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 27, No. 11, pp. 2007—2016, November 2008.
79. P.-H. Yu, C.-L. Yang, and Y.-W. Chang, "BioRoute: a network-flow-based routing algorithm for the synthesis of digital microfluidic biochips," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 27, No. 11, pp. 1928—1941, November 2008.
80. T.-C. Chen, P.-H. Yuh, Y.-W. Chang, F.-J. Huang, and D. Liu, "MP-trees: A packing-based macro placement algorithm for modern mixed-size designs," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 27, No. 9, pp. 1621--1634, September 2008.
81. C.-H. Liu, H.-Y. Liu, C.-W. Lin, S.-J. Chou, Y.-W. Chang, S.-Y. Kuo, and S.-Y. Yuan, "An efficient graph-based algorithm for ESD current path analysis," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 27, No. 8, pp. 1363--1375, August 2008.
82. T.-C. Chen, Z.-W. Jiang, T.-C. Hsu, H.-C. Chen, and Y.-W. Chang, "NTUplace3: An analytical placer for large-scale mixed-size designs with preplaced blocks and density constraints," *IEEE*

Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD), Vol. 27, No. 7, pp. 1228--1240, July 2008. **(Best paper nominee)**

83. Z.-W. Jiang and Y.-W. Chang, "An optimal network-flow-based simultaneous diode and jumper insertion algorithm for antenna fixing," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 27, No. 6, pp. 1055--1065, June 2008.
84. H.-Y. Chen, M.-F. Chiang, Y.-W. Chang, L. Chen, and B. Han, "Full-chip gridless routing considering double-via insertion," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 27, No. 5, pp. 844--857, May 2008.
85. C.-W. Lin, S.-Y. Chen, C.-F. Li, Y.-W. Chang, and C.-L. Yang, "Obstacle-avoiding rectilinear Steiner tree construction based on spanning graphs," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 27, No. 4, pp. 643--653, April 2008.
86. T.-C. Chen, Y.-L. Chuang, and Y.-W. Chang, "Effective wire models for X-architecture placement," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 27, No. 4, pp. 654--658, April 2008.
87. T.-C. Chen, Y.-W. Chang, and S.-C. Lin, "A new multilevel framework for large-scale interconnect-driven floorplanning," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 27, No. 2, pp. 286--294, February 2008.
88. P.-H. Yu, C.-L. Yang, and Y.-W. Chang, "Temporal floorplanning using the three-dimensional transitive closure subgraph," *ACM Trans. Design Automation of Electronic Systems (TODAES),* Vol. 12, No. 4, September 2007.
89. B.-Y. Su and Y.-W. Chang, "An optimal jumper insertion algorithm for antenna avoidance/fixing," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 26, No. 10, pp. 1818--1929, October 2007.
90. P.-H. Yu, C.-L. Yang, and Y.-W. Chang, "Placement of defect-tolerant digital microfluidic biochips using the T-tree formulation," *ACM Journal of Emerging Technologies in Computing Systems (JETC)*, Vol. 3, No. 3, November 2007 (32 pages).
91. K. S.-M. Li, C.-C. Su, Y.-W. Chang, C.-L. Lee, and J. E Chen, "P1500 standard compatible interconnect diagnosis for delay and crosstalk faults," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 27, No. 9, pp. 1625—1636, September 2007.
92. H.-C. Lee, Y.-W. Chang, and H. Yang, "MB*-tree: A multilevel floorplanner for large-scale building-module design," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 27, No. 8, pp. 1430—1444, August 2007.
93. J.-W. Fang, I.-J. Lin, Y.-W. Chang, and J.-H. Wang, "A network-flow based routing algorithm for flip chip design," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 26, No. 8, pp. 1417—1429, August 2007.
94. T.-C. Chen and Y.-W. Chang, "Multilevel full-chip gridless routing with applications to optical-proximity correction," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 27, No. 6, pp. 1041—1053, June 2007.
95. B.-Y. Su, Y.-W. Chang, and J. Hu, "An exact jumper insertion algorithm for antenna violation avoidance/fixing considering routing obstacles," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 27, No. 4, pp. 719—734, April 2007.

96. C.-W. Liu and Y.-W. Chang, "Power/ground network and floorplan co-synthesis for fast design convergence," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 27, No. 4, pp. 693--704, April 2007.
97. C.-H. Hsu, S.-J. Chou, J.-H. R. Jiang, and Y.-W. Chang, "A statistical approach to the timing-yield optimization of pipeline circuits," *Lecture Notes in Computer Science*, Vol. 4644, pp. 148--159, 2007.
98. S.-W. Tu, J.-Y. Jou, and Y.-W. Chang, "RLC coupling-aware simulation and on-chip bus encoding for delay reduction," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD),* Vol. 25, No. 10, pp. 2258--2264, October 2006.
99. T.-Y. Ho, Y.-W. Chang, and S.-J. Chen, "Multilevel Routing with Jumper Insertion for Antenna Avoidance," *Integration: The VLSI Journal*, Vol. 39, Issue 4, pp. 420--432, July 2006 (SCI).
100. T.-C. Chen and Y.-W. Chang, "Modern floorplanning based on B*-trees and fast simulated annealing," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 26, No. 4, pp. 637—650, April 2006.
101. H.-R. Jiang, S.-R., Pan, Y.-W. Chang, and J.-Y. Jou, "Reliable crosstalk-driven interconnect optimization," *ACM Trans. on Design Automation of Electronic Systems (TODAES),* Vol. 11, No. 1, pp. 88—103, January 2006.
102. T.-Y. Ho, Y.-W. Chang, S.-J. Chen, and D. T. Lee, "Crosstalk-and performance-driven multilevel full-chip routing," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 25, No. 6, pp. 869—878, June 2005.
103. J.-M. Lin and Y.-W. Chang, "TCG: A transitive closure graph based representation for general floorplans," *IEEE Trans. VLSI Systems (TVLSI)*, Vol. 13, No. 2, pp. 288--292, February 2005.
104. G.-M. Wu, C.-T. M. Chao, and Y.-W. Chang, "A clustering and probability based partitioning algorithm for time-multiplexed FPGAs," *Integration: The VLSI Journal*, Vol. 38, Issue 2, pp. 245—265, December 2004 (SCI).
105. J.-M. Lin and Y.-W. Chang, "TCG-S: Orthogonal coupling of P*-admissible representations for general floorplans," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 24, No. 6, pp. 968—980, June 2004.
106. Y.-W. Chang and S.-P. Lin, "MR: A new framework for multilevel full-chip routing," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 23, No. 5, pp. 793—800, May 2004.
107. H.-R. Jiang, Y.-W. Chang, J.-Y. Jou, K.-Y. Chao, "Simultaneous floorplan and buffer block optimization," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 23, No. 5, pp. 694—703, May 2004
108. G.-M. Wu, M. Shyu, and Y.-W. Chang, "Universal switch blocks for three-dimensional FPGA design," *IEE Proceedings---Circuits, Devices, and Systems,* Vol. 151, No. 1, pp. 49—57, February 2004.
109. T.-C. Chen, S.-R. Pan, and Y.-W. Chang, "Timing modeling and optimization under the transmission line model," *IEEE Trans. VLSI Systems (TVLSI)*, Vol. 12, No. 1, pp. 28--41, 2004.
110. J.-M. Lin, Y.-W. Chang, and S.-P. Lin, "Corner sequence: A P-admissible floorplan representation with a worst-case linear-time packing scheme," *IEEE Trans. on VLSI Systems*

(TVLSI), Vol. 11, No. 4, pp. 679--686, August 2003.

111. G.-M. Wu, Y.-C. Chang, and Y.-W. Chang, "Rectilinear block placement using B*-trees," *ACM Trans. on Design Automation of Electronic Systems (TODAES),* Vol. 8., No. 2, pp. 188-202, April 2003. **(Best paper nominee)**

112. S.-W. Tu, W.-Z. Shen, Y.-W. Chang, T.-C. Chen, and J.-Y. Jou, "Inductance modeling for on-chip interconnects," *International Journal of Analog Integrated Circuits and Signal Processing*, Vol. 35, No. 1, pp. 65--78, April 2003 **(Invited paper).**

113. Y.-W. Chang, K. Zhu, D. F. Wong, G.-M. Wu, and C. K. Wong, "Analysis of FPGA/FPIC switch modules,"' *ACM Trans. on Design Automation of Electronic Systems (TODAES),* Vol. 8, No. 1, pp. 11--37, January 2003.

114. J.-M. Lin, H.-L. Lin, and Y.-W. Chang, "Arbitrarily shaped rectilinear module placement using TCG," *IEEE Trans. VLSI Systems* (*TVLSI*), Vol. 10, No. 6, pp. 886--901, December 2002.

115. Y.-M. Lee, C.-P. Chen, Y.-W. Chang, and D.-F. Wong, "Simultaneous buffer-sizing and wire-sizing for clock trees based on Lagrangian relaxation," *VLSI Design,* Vol. 15, No. 3, pp. 587--594, November 2002 **(Invited paper).**

116. G.-M. Wu, J.-M. Lin, and Y.-W. Chang, "Performance-driven placement for dynamically reconfigurable FPGAs," *ACM Trans. on Design Automation of Electronic Systems (TODAES),* Vol. 7, No. 4, pp. 628--642, October 2002.

117. J.-M. Lin, H.-E. Yi, and Y.-W. Chang, "Module placement with boundary constraints using B*-trees," *IEE Proceedings--Circuits, Devices and Systems*, Vol. 149, No. 4, pp. 251--256, August 2002. (SCI)

118. H. Fang, Y.-L. Wu, and Y.-W. Chang, "Comments on "Generic universal switch blocks"," *IEEE Trans. on Computers (TC)*, Vol. 51, No.1, pp. 93--95, January 2002.

119. Y.-W. Chang, J.-M. Lin, and D. F. Wong, "A matching-based algorithm for FPGA segmentation design," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 20, No. 6, pp. 784--791, June 2001.

120. G.-M. Wu, J.-M. Lin, and Y.-W. Chang, "Generic ILP-based approaches for time-multiplexed FPGA partitioning," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems (TCAD),* Vol. 20, No. 10, pp. 1266--1274, October 2001.

121. H.-R. Jiang, Y.-W. Chang, and J.-Y. Jou, "Crosstalk-driven interconnect optimization," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems (TCAD),* Vol. 19, No. 9, pp. 999--1010, September 2000.

122. Y.-W. Chang, K. Zhu, and D. F. Wong, "Timing-driven routing for symmetrical-array-based FPGAs," *ACM Trans. on Design Automation of Electronic Systems (TODAES)*, Vol. 5, No. 3, pp. 433--450, July 2000.

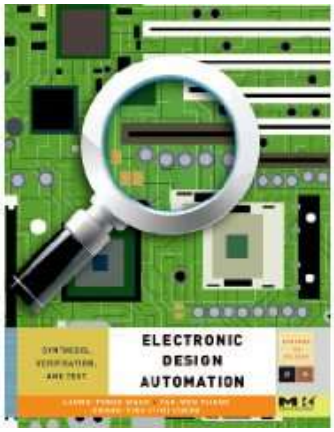
123. M. Shyu, Y.-D. Chang, G.-M. Wu, and Y.-W. Chang, "Generic universal switch blocks," *IEEE Trans. on Computers* (*TC*), Vol. 49, No. 4, pp. 348--359, April 2000.

124. G.-M. Wu and Y.-W. Chang, "Quasi-universal switch matrices for FPD design," *IEEE Trans. on Computers (TC)*, Vol. 48, No. 10, pp. 1107--1122, October 1999.

125. S. Thakur, Y.-W. Chang, D. F. Wong, and S. Muthukrishnan, "Algorithms for an FPGA switch module routing problem with application to global routing," *IEEE Trans. on Computer-Aided Design (TCAD)*, Vol. 16, No. 1, pp. 32--47, January 1997.
126. Y.-W. Chang, D. F. Wong, and C. K. Wong, "Universal switch modules for FPGA design," *ACM Trans. on Design Automation of Electronic Systems (TODAES)*, Vol. 1, No. 1, pp. 80--101, January 1996. **(Top-2 most highly cited research paper of TODAES for over 20 years)**

Books & Book Chapters

1. M. P.-H. Lin and Y.-W. Chang, "Hierarchical Placement with Layout Constraints," in Analog Layout Synthesis (H. E. Graeb, Editor), Springer 2010.
2. L.T. Wang, Y.-W. Chang, and K.-T. Cheng (Editors), *Electronic Design Automation: Synthesis, Verification, and Testing,* Elsevier/Morgan Kaufmann, 2009 (934 pages).
3. T.-C. Chen and Y.-W. Chang, "Floorplanning," in *Electronic Design Automation: Synthesis, Verification, and Testing* (L.T. Wang, Y.-W. Chang, and K.-T. Cheng, Editors), Elsevier/Morgan Kaufmann, 2009.
4. H.-Y. Chen and Y.-W. Chang, "Global and Detailed Routing," in *Electronic Design Automation: Synthesis, Verification, and Testing* (L.T. Wang, Y.-W. Chang, and K.-T. Cheng, Editors), Elsevier/Morgan Kaufmann, 2009.
5. C. E. Stroud, L.-T. Wang, and Y.-W. Chang, "Introduction," in *Electronic Design Automation: Synthesis, Verification, and Testing* (L.T. Wang, Y.-W. Chang, and K.-T. Cheng, Editors), Elsevier/Morgan Kaufmann, 2009.
6. F. Y. Young, C.-K. Koh, and Y.-W. Chang, "Buffer planning," in *Physical Design Handbook* (C. Alpert, S. Sapatnekar, and Dinesh D. Mehta, Editors), CRC Press, 2008 **(Invited article)**.
7. T.-C. Chen and Y.-W. Chang, "Packing floorplan representation," in *Physical Design Handbook* (C. Alpert, S. Sapatnekar, and Dinesh D. Mehta, Editors), CRC Press, 2008 **(Invited article)**.
8. T.-Y. Ho, Y.-W. Chang, and S.-J. Chen, *Full-chip Nanometer Routing Techniques,* Springer, 2007.
9. T.-C. Chen, Z.-W. Jiang, T.-C. Hsu, H.-C. Chen, and Y.-W. Chang, "NTUplace3: An Analytical Placer for Large-Scale Mixed-Size Designs," in *Modern Circuit Placement: Best Practices and Results* (G.-J. Nam and J. Cong, Editors), 2006 **(Invited article)**.
10. Y.-W. Chang, T.-C. Chen, and H.-Y. Chen, "Physical Design for System-On-a-Chip," in *Essential Issues in SOC Design* (Y.-L. Lin, Editor), John Wiley & Sons, 2006 **(Invited article)**.
11. Y.-W. Chang, D. F. Wong, and C. K. Wong, "Programmable logic arrays," in *Encyclopedia of Electrical and Electronics Engineering* (John G. Webster, Editor), Vol. 18, pp. 334-348, John Wiley & Sons, Inc., Publishers, 1999 **(Invited article)**.
12. M. Shyu, M.-H. Hsieh, W.-H. Shiue, Y.-T. Chang, and Y.-W. Chang, *Xilinx FPGA/CPLD Lab Practice, Chun-Hua Book Pub.,* 1998. (in Chinese)



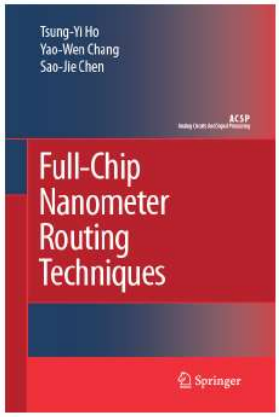


Figure 24: Books on EDA and routing (in English)

D. ACM/IEEE Conference Publications (Published the most DAC + ICCAD papers; published 107 DAC papers (#1 worldwide) and 87 ICCAD papers (#2 worldwide))

1. C.-M. Chang, S.-Y. Lo, Y.-W. Chang, and S. K. Lim, "Encoding symmetries into operator learning: towards accurate multi-physics simulation in advanced packaging," to appear in *Proceedings of IEEE/ACM Asia South Pacific Design Automation Conference (ASP-DAC-2027),* Tokyo, Japan, January 2027.
2. C.-Y. Chiang, W.-H. Tseng, Y.-W. Chang, and H.-M. Chen, "Learning-guided adaptive cell-wise optimization for mixed-size global placement," to appear in *Proceedings of IEEE/ACM Asia South Pacific Design Automation Conference (ASP-DAC-2027)*, Tokyo, Japan, January 2027.
3. C.-H. Tsou, J.-E. Lu, and Y.-W. Chang, "A consensus-optimization framework for progressive clearance-aware PCB legalization with irregular components," to appear in *Proceedings of IEEE/ACM Asia South Pacific Design Automation Conference (ASP-DAC-2027)*, Tokyo, Japan, January 2027.
4. P.-J. Lin, S.-H. Chen, C.-W. Yeh, Y.-W. Chang, "Efficient concurrent die-to-die routing with teardrop and offset-via awareness," to appear in *Proceedings of IEEE/ACM Asia South Pacific Design Automation Conference (ASP-DAC-2027),* Tokyo, Japan, January 2027.
5. Z.-Y. Cai and Y.-W. Chang, "Analytical concurrent decoupling capacitor placement for PCB power distribution networks via physics-informed cutting planes," to appear in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2026)*, San Jose, CA, November 2026.
6. B.-Y. Huang, Y.-E. Wu, and Y.-W. Chang, "Timing-driven bridging cell planning via congestion-aware region selection for double-sided signal routing," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2026)*, San Jose, CA, November 2026.
7. W.-K. Huang, J.-J. Lee, Y.-W. Chang, Y. Lu, J. Bai, and B.-C. Tseng, "Unified rail-signal co-design for multilayer PCBs: resource allocation, IR-drop, and routability," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2026),* Long Beach, CA, July 2026.

8. C.-C. Su, Y.-S. Yang, C.-Y. Li, S.-H. Chen and Y.-W. Chang, "Late Breaking Results: A unified analytical framework for MBFF clustering and placement for timing, power, and area co-optimization," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2026)*, Long Beach, CA, July 2026.
9. W.-H. Tseng, Y.-W. Chang, and J.-H. R. Jiang, "Late Breaking Results: Novel qubit mapping for two-dimensional trapped-ion quantum computing systems," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2026)*, Long Beach, CA, July 2026.
10. W.-C. Hung, J.-J. Lee, S.-H. Wang, and Y.-W. Chang, "Late Breaking Results: Unified PCB routing considering pair-spacing and width-range constraints," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2026)*, Long Beach, CA, July 2026.
11. X. Tong, C.-J. Hsu, G. Chen, Y.-H. Hung, J. Chen, and Y.-W. Chang, "Late Breaking Results: 3D analytical placement with smoothed multi-die wirelength model," in Proceedings of ACM/IEEE Design Automation Conference (DAC-2026), Long Beach, CA, July 2026.
12. M. Liu, Y.-W. Chang, and K.-Y. Chao, "Late Breaking Results: TSV assignment for backside power delivery network designs considering stress and IR-drop effect," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2026),* Long Beach, CA, July 2026.
13. J. Gao, W.-H. Tseng, and Y.-W. Chang, "Subgraph-based qubit mapping for noisy intermediate-scale quantum computing," in *Proceedings of IEEE/ACM Asia South Pacific Design Automation Conference (ASP-DAC-2026),* Hong Kong, January 2026.
14. Z.-Y. Cai, W.-H. Mao, Y.-W. Chang, Y. Lu, J. Bai, and B.-C. Tseng, "Semidefinite programming-based decoupling capacitor placement for power distribution network optimization," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2025)*, Munich, Germany, October 2025 **(First-place Best Paper Award out of 1078 submissions; William J. McCalla ICCAD Best Paper Award; Taiwan's first ICCAD BPA in its 44-year history)**
15. S.-H. Chen, Z.-W. Chen, P.-J. Lin, H.-J. Hsu, H.-Y. Lin, Y.-H. Chuang, H.-Y. Chen, J. Chang and Yao-Wen Chang, "Performance-Driven Pre-Assignment Routing for High-Speed Package Designs," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2025),* Munich, Germany, October 2025
16. Z.-H. Wu, B.-Y. Huang, Y.-C. Chen, and Y.-W. Chang, "Parallel non-integer multiple-cell-height node remapping," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2025)*, Munich, Germany, October 2025
17. S.-Y. Lo, C.-M. Chang, and Y.-W. Chang, "Advanced packaging warpage modeling with DeepONet-based operator learning," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2025),* Munich, Germany, October 2025
18. W.-C. Yu, T.-F. Chen, Y.-H. Chan, J.-H. R. Jiang, D.-W. Chiou, and Y.-W. Chang, "Optimal Qubit Reuse for Quantum Computation with Gate Reordering and Eager Measurement," in *Proceedings of IEEE International Conference on Quantum Computing and Engineering (QCE-2025),* Albuquerque, New Mexico, USA, September, 2025.

19. C.-Y. Li, C.-C. Su, Z.-W. Chen, S.-H. Chen, and Y.-W. Chang, "Late breaking results: multi-objective multi-bit flip-flop placement considering pre-placed cells," *in Proceedings of ACM/IEEE Design Automation Conference (DAC-2025)*, San Francisco, CA, June 2025.
20. C.-Y. Chiang, Z.-Y. Cai, C.-C. Lan, Y.-J. Chen, Y. Hsu, Y.-W. Chang, and H.-M. Chen, "Late breaking results: Scalable GPU-friendly parallelization for sweep-based maze routing," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2025)*, San Francisco, CA, June 2025.
21. M.-H. Chen, C.-Y. Li, C.-C. Su, Y.-W. Chang, and T.-C. Chen, "Late breaking results: Warpage-aware generative floorplanning for reliable advanced packaging," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2025)*, San Francisco, CA, June 2025.
22. C.-H. Tsou, Z.-X. Lee, and Y.-W. Chang, "Late breaking results: Advanced PCB placement with irregular components for efficient collision detection and routability optimization," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2025)*, San Francisco, CA, June 2025.
23. C.-Y. Ou, Y.-J. Chen, and Y.-W. Chang, "Constraint graph-based PCB legalization considering dense, heterogeneous, irregular-shaped, and any-oriented components," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2025)*, San Francisco, CA, June 2025.
24. Y.-J. Chen, W.-K. Huang, C.-T. Tsai, C.-Y. Ou, and Y.-W. Chang, "Clearance-constrained PCB global placement with heterogeneous components," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2025)*, San Francisco, CA, June 2025.
25. W.-Y. Kao, T.-J. Lin, and Y.-W. Chang, "Physically aware wavelength-routed optical NoC design for customized topologies with parallel switching elements and sequence-based models," in *Proceedings of IEEE/ACM Asia South Pacific Design Automation Conference (ASP-DAC-2025),* Tokyo, Japan, January 2025.
26. C.-C. Lan, C.-C. Su, Y.-H. Lu, and Y.-W. Chang, "Robust technology-transferable static IR drop prediction based on image-to-image machine learning," in *Proceedings of IEEE/ACM Asia South Pacific Design Automation Conference (ASP-DAC-2025)*, Tokyo, Japan, January 2025.
27. C.-Y. Chiang, Y.-H. Chiang, C.-C. Lan, Y. Hsu, C.-M. Chang, S.-C. Huang, S.-H. Wang, and Y.-W. Chang, "Mixed-size placement prototyping based on reinforcement learning with semi-concurrent optimization," in *Proceedings of IEEE/ACM Asia South Pacific Design Automation Conference (ASP-DAC-2025)*, Tokyo, Japan, January 2025.
28. S.-Y. Lo, M. Lin, and Y.-W. Chang, "Efficient high-fidelity two-dimensional warpage modeling for advanced packaging analysis," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2024)*, Newark, NJ, October 2024 **(Best-in-Track Paper)**
29. Y.-J Chen, C.-H Hsieh, P.-H Su, S.-H Chen, and Y.-W Chang, "Mixed-size 3D analytical placement with heterogeneous technology nodes," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2024),* San Francisco, CA, June 2024.
30. J.-W Chuang, Z.-H Wu, B.-Y Huang, and Y.-W Chang, "Redistribution layer routing with dynamic via insertion under irregular via structure," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2024)*, San Francisco, CA, June 2024.

31. W.-C. Tseng, Z.-Y. Cai, Y.-P. Huang, Y.-H. Lo, Y.-W. Chang, "Late breaking results: Power rail routing for advanced multi-layered printed circuit boards," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2024)*, San Francisco, CA, June 2024.
32. C.-H. Tsou, S.-Y. Lin, W.-C. Hung, and Y.-W. Chang, "Late breaking results: Modern automatic PCB placement with complex constraints," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2024)*, San Francisco, CA, June 2024.
33. Z. Lin, P. Zou, M. Wei, J. Chen, Y.-W. Chang, "Electrostatics-based analytical global placement for timing optimization," in *Proceedings of ACM/IEEE Design Automation and Test in Europe (DATE-2024)*, Valencia, Spain, March 2024.
34. Y.-W. Chang, "Physical design challenges in heterogeneous integrations," in *Proceedings of ACM International Symposium on Physical Design (ISPD-2024)*, Taipei, Taiwan, March 2024 **(Keynote Speech)**
35. W.-H. Tseng, Y.-W. Chang, and J.-H. Jiang, "Satisfiability modulo theories-based qubit mapping for trapped-ion quantum computing systems," in *Proceedings of ACM International Symposium on Physical Design (ISPD-2024)*, Taipei, Taiwan, March 2024
36. C.-C. Lee and Y.-W. Chang, "Floorplanning for embedded multi-die interconnect bridge packages," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2023)*, San Francisco, CA, October/November 2023
37. Y.-L. Chen, W.-C. Tseng, W.-Y. Kao, and Y.-W. Chang, "A general wavelength-routed optical networks-on-chip model with applications to provably good customized and fault-tolerant topology designs," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2023)*, San Francisco, CA, October/November 2023.
38. M.-H. Chung, J.-W. Chuang, and Y.-W. Chang, "Any-angle routing for redistribution layers in 2.5D IC packages," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2023)*, San Francisco, CA, July 2023.
39. W.-H. Chen and Y.-W. Chang, "Graph-based simultaneous placement and routing for two-dimensional directed self-assembly technology," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2023)*, San Francisco, CA, July 2023.
40. K.-C. Chen, Y.-L. Chen, Y.-S. Lu, and Y.-W. Chang, "Toward parallelism-optimal topology generation for wavelength-routed optical NoC designs," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2023)*, San Francisco, CA, July 2023.
41. Z. Cai, P. Zou, Z. Wu, X. Tong, J, Yu, J. Chen, and Y.-W. Chang, "PUFFER: A routability-driven placement framework via cell padding with multiple features and strategy exploration," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2023)*, San Francisco, CA, July 2023.
42. Q. Liu, D. Lin, C. Chen, H. He, J. Chen, and Y.-W. Chang, "A matching based escape routing algorithm with variable design rules and constraints," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2023)*, San Francisco, CA, July 2023.
43. Q. Liu, Q. Tang, J. Chen, C. Chen, Z. Zhu, H. He, J. Chen, and Y.-W. Chang, "Disjoint-path and golden-pin based irregular PCB routing with complex constraints," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2023)*, San Francisco, CA, July 2023.

44. W.-H. Tseng and Y.-W. Chang, "Late Breaking Results: An efficient bridge-based compression algorithm for topologically quantum error corrected circuits," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2023)*, San Francisco, CA, July 2023.
45. Y.-C. Chen, Y.-H. Chen, Y.-H. Lo, C.-Y. Chiang, and Y.-W. Chang, "Late Breaking Results: Analytical placement for 3D ICs with multiple manufacturing technologies," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2023)*, San Francisco, CA, July 2023
46. J.-W. Hsu, K.-C. Chen, Y.-S. Chen, Y.-H. Lo, Y.-W. Chang, "Security-aware physical design against trojan insertion, frontside probing, and fault injection attacks," in *Proceedings of ACM International Symposium on Physical Design (ISPD-2023)*, Virtual, March 2023.
47. Y. Hsu, M.-H. Chung, Y.-W. Chang, and C.-H. Lin, "Transitive closure graph-based warpage-aware floorplanning for package designs," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2022)*, San Diego, CA, October/November 2022.
48. Y.-T. Chen and Y.-W. Chang, "Obstacle-avoiding multiple redistribution layer routing with irregular structures," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2022)*, San Diego, CA, October/November 2022.
49. C.-Y. Wang, Y.o-W. Chang, and Y.-H. Chang, "SGIRR: sparse graph index remapping for ReRAM crossbar operation unit and power optimization," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2022)*, San Diego, CA, October/November 2022.
50. S.-R. Nie, Y.-T. Chen, and Y.-W. Chang, "Y-architecture-based flip-chip routing with dynamic programming-based bend minimization," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2022)*, San Francisco, CA, July 2022. **(Publicity Paper)**
51. F.-C. Chang, Y.-W. Tseng, Y.-W. Yu, S.-R. Lee, A. Cioba, I-L. Tseng, D.-S. Shiu, J.-W. Hsu, C.-Y. Wang, C.-Y. Yang, R.-C. Wang, Y.-W. Chang, T.-C. Chen, and T.-C. Chen, "Late breaking results: Flexible chip placement via reinforcement learning," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2022)*, San Francisco, CA, July 2022. **(Publicity Paper)**
52. W.-H. Tseng and Y.-W. Chang, "A bridge-based algorithm for simultaneous primal and dual defects compression on topologically quantum-error-corrected circuits," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2022)*, San Francisco, CA, July 2022.
53. Y.-S. Lu, K.-C. Chen, Y.-L. Hsu, and Y.-W. Chang, "Thermal-aware optical-electrical routing codesign for on-chip signal communications," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2022)*, San Francisco, CA, July 2022.
54. H. Wang, X. Tong, C. Ma, R. Shi, J. Chen, K. Wang, J. Yu, and Y.-W. Chang, "CNN-inspired analytical global placement for large-scale heterogeneous FPGAs," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2022)*, San Francisco, CA, July 2022.
55. Z. Zhu, Y. Mei, Z. Li, J. Lin, J. Chen, J. Yang, and Y.-W. Chang, "High-performance placement for large-scale heterogeneous FPGAs with clock constraints," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2022)*, San Francisco, CA, July 2022.

56. M. Su, Y. Xiao, S. Zhang, H. Su, J. Xu, H. He, Z. Zhu, J. Chen, and Y.-W. Chang, "Subgraph matching based reference placement for PCB designs," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2022)*, San Francisco, CA, July 2022. (LBR Paper)
57. I. H.-R. Jiang, Y.-W. Chang, J.-L. Huang, C. C.-P. Chen, "Intelligent design automation for heterogeneous integration," in *Proceedings of ACM International Symposium on Physical Design (ISPD-2022)*, pp. 105-106, Virtual, March 2022.
58. X. Bai, Z. Zhu, P. Zou, J. Chen, J. Yu, and Y.-W. Chang, "Voronoi diagram based heterogeneous circuit layout centerline extraction for mask verification," in *Proceedings of IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC-2022)*, Virtual Conference, January 2022.
59. M. Su, H. Ding, S. Weng, C. Zou, Z. Zhou, Y. Chen, J. Chen, and Y.-W. Chang, "High-correlation 3D routability estimation for congestion-guided global routing," in *Proceedings of IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC-2022)*, Virtual Conference, January 2022.
60. F.-Y. Chuang and Y.-W. Chang, "Optical routing considering waveguide matching constraints," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2021)*, November 2021.
61. Z.-Y. Lin and Y.-W. Chang, "A row-based algorithm for non-integer multiple-cell-height placement," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2021)*, November 2021.
62. W.-K. Liu, M.-H. Chen, C.-M. Chang, C.-C. Chang, and Y.-W. Chang, "Time-division multiplexing based system-level FPGA routing," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2021)*, November 2021.
63. Y.-J. Cai, Y. Hsu, and Y.-W. Chang, "Simultaneous pre- and free-assignment routing for multiple redistribution layers with irregular vias," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2021),* San Francisco, CA, July/December 2021.
64. B. Wang, L. Jiang, W. Zhu, L. Guo, J. Chen, and Y.-W. Chang, "A two-stage neural network classifier for the data imbalance problem with application to hotspot detection," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2021)*, San Francisco, CA, July/December 2021.
65. C.-H. Hsu, W.-H. Lin, W.-H. Tseng, and Y.-W. Chang, "A bridge-based compression algorithm for topological quantum circuits," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2021),* San Francisco, CA, July/December 2021.
66. M.-H. Chen, Y.-W. Chang, and J.-J. Wang, "Performance-driven simultaneous partitioning and routing for multi-FPGA systems," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2021)*, San Francisco, CA, July/December 2021.
67. Y. Chou, C.-W. Hsu, Y.-W. Chang, and T.-C. Chen, "VLSI structure-aware placement for convolutional neural network accelerator units," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2021)*, San Francisco, CA, July/December 2021.

68. H.-R. Jiang, Y.-W. Chang, J.-L. Huang, and C.-P. Chen, "Opportunities for 2.5/3D heterogeneous SoC integration," in *Proceedings of IEEE International Symposium on VLSI Design, Automation and Test (VLSI-DAT-21),* April 2021 **(Special Session)**
69. Z. Lin, Y. Xie, G. Qian, J. Chen, S. Wang, J. Yu, and Y.-W. Chang, "Timing-driven placement for FPGAs with heterogeneous architectures and clock constraints," in *Proceedings of ACM/IEEE Design Automation and Test in Europe (DATE-2021)*, February 2021.
70. Y.-W. Chang, "EDA for More-Moore and more-than-Moore designs: challenges and opportunities," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2020)*, November 2020. **(Keynote Speech)**
71. H.-R. Jiang, Y.-W. Chang, J.-L. Huang, and C.-P. Chen, "Intelligent design automation for 2.5/3D heterogeneous SoC integration," *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2020)*, November 2020. **(Special Session Paper)**
72. R. Wang and Y.-W. Chang, "Routability-aware pin access optimization for monolithic 3D designs," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2020)*, November 2020.
73. J. Chen, Z. Huang, Y. Huang, W. Zhu, J. Yu, and Y.-W. Chang, "An efficient EPIST algorithm for global placement with non-integer multiple-height cells," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2020)*, San Francisco, CA, July 2020. **(Best-in-Track Paper)**
74. P. Zou, Z. Lin, X. Shi, Y. Wu, J. Chen, J. Yu, and Y.-W. Chang, "Time-division multiplexing based system-level FPGA routing for logic verification," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2020)*, San Francisco, CA, July 2020. **(Best-in-Track Paper)**
75. Y.-S. Lu, S.-J. Yu, and Y.-W. Chang, "A provably good wavelength-division-multiplexing-aware clustering algorithm for on-chip optical routing," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2020)*, San Francisco, CA, July 2020.
76. Y.-S. Lu, S.-J. Yu, and Y.-W. Chang, "Topological structure and physical layout codesign for wavelength-routed optical networks-on-chip," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2020)*, San Francisco, CA, July 2020.
77. C.-C. Huang, G. Tellez, G.-J. Nam, and Y.-W. Chang, "Latch clustering for timing-power co-optimization," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2020)*, San Francisco, CA, July 2020.
78. H.-T. Wen, Y.-J. Cai, Y. Hsu, and Y.-W. Chang, "Via-based redistribution layer routing for InFO packages with irregular pad structures," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2020)*, San Francisco, CA, July 2020.
79. J. Chen, Z. Zhu, Q. Liu, Y. Zhang, W. Zhu, and Y.-W. Chang, "Hamiltonian path based mixed-cell-height legalization for neighbor diffusion effect mitigation," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2020)*, San Francisco, CA, July 2020.
80. C.-H. Chiang, F.-Y. Chuang, and Y.-W. Chang, "Unified redistribution layer routing for 2.5D IC packages," in *Proceedings of IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC-2020)*, Bejing, China, January 2020. **(Best Paper Nominee)**

81. T. Lan, X. Li, J. Chen, J. Yu, L. He, S. Dong, W. Zhu, and Y.-W. Chang, "Timing-aware fill insertions with design-rule and density constraints," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2019)*, Westminister, CO, November 2019. **(Best-in-Track Paper)**
82. J. Chen, W. Zhu, J. Yu, L. He, and Y.-W. Chang, "Analytical placement with 3D Poisson's equation and ADMM based optimization for large-scale 2.5D heterogeneous FPGAs," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2019)*, Westminister, CO, November 2019.
83. Z. Wang and Y.-W. Chang, "Graph- and ILP-based cut redistribution for two-dimensional directed self-assembly," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2019)*, Westminister, CO, November 2019.
84. Y.-H. Chang, H.-T. Wen and Y.-W. Chang, "Obstacle-aware group-based length-matching routing for pre-assignment area-I/O flip-chip designs," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2019)*, Westminister, CO, November 2019.
85. F.-K. Sun and Y.-W. Chang, "BiG: A bivariate gradient-based wirelength model for analytical circuit placement," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2019)*, Las Vegas, NV, June 2019.
86. C.-H. Hsu, S.-C. Hung, H. Chen, F.-K. Sun, and Y.-W. Chang, "A DAG-based algorithm for obstacle-aware topology-matching on-track bus routing," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2019)*, Las Vegas, NV, June 2019.
87. X. Li, J. Chen, W. Zhu and Y.-W. Chang, "Analytical mixed-cell-height legalization considering average and maximum movement minimization," in *Proceedings of ACM International Symposium on Physical Design (ISPD-2019),* San Francisco, CA, April 2019.
88. Y.-C. Liu, T.-C. Chen, and Y.-W. Chang, "MDP-trees: multi-domain macro placement for ultra large-scale mixed-size designs," in *Proceedings of IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC-2019),* Tokyo, Japan, January 2019.
89. W. Zhu, Z. Huang, J. Chen, and Y.-W. Chang, "Analytical solution of Poisson's equation and its application to VLSI global placement," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2018)*, San Diego, CA, November 2018. **(Best Paper Nominee)**
90. J. Chen, L. Yang, Z. Peng, W. Zhu, and Y.-W. Chang, "Novel proximal group ADMM for placement considering fogging and proximity effects," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2018)*, San Diego, CA, November 2018. **(Best-in-Track Paper)**
91. S.-C. Chen, R. Sun, and Y.-W. Chang, "Simultaneous partitioning and signals grouping for time-division multiplexing in 2.5D FPGA-based systems," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2018),* San Diego, CA, November 2018.
92. F.-K. Sun, H. Chen, C.-Y. Chen, C.-H. Hsu, and Y.-W. Chang, "A multithreaded initial detailed routing algorithm considering global routing guides," in *Proceedings of IEEE/ACM*

International Conference on Computer-Aided Design (ICCAD-2018), San Diego, CA, November 2018.

93. Z. Zhu, X. Li, Y. Chen, J. Chen, W. Zhu, and Y.-W. Chang, "Mixed-cell-height legalization considering technology and region constraints," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2018)*, San Diego, CA, November 2018.
94. Y.-W. Tseng and Y.-W. Chang, "Mixed-cell-height placement considering drain-to-drain abutment," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2018)*, San Diego, CA, November 2018.
95. J. Chen, P. Yang, X. Li, W. Zhu, and Y.-W. Chang, "Mixed-cell-height placement with complex minimum-implant-area constraints," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2018),* San Diego, CA, November 2018.
96. Y.-S. Lu, Y.-H. Chang, and Y.-W. Chang, "WB-trees: a meshed tree representation for FinFET-based analog layout designs," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2018)*, San Francisco, CA, June 2018. **(Best-in-Track Paper)**
97. Z. Zhu, J. Chen, Z. Peng, W. Zhu, and Y.-W. Chang, "Generalized augmented Lagrangian and its applications to VLSI global placement," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2018),* San Francisco, CA, June 2018.
98. H.-J. Yu and Y.-W. Chang, "DSA-friendly detailed routing considering double patterning and DSA template assignments," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2018)*, San Francisco, CA, June 2018.
99. R. Wang, C.-C. Pai, J.-J. Wang, H.-T. Wen, Y.-C. Pai, Y.-W. Chang, C.-M. Li, and J.-H. Jiang, "Efficient multi-layer obstacle-avoiding region-to-region rectilinear Steiner tree construction," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2018),* San Francisco, CA, June 2018.
100. Y.-Y. Wu and Y.-W. Chang, "Mixed-cell-height detailed placement considering complex minimum-implant-area constraints," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2017)*, Irvine, CA, November 2017. **(Best-in-Track Paper)**
101. Y.-C. Kuo, C.-C. Huang, S.-C. Chen, C.-H. Chiang, Y.-W. Chang, and S.-Y. Kuo, "Clock-aware placement for large-scale heterogeneous FPGAs," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2017)*, Irvine, CA, November 2017. **(Best-in-Track Paper)**
102. S.-W. Yang, Y.-W. Chang and T.-C. Chen, "Blockage-aware terminal propagation for placement wirelength minimization," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2017)*, Irvine, CA, November 2017.
103. T.-C. Lin, C.-C. Chi, and Y.-W. Chang. "Redistribution layer routing for wafer-level integrated fan-out package-on-packages," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2017)*, Irvine, CA, November 2017.
104. S.-C. Chen and Y.-W. Chang, "FPGA placement & routing: a survey," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2017*), Irvine, CA, November 2017. (Invited Paper)

105. C.-H. Chang, Y.-W. Chang and T.-C. Chen, "A novel damped-wave framework for macro placement," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2017)*, Irvine, CA, November 2017
106. S.-T. Chen, Y.-W. Chang and T.-C. Chen, "An integrated-spreading-based macro-refining algorithm for large-scale mixed-size circuit designs," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2017)*, Irvine, CA, November 2017.
107. J. Chen, Z. Zhu, W. Zhu, and Y.-W. Chang, "Toward optimal legalization for mixed-cell-height circuit designs," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2017),* Austin, TX, June 2017 **(First-place Best Paper Award out of about 700 submissions; Taiwan's first DAC BPA in its 62-year history)**
108. Y.-C. Huang and Y.-W. Chang, "Fogging effect aware placement in electron beam lithography," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2017),* Austin, TX, June 2017
109. C.-C. Huang, B.-Q. Lin, H.-Y. Lee, Y.-W. Chang, K.-Sheng Wu, and J.-Z. Yang, "Graph-based logic bit slicing for datapath-aware placement," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2017)*, Austin, TX, June 2017
110. Z.-W. Lin and Y.-W. Chang, "Detailed placement for two-dimensional directed self-assembly technology," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2017),* Austin, TX, June 2017
111. Y.-W. Chang, "Generalized force directed relaxation with optimal regions and its applications to circuit placement," in *Proceedings of ACM International Symposium on Physical Design (ISPD-2017)*, Portland, OR, March 2017 **(Invited Paper)**
112. C.-H. Wang, Y.-Y. Wu, J. Chen, Y.-W. Chang, S.-Y. Kuo, W. Wu, and G. Fan, "An effective legalization algorithm for mixed-cell-height standard cells," in *Proceedings of IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC-2017)*, Tokyo, January 2017.
113. Y.-H. Su and Y.-W. Chang, "DSA-compliant routing for two-dimensional patterns using block copolymer lithography," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2016)*, Austin, TX, November 2016.
114. Y.-H. Su and Y.-W. Chang, "VCR: simultaneous via-template and cut-template-aware routing for directed self-Assembly technology," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2016)*, Austin, TX, November 2016.
115. B.-Q. Lin, T.-C. Lin, and Y.-W. Chang, "Redistribution layer routing for integrated fan-out wafer-level chip-scale package," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2016)*, Austin, TX, November 2016.
116. C.-C. Huang, Y.-C. Liu, Y.-S. Lu, Y.-C. Kuo, Y.-W. Chang, and S.-Y. Kuo, "Timing-driven cell placement optimization for early slack histogram compression," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2016)*, Austin, TX, June 2016
117. I.-P. Wu, H.-C. Ou, and Y.-W. Chang, "QB-trees: towards an optimal topological representation with applications to analog layout designs," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2016)*, Austin, TX, June 2016. **(Best-in-Track Paper)**

118. K.-H. Tseng, Y.-W. Chang, and C. C.-C. Liu, "Minimum-implant-area-aware detailed placement with spacing constraints," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2016)*, Austin, TX, June 2016.
119. Z.-W. Lin and Y.-W. Chang, "Double-patterning aware DSA template guided cut redistribution for advanced 1-D gridded designs," in *Proceedings of ACM International Symposium on Physical Design (ISPD-2016)*, Santa Rosa, CA, April 2016.
120. Z.-W. Lin and Y.-W. Chang, "Cut redistribution with directed self-assembly templates for advanced 1-D gridded layouts," in *Proceedings of IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC-2016),* Macau, January 2016.
121. C.-H. Chiou, C.-H. Chang, S.-T. Chen, and Y.-W. Chang, "Circular-contour-based obstacle-aware macro placement," in *Proceedings of IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC-2016)*, Macau, January 2016.
122. M. P.-H. Lin, Y.-W. Chang, and C.-M. Hung, "Recent research development and new challenges in analog layout synthesis," in *Proceedings of IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC-2016)*, Macau, January 2016.
123. C.-C. Huang, H.-Y. Lee, B.-Q. Lin, S.-W. Yang, C.-H. Chang, S.-T. Chen, and Y.-W. Chang, "Detailed-routability-driven analytical placement for mixed-size designs with technology and region constraints," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2015)*, Austin, TX, November 2015.
124. Z.-W. Lin, S.-Y. Fang, Y.-W. Chang, W.-C. Rao, and C.-H. Kuan, "Provably good max-min-m-neighbor-TSP-based subfield scheduling for electron-beam photomask fabrication," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2015)*, Austin, TX, November 2015.
125. Y.-W. Chang, S.-Y. Fang, and R.-G. Liu, "EUV and e-beam manufacturability for next-generation lithography: challenges and solutions," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2015)*, San Francisco, CA, June 2015.
126. H.-C. Ou and Y.-W. Chang, "Layout-dependent-effects-aware analytical analog placement," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2015)*, San Francisco, CA, June 2015.
127. H.-C. Ou, I.-P. Wu, and Y.-W. Chang, "Cutting structure-aware analog placement based on self-aligned double patterning with e-beam lithography," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2015)*, San Francisco, CA, June 2015.
128. Y.-H. Su and Y.-W. Chang, "Nanowire-aware routing considering high cut-mask complexity," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2015)*, San Francisco, CA, June 2015.
129. S.-Y. Chen and Y.-W. Chang, "Routing-architecture-aware analytical placement for heterogeneous FPGAs," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2015)*, San Francisco, CA, June 2015.
130. C.-C. Huang, C.-H. Chiou, K.-H. Tseng, and Y.-W. Chang, "Detailed-routing-driven analytical standard-cell placement," in *Proceedings of IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC-2015),* Tokyo, Japan, January 2015.

131. P.-Y. Hsu and Y.-W. Chang, “Non-stitch triple patterning-aware routing based on conflict graph pre-coloring,” in *Proceedings of IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC-2015),* Tokyo, Japan, January 2015.
132. S.-Y. Fang, Y.-S. Tai, and Y.-W. Chang, “Layout decomposition for spacer-is-metal (SIM) self-aligned double patterning,” in *Proceedings of IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC-2015),* Tokyo, Japan, January 2015.
133. Y.-C. Chen, S.-Y. Chen, and Y.-W. Chang, “Efficient and effective packing and analytical placement for large-scale heterogeneous FPGAs,” in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2014)*, San Jose, November 2014.
134. Y.-H. Su, Y.-C. Huang, L.-C. Tsai, Y.-W. Chang, and S. Banerjee, “Fast lithographic mask optimization considering process variation,” in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2014),* San Jose, November 2014.
135. C.-Y. Liu and Y.-W. Chang, “Simultaneous EUV flare- and CMP-aware placement,” in *Proceedings of IEEE International Conference on Computer Design (ICCD-2014),* Seoul, Korea, October 2014.
136. C.-W. Lin, T.-H. Lin, X.-W. Lin, and Y.-W. Chang, “Buffered clock tree synthesis considering self-heating effects,” in *Proceedings of ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED-2014)*, La Jolla, CA, August 2014.
137. I.-J. Liu, S.-Y. Fang, and Y.-W. Chang, “Overlay-aware detailed routing for self-aligned double patterning lithography using the cut process,” in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2014)*, San Francisco, CA, June 2014.
138. K.-H. Ho and Y.-W. Chang, “A new asynchronous pipeline template for power and performance optimization,” in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2014)*, San Francisco, CA, June 2014.
139. H.-Y. Chang, I. H.-R. Jiang, and Y.-W. Chang, “Functional ECO using metal-configurable gate-array spare cells,” in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2014)*, San Francisco, CA, June 2014.
140. Y.-F. Chen, C.-C. Huang, C.-H. Chiou, and Y.-W. Chang, “Routability-driven blockage-aware macro placement,” in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2014)*, San Francisco, CA, June 2014.
141. C.-Y. Liu, H.-J. Jiang, Y.-W. Chang, and J.-H. Jiang, “Simultaneous EUV flare variation minimization and CMP control with coupling-aware dummification,” in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2014)*, San Francisco, CA, June 2014.
142. S.-Y. Fang, I.-J. Liu, and Y.-W. Chang, “Stitch-aware routing framework for multiple e-beam lithography,” in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2013)*, Austin, TX, June 2013.
143. H.-C. Chang-Chien, H.-C. Ou, T.-C. Chen, and Y.-W. Chang, "Double patterning lithography-aware analog placement," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2013)*, Austin, TX, June 2013.

144. H.-C. Ou, K.-H. Ho, Y.-W. Chang, and H.-F. Tsao, "Coupling-aware length-ratio-matching routing for capacitor arrays in analog integrated circuits," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2013)*, Austin, TX, June 2013.
145. T.-H. Lin, P. Banerjee, and Y.-W. Chang, "An efficient and effective analytical placer for FPGAs," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2013)*, Austin, TX, June 2013.
146. Y.-K. Ho and Y.-W. Chang, "Multiple chip planning for chip-interposer codesign," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2013)*, Austin, TX, June 2013.
147. H.-C. Oh, S.-C. Chang-Chien, and Y.-W. Chang, "Simultaneous analog placement and pouting with current flow and current density considerations," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2013)*, Austin, TX, June 2013.
148. M.-K. Hsu, Y.-F. Chen, C.-C. Huang, T.-C. Chen, and Y.-W. Chang, "Routability-driven placement for hierarchical mixed-size circuit designs," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2013)*, Austin, TX, June 2013.
149. S.-Y. Fang, C.-W. Lin, G.-W. Liao, and Y.-W. Chang, "Simultaneous OPC- and CMP-aware routing based on accurate closed-form modeling," in *Proceedings of ACM International Symposium on Physical Design (ISPD-2013)*, Stateline, NV, March 2013. **(Best paper nominee; 4 nominees)**
150. Y.-K. Ho, X.-W. Shih, Y.-W. Chang, and C.-K. Cheng, "Layer minimization in escape routing for staggered-pin-array PCBs," in *Proceedings of IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC-2013)*, Yokohama, Japan, January 2013.
151. X.-W. Shih, T.-H. Hsu, H.-C. Lee, Y.-W. Chang, and K.-Y. Chao, "Symmetrical buffered clock-tree synthesis with supply-voltage alignment," in *Proceedings of IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC-2013)*, Yokohama, Japan, January 2013.
152. S.-Y. Fang and Y.-W. Chang, "Simultaneous flare level and flare variation minimization with dummification in EUVL," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2012)*, San Francisco, CA, June 2012.
153. H.-C. Lee and Y.-W. Chang, "A chip-package-board co-design methodology," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2012)*, San Francisco, CA, June 2012.
154. S. Chou, M.-K. Hsu, and Y.-W. Chang, "Structure-aware placement for datapath intensive circuit designs," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2012)*, San Francisco, CA, June 2012.
155. S.-Y. Fang, Y.-W. Chang, and W.-Y. Chen, "A novel layout decomposition algorithm for triple patterning lithography," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2012)*, San Francisco, CA, June 2012.
156. H.-C. Oh, S.-C. Chang-Chien, and Y.-W. Chang, "Non-uniform multilevel analog routing with matching constraints," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2012)*, San Francisco, CA, June 2012.
157. H.-Y. Chang, H.-R. Jiang, and Y.-W. Chang, "Timing ECO optimization using metal-configurable gate-array spare cells," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2012)*, San Francisco, CA, June 2012.

158. P.-W. Lee, H.-C. Lee, Y.-K. Ho, Y.-W. Chang, I.-J. Lin, and C. Shen, "Obstacle-avoiding free-assignment routing for flip-chip designs," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2012)*, San Francisco, CA, June 2012.
159. S.-Y. Fang, W.-Y. Chen, and Y.-W. Chang, "Graph-based subfield scheduling for electron-beam photomask fabrication," in *Proceedings of ACM International Symposium on Physical Design (ISPD-2012)*, Napa Valley, CA, March 2012. **(Best paper nominee; 5 nominees)**
160. D.-C. Juan, Y.-L. Chuang, D. Marculescu, and Y.-W. Chang, "Statistical thermal modeling and optimization considering leakage power variations," in *Proceedings of IEEE/ACM European Design Automation and Test Conference (DATE-2012)*, Dresden, Germany**,** March 2012.
161. H.-Y. Chang, I. H.-R. Jiang, and Y.-W. Chang, "Timing ECO optimization via Bezier curve smoothing and fixability identification," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2011)*, San Jose, November 2011.
162. Y.-K. Ho, H.-C. Lee, and Y.-W. Chang, "Escape routing for staggered-pin-array PCBs," *in Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2011)*, San Jose, November 2011.
163. H.-F. Tsao, P.-Y. Chou, S.-L. Huang, Y.-W. Chang, M. P.-H. Lin, D.-P. Chen, and D. Liu, "A corner stitching compliant B*-tree representation and its applications to analog placement," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2011)*, San Jose, November 2011.
164. Y.-L. Chuang, H.-T. Lin, T.-Y. Ho, Y.-W. Chang, and D. Marculescu, "PRICE: Power reduction by placement and clock-network co-synthesis for pulsed-latch designs," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2011)*, San Jose, November 2011.
165. M.-K. Hsu, S. Chou, T.-H. Lin, and Y.-W. Chang, "Routability-driven analytical placement for mixed-size circuit designs," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2011)*, San Jose, November 2011.
166. P.-Y. Chou, H.-C. Ou, Y.-W. Chang, "Heterogeneous B*-trees for analog placement with symmetry and regularity considerations," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2011)*, San Jose, November 2011.
167. M.-K. Hsu, Y.-W. Chang, and V. Balabanov "TSV-aware analytical placement for 3D IC designs," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2011)*, San Diego, CA, June 2011. **(Best Paper Award Runner-Up; Best paper nominee**; 9 out of 675 submissions)
168. H.-Y. Chang, H.-R. I. Jiang, and Y.-W. Chang, "Simultaneous functional and timing ECO," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2011)*, San Diego, CA, June 2011.
169. H.-C. Lee, P.-W. Lee, and Y.-W. Chang, "Recent development in flip-chip routing," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2010)*, San Jose, November 2010. (**Invited embedded tutorial paper**)

170. S.-Y. Chen and Y.-W. Chang, "Native-conflict-aware wire perturbation for double patterning technology," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2010)*, San Jose, November 2010 **(Best paper nominee**; 9 out of 435 submissions)
171. M.-K. Hsu and Y.-W. Chang, "Unified analytical global placement for large-scale mixed-size circuit designs," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2010)*, San Jose, November 2010.
172. S.-Y. Fang, T.-F. Chien, and Y.-W. Chang, "Redundant-wires-aware ECO timing and mask-cost optimization," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2010)*, San Jose, November 2010.
173. C.-H. Hsu, Y.-W. Chan, and R. S. Nassif, "Template-mask design methodology for double patterning technology," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2010)*, San Jose, November 2010.
174. X.-W. Shih, H.-C. Lee, K.-H. Ho, and Y.-W. Chang, "High variation-tolerant obstacle-avoiding clock mesh synthesis with symmetrical driving trees," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2010)*, San Jose, November 2010.
175. Y.-L. Chuang, G.-J. Nam, C. J. Alpert, Y.-W. Chang, J. Roy, and N. Viswanathan, "Design-hierarchy aware mixed-size placement for routability optimization," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2010)*, San Jose, November 2010.
176. S.-L. Huang, C.-W. Lin, and Y.-W. Chang, "Provably good OPC modeling and its applications to interconnect optimization," in *Proceedings of IEEE International Conference on Computer Design (ICCD-2010)*, Amsterdam, Netherland, October 2010. **(Best Paper Award)**
177. X.-W. Shih and Y.-W. Chang, "Fast timing-model independent clock-tree synthesis," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2010)*, Anaheim, CA, June 2010.
178. C.-Y. Lin and Y.-W. Chang, "Cross contamination aware design methodology for pin-constrained digital microfludic biochips," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2010)*, Anaheim, CA, June 2010.
179. Y.-L. Chuang, S. Kim, Y. Shin, and Y.-W. Chang, "Pulsed-latch-aware placement for timing-integrity optimization," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2010)*, Anaheim, CA, June 2010.
180. H.-Y. Chen, S.-J. Chou, and Y.-W. Chang, "Density gradient minimization with coupling-constrained dummy fill for CMP control," in *Proceedings of ACM International Symposium on Physical Design (ISPD-2010)*, San Diego, CA, March 2010.
181. K.-H. Ho, J.-H. Jiang, Y.-W. Chang, "TRECO: Dynamic technology remapping for timing engineering change orders," in *Proceedings of IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC-2010),* Taipei, Taiwan, January 2010.
182. X.-W. Shih, C.-C. Cheng, Y.-K. Ho, and Y.-W. Chang, "Blockage-avoiding buffered clock-tree synthesis," in *Proceedings of IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC-2010),* Taipei, Taiwan, January 2010.

183. P. Falkenstern, Y. Xie, and Y.-W. Chang, "Three-dimensional integrated circuit (3D IC) floorplan and power/ground network co-synthesis," in *Proceedings of IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC-2010),* Taipei, Taiwan, January 2010.
184. Y.-L. Chuang, P.-W. Lee, and Y.-W. Chang, "Voltage-drop aware analytical placement by global power spreading for mixed-size circuit designs," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2009)*, San Jose, November 2009. **(Best paper nominee; 13 out of 435 submissions)**
185. P.-W. Lee, C.-W. Lin, Y.-W. Chang, C.-F. Shen, and W.-C. Tseng "An efficient pre-assignment routing algorithm for flip-chip designs," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2009)*, San Jose, November 2009.
186. C.-H. Hsu, Y.-W. Chang, S. R. Nassif, "Simultaneous layout migration and decomposition for double patterning technology," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2009)*, San Jose, November 2009.
187. T.-F. Chien, W.-C. Chao, Chien-Mo Li, K.-Y. Liao, Y.-W. Chang, M.-T. Chang, M.-H. Tsai, and C.-M. Tseng, "BIST design optimization for large-scale embedded memory cores," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2009)*, San Jose, Nov. 2009.
188. C.-Y. Lin and Y.-W. Chang, "ILP-based pin-count aware design methodology for microfluidic biochips," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2009)*, San Francisco, CA, July 2009.
189. P.-H. Lin, H. Zhang, D. F. Wong, and Y.-W. Chang, "Thermal-driven analog placement considering device matching," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2009)*, San Francisco, CA, July 2009.
190. Z.-W. Jiang, M-K. Hsu, Y.-W. Chang, and K.-Y. Chao, "Spare-cell-aware multilevel analytical placement," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2009)*, San Francisco, CA, July 2009.
191. J.-W. Fang, D. F. Wong, and Y.-W. Chang, "Flip-chip routing with unified area-I/O pad assignments for package-board co-design," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2009)*, San Francisco, CA, July 2009.
192. W.-P. Lee, D. Marculescu, and Y.-W. Chang, "Post-floorplanning power/ground ring synthesis for multiple-supply-voltage designs," in *Proceedings of ACM International Symposium on Physical Design (ISPD-2009)*, San Diego, CA, April 2009.
193. F. Balasa, R. Castro-Lopez, Y.-W. Chang, F. Fernandez, H. Graeb, P.-H. Lin, M. Strasser, "Analog layout synthesis --- recent approaches," in *Proceedings of ACM/IEEE Design Automation and Test in Europe (DATE-2009)*, Niece, France, March 2009.
194. C.-H. Hsu, H.-Y. Chen, and Y.-W. Chang, "High-performance global routing with fast overflow reduction," in *Proceedings of ACM/IEEE Asia South Pacific Design Automation Conference (ASP-DAC-2009)*, Yokohama, Japan, January 2009.
195. J.-W. Fang and Y.-W. Chang, "Area-I/O flip-chip routing for chip-package co-design," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2008)*, San Jose, Nov. 2008.

196. J.-W. Fang, K.-H. Ho, and Y.-W. Chang, "Placement and routing for chip-package-board co-design considering differential pairs," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2008)*, San Jose, Nov. 2008.
197. C.-H. Hsu, H.-Y. Chen, and Y.-W. Chang, "Multi-layer global routing considering via and wire capacities," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2008)*, San Jose, Nov. 2008.
198. H.-C. Chen, Y.-L. Chuang, Y.-W. Chang, and Y.-C. Chang, "Constraint graph-based macro placement for mixed-size circuit designs," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2008)*, San Jose, Nov. 2008.
199. T.-C. Chen, G.-W. Liao, and Y.-W. Chang, "Predictive formulae for OPC with applications to lithography-friendly routing," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2008)*, Anaheim, CA, June 2008. **(Best paper nominee; 14 out of 639 submissions)**
200. Z.-W. Jiang, B.-Y. Su, and Y.-W. Chang, "Routability-driven analytical placement by net overlapping removal for large-scale mixed-size designs," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2008)*, Anaheim, CA, June 2008.
201. P.-H. Yuh, S. Sapatnekar, C.-L. Yang, and Y.-W. Chang, "A progressive-ILP based routing algorithm for cross-referencing biochips," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2008)*, Anaheim, CA, June 2008.
202. W.-P. Lee, H.-Y. Liu, K.-H. Ho, and Y.-W. Chang, "Sensitivity-based multiple-Vt cell swapping for leakage power reduction under timing requirements," in *Proceedings of the 4th IEEE-TSA VLSI Design Automation and Test Conference (VLSI-DAT-2008)*, Hsinchu, Taiwan, April 2008.
203. T.-C. Chen, M. Cho, D. Z. Pan and Y.-W. Chang, "Metal-density driven placement for CMP variation and routability," in *Proceedings of ACM International Symposium on Physical Design (ISPD-2008)*, Portland, Oregon, April 2008.
204. P.-H. Yu, C.-L. Yang, and Y.-W. Chang, "BioRoute: A network flow based routing algorithm for digital microfluidic biochips," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2007)*, pp. 752—757, San Jose, Nov. 2007. **(Prof. Margarida Jacome Memorial Travel Grant Award; 2 papers)**
205. H.-Y. Chen, S.-J. Chou, S.-L. Wang, and Y.-W. Chang, "Novel wire density driven full-chip routing for CMP variation control," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2007)*, pp. 831—838, San Jose, Nov. 2007. **(Best paper nominee; 9 out of 508 submissions)**
206. W.-P. Lee, H.-Y. Liu, and Y.-W. Chang, "An ILP algorithm for post-floorplanning voltage-island generation," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2007)*, pp. 650—655, San Jose, Nov. 2007.
207. Y.-P. Chen, J.-W. Fang, and Y.-W. Chang, "ECO timing optimization using spare cells and technology remapping," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2007)*, pp. 530—535, San Jose, Nov. 2007.
208. I.-J. Lin and Y.-W. Chang, "An efficient algorithm for statistical circuit optimization using Lagrangian relaxation," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2007)*, pp. 119—204, San Jose, Nov. 2007.

209. C.-W. Lin. S.-L. Huang, K.-C. Hsu, M.-X. Lee, and Y.-W. Chang, "Efficient multi-layer obstacle-avoiding rectilinear Steiner tree construction," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2007)*, pp. 380--385, San Jose, Nov. 2007.
210. C.-F. Li, P.-H. Yuh, C.-L. Yang, and Y.-W. Chang, "Post-placement leakage optimization for partially dynamically reconfigurable FPGAs," in *Proceedings of IEEE/ACM International Symposium on Low Power Electronic Design (ISLPED-07)*, August 2007.
211. J.-W. Fang, C.-H. Hsu, and Y.-W. Chang, "An integer linear programming algorithm for flip-chip routing," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2007)*, San Diego, CA, June 2007. **(Best paper nominee; 15 out of 695 submissions)**
212. T.-C. Chen, P.-H. Yuh, Y.-W. Chang, F.-J. Liu, and D. Liu, "MP-trees: a packing-based macro placement algorithm for mixed-size designs," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2007)*, San Diego, CA, June 2007. **(Received the 2nd highest score out of 52 papers in the physical design and manufacturability track)**
213. H.-Y. Liu, W.-P. Lee, and Y.-W. Chang, "A provably good approximation algorithm for power optimization using multiple supply voltages," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2007)*, San Diego, CA, June 2007.
214. Z.-W. Jiang, H.-C. Chen, T.-C. Chen, and Y.-W. Chang, "Challenges and solutions in modern VLSI placement," in *Proceedings of the 3rd IEEE-TSA VLSI Design Automation and Test Conference (VLSI-DAT-2007)*, pp. 111--115, Hsinchu, Taiwan, April 2007. (invited paper)
215. T.-C. Chen, Y.-L. Chuang, and Y.-W. Chang, "X-architecture placement based on effective wire models," in *Proceedings of ACM International Symposium on Physical Design (ISPD-2007)*, pp. 87--94, Austin, TX, March 2007. **(Best paper nominee; highest score; 5 nominees)**
216. C.-W. Lin, C.-F. Li, S.-Y. Chen, Y.-W. Chang, and C.-L. Yang, "Efficient obstacle-avoiding rectilinear Steiner tree construction," in *Proceedings of ACM International Symposium on Physical Design (ISPD-2007)*, pp. 127--134, Austin, TX, March 2007. **(Best paper nominee; highest score; 5 nominees)**
217. I.-J. Lin, T.-Y. Lin, and Y.-W. Chang, "Statistical circuit optimization considering device and interconnect process variations," in *Proceedings of ACM International Workshop on System Level Interconnect Prediction (SLIP-2007)*, Austin, TX, March 2007.
218. C.-W. Lin, M.-C. Tsai, K.-Y. Lee, T.-C. Chen, T.-C. Wang, and Y.-W. Chang, "Recent research and emerging challenges in physical design for manufacturability/reliability," in *Proceedings of ACM/IEEE Asia South Pacific Design Automation Conference (ASP-DAC-2007)*, pp. 238--243, Yokohama, Japan, January 2007 (invited paper).
219. T.-C. Chen, Z.-W. Jiang, T.-C. Hsu, H.-C. Chen, and Y.-W. Chang, "A high quality analytical placer considering preplaced blocks and density constraint," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2006)*, pp. 187--192, San Jose, Nov. 2006. **(Highest review score in Topic 1.1 Partitioning/Floorplanning/Placement)**
220. Z.-W. Jiang and Y.-W. Chang, "An optimal simultaneous diode/jumper insertion algorithm for antenna fixing," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2006)*, pp. 669--674, San Jose, Nov. 2006.

221. W.-P. Lee, H.-Y. Liu, and Y.-W. Chang, “Voltage island aware floorplanning for power and timing optimization,” in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2006)*, pp. 389--394, San Jose, Nov. 2006.
222. H.-Y. Liu, C.-W. Lin, S.-J. Chou, W.-T. Tu, Y.-W. Chang, and S.-Y. Kuo, “Current path analysis for electrostatic discharge protection,” in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2006)*, pp. 510--515, San Jose, Nov. 2006.
223. H.-Y. Chen, M.-F. Chiang, Y.-W. Chang, L. Chen, and B. Han, “Novel full-chip gridless routing considering double-via insertion,” in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2006)*, pp. 755--760, San Francisco, CA, July 2006.
224. P-H. Yuh, C.-L. Yang, and Y.-W. Chang, “Placement of digital microfluidic biochips using the T-tree formulation,” in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2006)*, pp. 931--934, San Francisco, CA, July 2006.
225. C.-Y. Lai, S.-K. Jeng, Y.-W. Chang, and C.-C. Tsai, “Inductance extraction for general interconnect structures,” in *Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS-2006)*, Kos, Greece, May 2006.
226. C.-W. Liu and Y.-W. Chang, “Floorplan and power/ground network co-synthesis for fast design convergence,” in *Proceedings of ACM International Symposium on Physical Design (ISPD-2006)*, San Jose, CA, pp. 86—93, April 2006.
227. B.-Y. Su, Y.-W. Chang, and J. Hu, “An optimal jumper insertion algorithm for antenna effect avoidance/fixing on general routing trees with obstacles,” in *Proceedings of ACM International Symposium on Physical Design (ISPD-2006)*, San Jose, CA, pp. 56—63, April 2006.
228. T.-C. Chen, Z.-W. Jiang, T.-C. Hsu, H.-C. Chen, and Y.-W. Chang, “NTUplace2: a hybrid placer using partitioning and analytical techniques,” in *Proceedings of ACM/IEEE International Symposium on Physical Design (ISPD-2006)*, pp. 215--217, San Jose, CA, April 2006.
229. Y.-W. Lin and Y.-W. Chang, “Thermal-driven interconnect optimization by gate and wire sizing,” in *Proceedings of the 2nd IEEE-TSA VLSI Design Automation and Test Conference (VLSI-DAT-2006)*, pp. 151--154, Hsinchu, Taiwan, April 2006.
230. C.-Y. Peng, W.-C. Chao, Y.-W. Chang, and J.-H. Wang, “Simultaneous block and I/O buffer floorplanning for flip-chip design,” in *Proceedings of ACM/IEEE Asia South Pacific Design Automation Conference (ASP-DAC-2006)*, pp. 213--218, Yokohama, Japan, January 2006.
231. K. S.-M. Li, Y.-W. Chang, C.-C. Su, C.-L. Lee, and J. E. Chen, “P1500 based interconnect diagnosis for delay and crosstalk faults,” in *Proceedings of ACM/IEEE Asia South Pacific Design Automation Conference (ASP-DAC-2006)*, pp. 366--371, Yokohama, Japan, January 2006.
232. T.-C. Chen, Y.-W. Chang, and S.-C. Lin, “A novel framework for multilevel full-chip gridless routing,” in *Proceedings of ACM/IEEE Asia South Pacific Design Automation Conference (ASP-DAC-2006)*, pp. 636--641, Yokohama, Japan, January 2006.
233. T.-C. Chen, Y.-W. Chang, and C.-C. Lin, “IMF: Interconnect-driven multilevel floorplanning for large-scale building-module designs,” in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2005)*, pp. 159--164, San Jose, Nov. 2005.

234. J.-W. Fang, I.-J. Lin, P.-H. Yuh, Y.-W. Chang, and J.-H. Wang, "A routing algorithm for flip chip design," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2005)*, pp. 753--758, San Jose, Nov. 2005.
235. Y.-W. Wu, P.-H. Yuh, C.-L. Yang, and Y.-W. Chang, "Joint exploration of architectural and physical design spaces with thermal consideration," in *Proceedings of IEEE/ACM International Symposium on Low Power Electronic Design (ISLPED-05)*, August 2005.
236. C.-S. Shih, C.-L. Yang, M.-K. Ku, T.-W. Kuo, S.-Y. Chien, Y.-W. Chang, and L.-G. Chen, "Reconfigurable platform for content science research," in *Proceedings of the 11th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA'05),* pp. 481--486, August 2005.
237. T.-Y. Ho, C.-F. Chang, Y.-W. Chang, and S.-J. Chen, "Multilevel full-chip routing for the X-based architecture," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2005)*, Anaheim, CA, June 2005 **(Best paper nominee; 14 out of 735 submissions)**
238. B.-Y. Su and Y.-W. Chang, "An optimal jumper insertion algorithm for antenna effect avoidance/fixing," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2005)*, Anaheim, CA, June 2005.
239. S.-W. Tu, J.-Y. Jou, and Y.-W. Chang, "RLC coupling-aware simulation for on-chip buses and their encoding for delay reduction," in *Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS-2005)*, Kobe, Japan, May 2005.
240. S.-L. Wang and Y.-W. Chang, "Delay modelling for buffered RLC/RLY trees," in *Proceedings of The 1st IEEE-TSA VLSI Design Automation and Test Conference (VLSI-DAT-2005)*, Hsinchu, Taiwan, April 2005.
241. T.-C. Chen and Y.-W. Chang, "Modern floorplanning based on fast simulated annealing," in *Proceedings of ACM International Symposium on Physical Design (ISPD-2005)*, San Francisco, CA, April 2005.
242. T.-C. Chen, Tien-Chang Hsu, Zhe-Wei Jiang, and Y.-W. Chang, "NTUplace: a ratio partitioning based placement algorithm for large-scale mixed-size designs," in *Proceedings of ACM International Symposium on Physical Design (ISPD-2005)*, San Francisco, CA, April 2005.
243. S.-M Lee, C.-W. Lee, Y.-W. Chang, C.-C. Su, and J.-Y. Chen, "Multilevel full-chip routing with testability and yield enhancement," in *Proceedings of ACM International Workshop on System Level Interconnect Prediction (SLIP-2005)*, San Francisco, CA, April 2005.
244. T.-C. Chen and Y.-W. Chang, "Multilevel gridless routing considering optical proximity effects," in *Proceedings of ACM/IEEE Asia South Pacific Design Automation Conference (ASP-DAC-2005)*, Shanghai, China, January 2005.
245. J.-Y. Wuu, T.-C. Chen, and Y.-W. Chang, "SoC test scheduling using the B*-tree based flooprlanning technique," in *Proceedings of ACM/IEEE Asia South Pacific Design Automation Conference (ASP-DAC-2005)*, Shanghai, China, January 2005.
246. G.-M. Wu, J.-M. Lin, Y.-W. Chang, and R.-H. Chuang, "Placement with symmetry constraints for analog layout design," in *Proceedings of ACM/IEEE Asia South Pacific Design Automation Conference (ASP-DAC-2005)*, Shanghai, China, January 2005.

247. J.-M. Hsu and Y.-W. Chang, "A reusable methodology for non-slicing floorplanning," in *Proceedings of IEEE Asia and Pacific Conference on Circuits and Systems (APCCAS-2004)*, Tainan, Taiwan, December 2004.
248. P.-H. Yu, C.-L.Yang and Y.-W. Chang, "Temporal floorplanning using the T-tree formulation," in *Proceedings of IEEE/ACM International Conference on computer-Aided Design (ICCAD-2004)*, San Jose, CA, November 2004.
249. T.-Y. Ho, Y.-W. Chang, and S.-J. Chen, "Multilevel routing with jumper insertion for antenna avoidance," in *Proceedings of IEEE International SOC Conference (SOC-2004)*, Santa Clara, California, September 2004.
250. M.-C. Wu and Y.-W. Chang, "Placement with alignment and performance constraints using the B*-tree representation," in *Proceedings of IEEE International Conference on Computer Design (ICCD-2004)*, San Jose, CA, September 2004.
251. S.-W. Wu and Y.-W. Chang, "Efficient power/ground network analysis for power integrity driven design methodology," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2004)*, June 2004.
252. S.-W. Tu, J.-Y. Jou, and Y.-W. Chang, "RLC effects on worst-case switching patterns for on-chip buses," in *Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS-2004)*, Vancouver, Canada, May 2004.
253. T.-Y. Ho, Y.-W. Chang, and S.-J. Chen, "Multilevel routing with antenna avoidance," in *Proceedings of ACM International Symposium on Physical Design (ISPD-2004)*, Phoenix, Arizona, April 2004.
254. Y.-H. Cheng and Y.-W. Chang, "Integrating buffer planning with floorplanning for simultaneous multi-objective Optimization," in *Proceedings of ACM/IEEE Asia South Pacific Design Automation Conference (ASP-DAC-2004)*, Yokohama, Japan, January 2004.
255. S.-W. Tu, J.-Y. Jou, and Y.-W. Chang, "Layout techniques for on-chip interconnect inductance reduction," in *Proceedings of ACM/IEEE Asia South Pacific Design Automation Conference (ASP-DAC-2004)*, Yokohama, Japan, January 2004.
256. P.-H. Yu, C.-L.Yang, Y.-W. Chang, and H.-L. Chen, "Temporal floorplanning using 3D-subTCG," in *Proceedings of ACM/IEEE Asia South Pacific Design Automation Conference (ASP-DAC-2004)*, Yokohama, Japan, January 2004. **(Best paper nominee; 8 out of 291 submissions)**
257. T.-Y. Ho, Y.-W. Chang, S.-J. Chen, and D. T. Lee, "A fast crosstalk- and performance-driven multilevel routing system," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-2003)*, San Jose, Nov. 2003.
258. H.-C. Lee, Y.-W. Chang, J.-M. Hsu, and H. Yang, "Multilevel floorplanning/placement for large-scale modules using B*-trees," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-2003)*, Anaheim, CA, June 2003.
259. H.-R. Jiang, J.-Y. Jou, Y.-W. Chang, and K.-Y. Chao, "Simultaneous floorplanning and buffer planning," in *Proceedings of ACM Asia South Pacific Design Automation Conference* (*ASP-DAC-03*), pp. 431-434, Kitakyushu, Japan, January 2003.
260. S.-M. Li, Y.-H. Cherng, and Y.-W. Chang, "Noise-constrained buffer-block planning for

interconnect-driven floorplanning," in *Proceedings of ACM Asia South Pacific Design Automation Conference* (*ASP-DAC-03*), pp. 423-426, Kitakyushu, Japan, January 2003.

261. J.-M. Lin, S.-R. Pan, and Y.-W. Chang, "Graph matching-based algorithms for array-based FPGA segmentation design and routing," in *Proceedings of ACM/IEEE Asia South Pacific Design Automation Conference (ASP-DAC-2003)*, pp. 851--854, Kitakyushu, Japan, January. 2003.
262. S.-P. Lin and Y.-W. Chang, "A novel framework for multilevel routing considering routability and performance," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-02)*, p. 44--50, San Jose, Nov. 2002. **(Best paper nominee)**.
263. J.-M. Lin and Y.-W. Chang, "TCG-S: Orthogonal coupling of P*-admissible representations for general floorplans," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-02)*, pp. 842—847, New Orleans, LA, June 2002.
264. S.-W. Tu, W.-Z. Shen, Y.-W. Chang, and T.-C. Chen, "Inductance modeling for on-chip interconnects," in *Proceedings of IEEE International Symposium on Circuits and Systems* (*ISCAS-02*), Vol. 3, pp. 787–790, AZ, May 2002.
265. C.-Y. Chang, H.-R. Jiang, and Y.-W. Chang, "Formulae for performance optimization and their applications to interconnect-driven floorplanning," in *2002 Proceedings of IEEE International Symposium on Quality of Electronic Design (ISQED-02)*, San Jose, CA, March 2002.
266. J.-M. Lin, H.-L. Lin, and Y.-W. Chang, "Arbitrary convex and concave rectilinear module packing using TCG," in *Proceedings of ACM/IEEE Design Automation and Test in Europe (DATE-2002)*, pp. 69—75, Paris, France, March 2002.
267. G.-M. Wu and Y.-W. Chang, "An algorithm for dynamically rconfigurable FPGA placement," in *Proceedings of IEEE International Conference on Computer Design (ICCD-01)*, pp. 501--504, Austin, TX, Oct. 2001.
268. G.-M. Wu, J.-M. Lin, M. C.-T. Chao, and Y.-W. Chang, "Generic ILP-based approaches for dynamically reconfigurable FPGA partitioning," in *Proceedings of IEEE International Conference on Computer Design (ICCD-01)*, pp. 335--340, Austin, TX, Oct. 2001. **(Best paper nominee)**
269. T.-C. Chen, S.-R. Pan, and Y.-W. Chang, "Performance optimization by wire and buffer sizing under the transmission line model," in *Proceedings of IEEE International Conference on Computer Design (ICCD-01)*, pp. 192--197, Austin, TX, Oct. 2001
270. J.-M. Lin and Y.-W. Chang, "TCG: A transitive closure graph based representation for non-slicing floorplans," in *Proceedings of ACM/IEEE Design Automation Conference (DAC-01)*, pp. 764--769, Las Vegas, NV, June 2001.
271. S.-R. Pan and Y.-W. Chang, "Crosstalk-constrained performance optimization using wire sizing and perturbation," in *Proceedings of IEEE International Conference on Computer Design (ICCD-2K), pp.581-584, A*ustin, TX, Oct. 2000.
272. G.-M. Wu, Y.-C. Chang, and Y.-W. Chang, "Rectilinear block placement using B*-trees," in *Proceedings of IEEE International Conference on Computer Design (ICCD-2K), pp.351-356, A*ustin, TX, Oct. 2000.
273. Y.-C. Chang, Y.-W. Chang, G.-M. Wu, and S.-W. Wu, "B*-trees: A new representation for non-

slicing floorplans," in *Proceedings of the 37th ACM/IEEE Design Automation Conference (DAC-2K)*, pp. 458-463, LA, CA, June 2000. **(Best paper nominee)**

274. Y.-W. Chang and Y.-T. Chang, "An architecture-driven simultaneous placement and routing for FPGAs," in *Proceedings of the 37th ACM/IEEE Design Automation Conference (DAC-2K)*, pp. 567-572, LA, CA, June 2000.
275. H.-R. Jiang, S.-R., Pan, Y.-W. Chang, and J.-Y. Jou, "Optimal reliable crosstalk-driven interconnect optimization," in Proceedings of *ACM International Symposium on Physical Design (ISPD-2K)*, pp. 128-133, San Diego, CA, April 2000
276. C.-T. M. Chao, G.-M. Wu, H.-R. Jiang, and Y.-W. Chang, "A clustering- and probability-based algorithm for time-multiplexed FPGA partitioning," in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD-99)*, pp. 364-368, San Jose, CA, Nov. 1999.
277. M. Shyu, Y.-D. Chang, G.-M. Wu, and Y.-W. Chang, "Generic universal switch-block architecture and its interaction with routing," in *Proceedings of IEEE International Conference on Computer Design (ICCD-99), pp. 311-314, A*ustin, TX, Oct. 1999.
278. H.-R. Jiang, J.-Y. Jou, and Y.-W. Chang, "Noise-constrained performance optimization by simultaneous wire and gate sizing based on Lagrangian relaxation," in *Proceedings of the 36th ACM/IEEE Design Automation Conference (DAC-99)*, pp. 90-95, New Orleans, LA, June 1999.
279. G.-M. Wu, M. Shyu, and Y.-W. Chang, "Three-dimensional universal switch modules," presented at *1999 ACM Symposium on Field Programmable Gate Arrays (FPGA-99),* Monterey, CA, Feb. 1999. (This work was cited in the article "FPGA'99: Advanced processes unleash architectural ideas" in *EE Times*, February 23, 1999.)
280. Y.-W. Chang, J.-M. Lin, and D. F. Wong, "Graph-matching based algorithms for FPGA segmentation design," in *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design* (*ICCAD-98*), pp. 34-39, San Jose, CA, November 1998
281. K. Zhu, Y.-W. Chang, and D. F. Wong, "Timing-driven routing for symmetrical-array-based FPGAs," in *Proceedings of the IEEE International Conference on Computer Design (ICCD-98)*, Austin, TX, October 1998.
282. G.-M. Wu and Y.-W. Chang, "Maximally routable switch matrices for FPD design," *Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS-98)*, Monterey, CA, May 1998.
283. G.-M. Wu and Y.-W. Chang, "Switch-matrix design and routing for FPDs," *Proceedings of ACM International Symposium on Physical Design (ISPD)*, pp. 158-163, Monterey, CA, April 1998.
284. Y.-W. Chang, D. F. Wong, and C. K. Wong, "A graph-theoretic sufficient condition for FPGA/FPIC switch-module routability," *Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS)*, vol. III, pp. 1572--1575, Hong Kong, June 1997.
285. C.-P. Chen, Y.-W. Chang, and D. F. Wong, "Fast performance-driven optimization for buffered clock trees based on Lagrangian relaxation," *Proceedings of 33rd ACM/IEEE Design Automation Conference (DAC)*, pp. 405--408, Las Vegas, NV, June 1996.
286. Y.-W. Chang, D. F. Wong, K. Zhu, and C. K. Wong, "On a new timing-driven routing tree problem," *Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. IV: 420--423, Atlanta, GA, May 1996.

287. Y.-W. Chang, D. F. Wong, and C. K. Wong, "Universal switch-module design for symmetrical-array-based FPGAs," *Proceedings of ACM International Symposium on Field Programmable Gate Arrays (FPGA)*, pp. 80--86, Monterey, CA, February 1996. (Received the highest score.)
288. Y.-W. Chang, D. F. Wong, and C. K. Wong, "FPGA global routing based on a new congestion metric," *Proceedings of IEEE International Conference on Computer Design (ICCD)*, pp. 372--378, Austin, TX, Oct. 1995. **(Best Paper Award)**
289. Y.-W. Chang, D. F. Wong, and C. K. Wong, "Design and analysis of FPGA/FPIC switch modules," *Proceedings of IEEE International Conference on Computer Design (ICCD)*, pp. 394--401, Austin, TX, Oct. 1995.
290. Y.-W. Chang, S. Thakur, K. Zhu, and D. F. Wong, "A new global routing algorithm for FPGAs," *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pp. 380--385, San Jose, CA, Nov. 1994.
291. K. Zhu, D. F. Wong, and Y.-W. Chang, "Switch module design with application to two-dimensional segmentation design," *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pp. 480--485, Santa Clara, CA, Nov. 1993.

Other Conferences

1. C.-Y. Chiang, W.-H. Tseng, Y.-W. Chang, and H.-M. Chen, "Standard-Cell-Aware Learning-Guided Adaptive Weighting for Analytical Mixed-Size Placement," in *Proceedings of the 36th VLSI Design/CAD Symposium*, Tainan, Taiwan, Aug. 2026. **(Best Paper Award)**
2. Z.-Y. Cai and Y.-W. Chang, "Physics-Informed Branch-and-Cut for Analytical Concurrent Decoupling Capacitor Placement in PCB Power Distribution Networks," in *Proceedings of the 36th VLSI Design/CAD Symposium*, Tainan, Taiwan, Aug. 2026. **(Best Paper Candidate)**
3. C.-W.u Yeh, S.-H. Chen, P.-J. Lin, Y.-W. Chang, H.-Y. Lin, H.-Y. Chen, J. Chang, "High-Speed Advanced Package Substrate Routing with Plated-Through-Hole-Aware Optimization," in *Proceedings of the 36th VLSI Design/CAD Symposium*, Tainan, Taiwan, Aug. 2026.
4. S.-H. Chen, Z.-W. Chen, P.-J. Lin, H.-J. Hsu, H.-Y. Lin, Y.-H. Chuang, H.-Y. Chen, J. Chang and Y.-W. Chang, "Pre-assignment routing for performance optimization in high-speed 2.5D/3D packaging," in *Proceedings of the 35th VLSI Design/CAD Symposium*, Kaohsiung, Taiwan, Aug. 2025. **(1st-Place Best Paper Award in the EDA/Testing Category)**
5. Z.-H. Wu, B.-Y. Huang, Y.-C. Chen, and Y.-W. Chang, "Parallel longest-path-first and minimum-slack-first non-integer multiple-cell-height node remapping," in *Proceedings of the 35th VLSI Design/CAD Symposium,* Tainan, Taiwan, Aug. 2025.
6. T.-J. Lin and Y.-W. Chang, "Scalable optical-electrical codesign for on-chip signal transmissions," in *Proceedings of the 35th VLSI Design/CAD Symposium*, Kaohsiung, Taiwan, Aug. 2025.
7. S.-Y. Lo, C.-M. Chang, and Y.-W. Chang, "DeepONet-based operator learning for warpage modeling in advanced packaging," in *Proceedings of the 35th VLSI Design/CAD Symposium*, Kaohsiung, Taiwan, Aug. 2025.
8. Z.-Y. Cai, W.-H. Mao, Y.-W. Chang, Y. Lu, J. Bai, and B.-C. Tseng, "Analytical decoupling

capacitor placement based on semidefinite programming for power distribution network optimization," in *Proceedings of the 35th VLSI Design/CAD Symposium*, Kaohsiung, Taiwan, Aug. 2025.

9. C.-C. Lan, Y.-H. Lu, C.-C. Su, Y.-W. Chang, "Fast robust technology-transferable static IR drop prediction using image-to-image machine learning," in *Proceedings of the 34th VLSI Design/CAD Symposium,* Taichung, Taiwan, Aug. 2024.
10. S.-Y. Lo, M. Liu, and Y.-W. Chang, "Fast high-fidelity warpage modeling for advanced packaging analysis," in *Proceedings of the 34th VLSI Design/CAD Symposium,* Taichung, Taiwan, Aug. 2024.
11. C.-Y. Chiang, Y.-H. Chiang, C.-C. Lan, Y. Hsu, J.-M. Chang, S.-C. Huang, S.-H. Wang, Y.-W. Chang, and H.-M. Chen, "Reinforcement learning-based mixed-size placement prototyping with semi-concurrent optimization," in *Proceedings of the 34th VLSI Design/CAD Symposiu*m, Taichung, Taiwan, Aug. 2024.
12. W.-H. Tseng, Y.-W. Chang, and J.-H. Roland Jiang, "Qubit mapping for trapped-ion systems using satisfiability modulo theories," in *Proceedings of the 34th VLSI Design/CAD Symposium,* Kaohsiung, Taiwan, Aug. 2023.
13. S.-Y. Lo, M.-H. Chen, and Y.-W. Chang, "Optimizing package designs: an analytical multi-die floorplanner considering warpage effects," in *Proceedings of the 34th VLSI Design/CAD Symposium,* Kaohsiung, Taiwan, Aug. 2023.
14. Y.-L. Chen, W.-C. Tseng, W.-Y. Kao, and Y.-W. Chang, "STAR ONoCs: provably good fault-tolerant topologies for wavelength-routed optical networks-on-chip designs," in *Proceedings of the 34th VLSI Design/CAD Symposium*, Kaohsiung, Taiwan, Aug. 2023.
15. K.-C. Chen, Y.-L. Chen, Y.-S. Lu, and Y.-W. Chang, "Toward optimal topology generation and efficient radius selection for parallelism-aware wavelength-routed optical Networks-on-chip design," in *Proceedings of the 33rd VLSI Design/CAD Symposium*, Aug. 2022.
16. Y. Hsu, M.-H. Chung, and Y.-W. Chang, "TCG-based warpage-aware floorplanning for heterogeneous integration," in *Proceedings of the 33rd VLSI Design/CAD Symposium,* Aug. 2022.
17. W.-H. Tseng, C.-H. Hsu, W.-H. Lin, and Y.-W. Chang, "A compression algorithm for topological quantum error-corrected circuits based on bridging," in *Proceedings of the 32nd VLSI Design/CAD Symposium*, Aug. 2021. **(Invited Paper)**
18. Y.-S. Lu, K.-C. Chen, Y.-L. Hsu, and Y.-W. Chang, "Thermal-aware optical-electrical co-routing algorithm for networks-on-chip," in *Proceedings of the 32nd VLSI Design/CAD Symposium*, Aug. 2021. **(Best Paper Award)**
19. W.-K. Liu, M.-H. Chen, C.-M. Chang, C.-C. Chang, and Y.-W. Chang, "Time-division multiplexing based system-level FPGA routing for logic verification," in *Proceedings of 31st VLSI Design/CAD Symposium*, Taichung, Taiwan, Aug. 2020. **(Best Paper Candidate)**
20. Y.-J. Cai, Y. Hsu, and Y.-W. Chang, "Multiple RDL routing considering irregular vias," in *Proceedings of 31st VLSI Design/CAD Symposium*, Taichung, Taiwan, Aug. 2020.
21. C.-H. Chiang, F.-Y. Chuang, and Y.-W. Chang, "Toward optimal unified RDL routing algorithms for 2.5D IC packages," in *Proceedings of 29th VLSI Design/CAD Symposium,* Tainan, Taiwan, Aug. 2018. **(Best Paper Award)**
22. C.-H. Hsu, H. Chen, F.-K. Sun, C.-Y. Chen, and Y.-W. Chang, "An effective algorithm on initial

detailed routing," in *Proceedings of 29th VLSI Design/CAD Symposium*, Tainan, Taiwan, Aug. 2018.

23. B.-Q. Lin, T.-C. Lin, and Y.-W. Chang, "An effective RDL routing algorithm for the InFO WLCSP technology," in *Proceedings of 27th VLSI Design/CAD Symposium*, Kaohsiung, Taiwan, Aug. 2016. (**Best feature paper award**; originally named best paper award)
24. C.-H. Wang, Y.-Y. Wu, J. Chen, Y.-W. Chang, S.-Y. Kuo, W. Wang, and G. Fan, "Legalization for multiple-cell-height standard cells," in *Proceedings of 27th VLSI Design/CAD Symposium*, Kaohsiung, Taiwan, Aug. 2016.
25. C.-C. Huang, H.-Y. Lee, B.-Q. Lin, S.-W. Yang, C.-H. Chang, S.-T. Chen, and Y.-W. Chang, "A detailed-routability-driven analytical placer considering technology and region constraints," in *Proceedings of 26th VLSI Design/CAD Symposium*, Hau-Lien, Taiwan, Aug. 2015. **(Best Paper Award)**
26. Z.-W. Lin and Y.-W. Chang, "DSA templates guided cut redistribution for advanced 1-D gridded layouts," in *Proceedings of the 26th VLSI Design/CAD Symposium*, Hau-Lien, Taiwan, Aug. 2015.
27. S.-Y. Fang, C.-W. Lin, G.-W. Liao, and Y.-W. Chang, "Accurate closed-form modeling for simultaneous OPC- and CMP-aware routing," in *Proceedings of the 23rd VLSI Design/CAD Symposium*, Ping-Tong, Taiwan, Aug. 2012.
28. T.-H. Lin, P. Banerjee, and Y.-W. Chang, "An efficient analytical placer for FPGA designs," in *Proceedings of the 23rd VLSI Design/CAD Symposium*, Ping-Tong, Taiwan, Aug. 2012.
29. M.-K. Hau, S. chou, T.-H. Lin, and Y.-W. Chang, "A novel routability-driven analytical placement algorithm," in *Proceedings of the 22nd VLSI Design/CAD Symposium*, Yun-Lin, Taiwan, Aug. 2011. **(Best paper nominee)**
30. H.-Y. Chang, H.-R. I. Jiang, and Y.-W. Chang, "Cost-effective timing ECO optimization," in *Proceedings of the 22nd VLSI Design/CAD Symposium*, Yun-Lin, Taiwan, Aug. 2011. **(Best paper nominee)**
31. S.-Y. Fang and Y.-W. Chang, "Subfield scheduling with blocked region consideration for electron-beam photomask fabrication," in *Proceedings of the 22nd VLSI Design/CAD Symposium*, Yun-Lin, Taiwan, Aug. 2011.
32. S.-Y. Fang, T.-F. Chien, and Y.-W. Chang, "ECO timing and mask-cost optimization with Redundant wires," in *Proceedings of the 21st VLSI Design/CAD Symposium*, Kaohsiung, Taiwan, Aug. 2010. **(Best Paper Award)**
33. K.-H. Ho, X.-W. Shih, S.-H. Chuang, J.-H. Jiang, and Y.-W. Chang, "ECO timing optimization using clock rescheduling," in *Proceedings of the 21st VLSI Design/CAD Symposium*, Kaohsiung, Taiwan, Aug. 2010. **(Best paper nominee)**
34. M.-K. Hsu and Y.-W. Chang, "Unified analytical approach for mixed-size global placement," in *Proceedings of the 21st VLSI Design/CAD Symposium*, Kaohsiung, Taiwan, Aug. 2010. **(Best paper nominee)**
35. P.-W. Lee, C.-W. Lin, and Y.-W. Chang, "Fast pre-assignment flip-chip routing," in *Proceedings of the 20th VLSI Design/CAD Symposium*, Hua-Lien, Taiwan, Aug. 2009. **(Best paper nominee; best paper selection was cancelled due to Typhoon Morakot)**
36. X.-W. Shih, C.-C. Cheng, Y.-K. Ho, and Y.-W. Chang, "NTUclock: A high-quality blockage-

avoiding buffered clock-tree router for modern circuit designs," in *Proceedings of the 20th VLSI Design/CAD Symposium* Hua-Lien, Taiwan, Aug. 2009.

37. T.-F. Chien, W.-C. Chao, Chien-Mo Li, K.-Y. Liao, Y.-W. Chang, M.-T. Chang, M.-H. Tsai, and C.-M. Tseng, "SoC memory BIST design optimization," in *Proceedings of the 20th VLSI Design/CAD Symposium*, Hua-Lien, Taiwan, Aug. 2009.
38. K.-H. Ho, J.-H. Jiang, and Y.-W. Chang, "Technology remapping for ECO timing optimization," in *Proceedings of the 20th VLSI Design/CAD Symposium*, Hua-Lien, Taiwan, Aug. 2009.
39. H.-Y. Chen, S.-J. Chou, and Y.-W. Chang, "Coupling-constrained dummy fill for density gradient minimization," in *Proceedings of the 19th VLSI Design/CAD Symposium*, Ping-Tong, Taiwan, Aug. 2008. **(Best Paper Award)**
40. C.-H. Hsu, H.-Y. Chen, and Y.-W. Chang, "Fast global routing with forbidden-region rerouting," in *Proceedings of the 19th VLSI Design/CAD Symposium*, Ping-Tong, Taiwan, Aug. 2008.
41. C.-H. Hsu, H.-Y. Chen, and Y.-W. Chang, "Global routing with via/wire capacity considerations," in *Proceedings of the 19th VLSI Design/CAD Symposium*, Ping-Tong, Taiwan, Aug. 2008.
42. P.-H. Yuh, C.-L. Yang, and Y.-W. Chang, "BioRoute: A network-flow based routing algorithm for digital microfluidic biochips," in *Proceedings of the 18th VLSI Design/CAD Symposium*, Hua-Lien, Taiwan, Aug. 2007. **(Best Paper Award)**
43. T.-C. Chen, G.-W. Liao, and Y.-W. Chang, "Lithography-aware routing with predictive OPC formulae," in *Proceedings of the 18th VLSI Design/CAD Symposium*, Hua-Lien, Taiwan, Aug. 2007.
44. H.-C. Chen, Y.-L. Chuang, and Y.-W. Chang, "A high-quality transitive-closure-graph-based macro placer," in *Proceedings of the 18th VLSI Design/CAD Symposium*, Hua-Lien, Taiwan, Aug. 2007.
45. S.-J. Chou, C.-H. Hsu, J.-H. Jiang, and Y.-W. Chang, "Statistical timing-yield optimization via latch substitution," in *Proceedings of the 17th VLSI Design/CAD Symposium*, Hua-Lien, Taiwan, Aug. 2006.
46. T.-Y. Ling, I-J. Lin, and Y.-W. Chang, "A statistical circuit optimization algorithm under thermal and timing constraints," in *Proceedings of the 17th VLSI Design/CAD Symposium*, Hua-Lien, Taiwan, Aug. 2006.
47. W.-P. Lee, H.-Y. Liu, and Y.-W. Chang, "Timing-constrained voltage island assignment and floorplanning for power optimization," in *Proceedings of the 15th VLSI Design/CAD Symposium*, Hua-Lien, Taiwan, Aug. 2006.
48. T.-C. Chen, Z.-W. Jiang, T.-C. Hsu, H.-C. Chen, and Y.-W. Chang, "A novel analytical mixed-size placement algorithm considering preplaced blocks," in *Proceedings of the 17th VLSI Design/CAD Symposium*, Hua-Lien, Taiwan, Aug. 2006.
49. T.-C. Chen, P.-H. Yuh, Y.-W. Chang, F.-J. Huang, and D. Liu, "A macro placer based on a new packing representation," in *Proceedings of the 17th VLSI Design/CAD Symposium*, Hua-Lien, Taiwan, Aug. 2006.
50. K. S.-M. Li, C.-L. Lee, Y.-W. Chang, C.-C. Su, and J. E. Chen, "P1500 based interconnect delay and crosstalk fault diagnosis," in *Proceedings of the 16th VLSI Design/CAD Symposium*, Hua-Lien, Taiwan, Aug. 2005.

51. T.-C. Chen and Y.-W. Chang, "A new multilevel framework for large-scale interconnect-driven floorplanning," in *Proceedings of the 16th VLSI Design/CAD Symposium*, Hua-Lien, Taiwan, Aug. 2005.
52. C.-F. Chang, T.-Y. Ho, and Y.-W. Chang, "XRoute: a multilevel routing system for the X-based architecture," in *Proceedings of the 16th VLSI Design/CAD Symposium*, Hua-Lien, Taiwan, Aug. 2005.
53. J.-W. Fang, I.-J. Lin, and Y.-W. Chang, "An RDL router for flip-chip design," in *Proceedings of the 16th VLSI Design/CAD Symposium*, Hua-Lien, Taiwan, Aug. 2005.
54. K. S.-M. Li, C.-L. Lee, Y.-W. Chang, C.-C. Su, and J. E. Chen, "Multilevel full-chip routing with testability and yield enhancement," in *Proceedings of the 16th VLSI Design/CAD Symposium*, Hua-Lien, Taiwan, Aug. 2005.
55. T.-C. Chen and Y.-W. Chang, "Full-chip gridless routing using a novel multilevel framework," in *Proceedings of the 16th VLSI Design/CAD Symposium*, Hua-Lien, Taiwan, Aug. 2005.
56. T.-C. Chen and Y.-W. Chang, "Multilevel gridless routing," in *Proceedings of the 15th VLSI Design/CAD Symposium*, Pin-Tung, Taiwan, Aug. 2004.
57. S.-W. Tu, Y.-W. Chang, and J.-Y. Jou, "RLC circuit simulation and bus encoding for delay reduction," in *Proceedings of the 15th VLSI Design/CAD Symposium*, Pin-Tung, Taiwan, Aug. 2004.
58. T.-C. Chen and Y.-W. Chang, "Fixed-outline floorplanning using the B*-tree representation," in *Proceedings of the 15th VLSI Design/CAD Symposium*, Pin-Tung, Taiwan, Aug. 2004.
59. C.-Y. Lai, S.-K. Jeng, and Y.-W. Chang, "Surface integral inductance extraction for general interconnect structures," in *Proceedings of the 15th VLSI Design/CAD Symposium*, Hua-Lien, Pin-Tung, Taiwan, Aug. 2004.
60. Y.-W. Chang, L.-G. Chen, C.-W. Jen, and M.-C. Lan, "The VLSI circuits and systems education program in Taiwan," in *Proceedings of 2003 International Conference on Engineering Education (ICEE-2003)*, Valencia, Spain, July 2003.
61. S.-W. Tu, J.-Y. Jou, and Y.-W. Chang, "Layout techniques for minimizing on-chip interconnect inductance," in *Proceedings of the 14th VLSI Design/CAD Symposium*, Hua-Lien, Taiwan, Aug. 2003.
62. M.-C. Wu and Y.-W. Chang, "Placement with an optimal evaluation scheme for alignment and performance constraints using B*-trees," in *Proceedings of the 14th VLSI Design/CAD Symposium*, Hua-Lien, Taiwan, Aug. 2003.
63. T.-Y. Ho, Y.-W. Chang, and S.-J. Chen, "A fast crosstalk-driven multilevel routing system," in *Proceedings of the 14th VLSI Design/CAD Symposium*, Hua-Lien, Taiwan, Aug. 2003.
64. S.-L. Wang and Y.-W. Chang, "Accurate delay formulae for buffered RLC trees," in *Proceedings of the 14th VLSI Design/CAD Symposium*, Hua-Lien, Taiwan, Aug. 2003.
65. Y.-H. Cheng, Y.-W. Chang and R.-H. Chuang, "Integrating buffer planning with floorplanning for simultaneous area, timing, noise, and congestion optimization," in *Proceedings of the 13th VLSI Design/CAD Symposium*, Taitung, Taiwan, Aug. 2002. **(Received the highest score out of 182 papers; score = 4.0 based on 4.0.)**
66. S-P. Lin and Y.-W. Chang, "A performance-driven multilevel router," in *Proceedings of the 13th*

VLSI Design/CAD Symposium, Taitung, Taiwan, Aug. 2002.**)**

67. H.-E. Yi, Y.-W. Chang, and M.-T. Wu, "A B*-tree based placer for boundary modules," in *Proceedings of the 13th VLSI Design/CAD Symposium*, Taitung, Taiwan, Aug. 2002.
68. S.-M. Lee, Y.-H. Cherng, and Y.-W. Chang, "Noise-aware buffer planning for interconnect-driven floorplanning," in *Proceedings of the 12th VLSI Design/CAD Symposium*, Hsinchu, Taiwan, Aug. 2001.
69. J.-M. Lin, S.-P. Lin, and Y.-W. Chang, "A P-admissible non-slicing floorplan representation with a worst-case linear-time packing scheme," in *Proceedings of the 12th VLSI Design/CAD Symposium*, Hsinchu, Taiwan, Aug. 2001. **(Received the highest score out of 152 papers; score = 4.66 based on 5.0)**
70. S.-C. Lee, J.-M. Hsu, and Y.-W. Chang, "Multilevel large-scale module placement/floorplanning using B*-trees," in *Proceedings of the 12th VLSI Design/CAD Symposium*, Hsinchu, Taiwan, Aug. 2001.
71. S.-W. Tu, W.-Z. Shen, Y.-W. Chang, and T.-C. Chen, "Inductance modeling for on-chip interconnects," in *Proceedings of the 12th VLSI Design/CAD Symposium*, Hsinchu, Taiwan, Aug. 2001.
72. G.-M. Wu, J.-M. Lin, M. C.-T. Chao, and Y.-W. Chang, "Generic ILP-based approaches for time-multiplexed FPGA partitioning," in *Proceedings of the 11th VLSI Design/CAD Symposium*, Pingdong, Taiwan, Aug. 2000.
73. G.-M. Wu and Y.-W. Chang, "Precedence-constrained placement for dynamically reconfigurable FPGAs," in *Proceedings of the 11th VLSI Design/CAD Symposium*, Pingdong, Taiwan, Aug. 2000.
74. S.-R. Pan and Y.-W. Chang, "Performance optimization by wire/buffer sizing under the transmission line model," in *Proceedings of the 11th VLSI Design/CAD Symposium*, Pingdong, Taiwan, Aug. 2000.
75. C.-Y. Chang, Y.-W. Chang, and I. H.-R. Jiang, "Simultaneous buffer-insertion/-sizing and wire-sizing formulae with applications to interconnect-driven floorplanning," in *Proceedings of the 11th VLSI Design/CAD Symposium*, Pingdong, Taiwan, Aug. 2000 **(Best Paper Award---the only year (during 1996—2002) to give such an award; two out of 125 papers were selected).**
76. J.-M. Lin, S.-R. Pan, and Y.-W. Chang, "A timing-driven matching-based algorithm for array-based FPGA routing," in *Proceedings of the 10th VLSI Design/CAD Symposium*, Nangtou, Taiwan, Aug. 1999.
77. H.-R. Jiang, S.-R. Pan, Y.-W. Chang, and J.-Y. Jou, "Reliable crosstalk-driven interconnect optimization in the deep submicron technology," in *Proceedings of the 10th VLSI Design/CAD Symposium*, Nangtou, Taiwan, Aug. 1999. **(Received the highest score in the CAD track; score = 3.67 based on 4.0.)**
78. Y.-W. Chang and J.-M. Lin, "Channel segmentation for FPGA design," in *Proceedings of the 9th VLSI Design/CAD Symposium*, pp. 335—338, Nantou, Taiwan, August 1998.
79. Y.-D. Chang, Y.-W. Chang, and M. Shyu, "Design and analysis of universal switch modules for hierarchical FPGAs," in *Proceedings of the 9th VLSI Design/CAD Symposium*, pp. 339-342 Nantou, Taiwan.
80. Y.-D. Chang, G.-M. Wu, and Y.-W. Chang, "Can FPD switch matrices be universal?," in

Proceedings of the 8th VLSI Design/CAD Symposium, Nantou, Taiwan, August 1997.

F. **Patents**

- **US Patents (20)**

1. M.-H. Chung, J.-W. Chuang, Y.-W. Chang, Y.-T. Hsieh, *Method for routing of redistribution layers in IC package,* US Patent App., US18/104,952, US20240265186A1, Feb. 2026 (granted; with AnaGlobe)
2. J. Jung, G.-J. Nam, J. Kazda, G. Enrique T., C.-C. Huang, Y.-W. Chang, *Timing-aware simultaneous optimization of latch clustering and placement in an integrated circuit*, US Patent 12,493,730, December 2025 (granted; with the IBM T. J. Watson Research Center)
3. Y. Hsu, M.-H. Chung, Y.-W. Chang, and Y.-T. Hsieh, *Method of warpage-aware floorplanning for heterogeneous integration structure*, US Patent 12,346,646, July 2025 (with AnaGlobe)
4. K.-C. Chen, Y.-L. Chen, Y.-S. Lu, Y.-W. Chang, and Y.-T. Hsieh, *Method for parallelism-aware wavelength-routed optical networks-on-chip design*, US Patent 12,190,033, July 2025 (with AnaGlobe)
5. Y.-S. Lu, S.-L. Liu, Y.-W. Chang, C.-C. Lin, C.-Y. Yang, *Method of wavelength-division-multiplexing-aware clustering for on-chip optical routing*, US Patent 11,177,901, November 2021 (with AnaGlobe)
6. C.-H. Wang, Y.-Y. Wu, S.-C. Chen, Y.-W. Chang, M.-K. Hsu, *Method for legalizing mixed-cell height standard cells of IC,* US Patent 10,713,410, July 14, 2020 (with TSMC)
7. C.-H. Chiang, F.-Y. Chuang, Y.-W. Chang, C.-C. Lin, C.-Y. Yang, *Method of redistribution layer routing for 2.5-dimensional integrated circuit packages*, US Patent 10,558,779, Feb. 2020 (with AnaGlobe)
8. C.-H. Wang, Y.-Y. Wu, S.-C. Chen, Y.-W. Chang, M.-K. Hsu, *Method for legalizing mixed-cell height standard cells of IC*, US Patent 10,275,559, Apr. 30, 2019 (with TSMC; **won an excellent patent award from TSMC**)
9. Y.-W. Chang and K.-H. Tseng, *Systems and methods for minimum-implant-area aware detailed placement*, US Patent 9,940,424, Apr. 2018 (with TSMC)
10. B.-Q. Lin, T.-C. Lin, C.-Y. Yang, Y.-W. Chang, and Y.-C. Hsieh, *Redistribution layer routing for integrated fan-out wafer-level chip-scale packages*, US Patent 9,928,334, Mar. 2018 (with AnaGlobe)
11. I.-P. Wu, H.-C. Ou, Y.-W. Chang, and Y.-C. Hsieh, *Method for analog circuit placement,* US Patent 9,830,416, Nov. 2017 (AnaGlobe)
12. C.-F. Chang, C.-F. Shen, H.-S. Chiu, I-J. Lin, T.-C. Hsu, Y.-W. Chang, C.-W. Lin, and P.-W. Lee, *Routing method for flip chip package and the computerized apparatus using the same*, US Patent 8,875,083, Oct. 2014 (Synopsys)
13. H.-Y. Chang, H.-R. Jiang, and Y.-W. Chang, *Method of implementing timing engineering change order*, US Patent 8,776,000, July 2014 (jointly won by NTU and NCTU)
14. V. Balabanov, H.-K. Hsu, and Y.-W. Chang, *Method of analytical placement with weighted-average wirelength model*, US Patent 8,689,164, April 2014 (NTU) (Google citations: 272)
15. T.-C. Chen, P.-H. Yu, Y.-W. Chang, F.-J. Lin, and T.-Y. Liu, *Method of packing-based macro*

placement and semiconductor chip using the same, US Patent: 8,661,388 (**Japan, European Union, and China patents granted**), February 2014 (MediaTek)

16. C.-F. Chang, C.-F. Shen, H.-S. Chiu, I-J. Lin, T.-C. Hsu, Y.-W. Chang, C.-W. Lin, and P.-W. Lee, *Routing method for flip chip package and apparatus using the same*, US Patent 8,578,317, Nov. 2013 (Synopsys)
17. X.-W. Shih and Y.-W. Chang, *Clock-tree structure and method for synthesizing the same*, US Patent 8,572,542, Oct. 2013 (NTU)
18. M.-K. Hsu, Y.-W. Chang, T.-C. Chen, *Hierarchy-based analytical placement method capable of macro rotation within an integrated circuit*, US Patent 8,261,223, Sep. 2012 (SpringSoft/Synopsys)
19. S.-C. Lin, T.-C. Chen, Y.-W. Chang, F.-Y. Chang, *V-Shaped multilevel full-chip gridless routing*, US Patent 7,707,536, Apr. 2010 (SpringSoft/Synopsys)
20. S.-C. Lin, T.-C. Chen, and Y.-W. Chang, *Multilevel IC floorplanner*, US Patent 7,603,640, Oct. 2009 (SpringSoft/Synopsys)
21. Y.-L. Chen, W.-C. Tseng, W.-Y. Kao, Y.-W. Chang, and Y.-T. Hsieh, Method for generating a customized WRONoC topology, US Patent App. 18/171,955, August 2024 (pending)
22. P.-W. Huang, H.-W. Chang, Y.-W. Chang, Machine-learning-based power/ground (p/g) via removal, US Patent App. 17/841,400, December 2022 (pending)

- **Taiwan/R.O.C. Patents (7)**

1. Chen-Feng Chang, Chin-Fang Shen, Hsien-Shih Chiu, I-Jye Lin, Tien-Chang Hsu, Yao-Wen Chang, Chun-Wei Lin, and Po-Wei Lee (張宸峰, 沈勤芳, 邱顯仕, 林依潔, 許天彰, 張耀文, 林忠緯, 李柏緯), *Method for analyzing single layer routing tracks and the computerized apparatus using the same (應用於單層繞線軌跡之分析方法及其電腦化裝置),* 中華民國專利, Application Number: 201122881, TW201122881A, March 2016 (SpringSoft/Synopsys)
2. Chen-Feng Chang, Chin-Fang Shen, Hsien-Shih Chiu, I-Jye Lin, Tien-Chang Hsu, Yao-Wen Chang, Chun-Wei Lin, and Po-Wei Lee (張宸峰, 沈勤芳, 邱顯仕, 林依潔, 許天彰, 張耀文, 林忠緯, 李柏緯), *Routing method for flip chip package and the computerized apparatus using the same (覆晶封裝之繞線方法及其電腦化裝置),* 中華民國專利, Application Number: 201122876, TW201122875A, January 2015 (SpringSoft/Synopsys)
3. Hua-Yu Chang, Hui-Ru Jiang, and Yao-Wen Chang (張華宇, 江蕙如, 張耀文), *時序設計變更的方法 (Method of implementing timing engineering change order),* 中華民國專利, Application Number: 101128031, TW201346608A, November 1, 2014
4. 施信瑋, 張耀文, *時鐘樹結構及其合成方法*, 中華民國專利, I435437, TWI435437B, April 21, 2014
5. 包偉力, 徐孟楷, 張耀文, *以加權平均線長模型實現之解析配置演算法*, 中華民國專利, I430127, TWI430127B, March 11, 2014 (Google Citations: 196)
6. 張耀文 and 陳皇宇, *應用於雙圖案微影技術的佈局分解方法* (*Method for resolving layout and configured for use with dual-pattern lithography)*, 中華民國專利, I 397828, TWI397828B , June 1, 2013
7. Tung-Chieh Chen, Ping-Hung Yu, Yao-Wen Chang, Fwu-Juh Huang, Tien-Yueh Liu (陳東傑,

喻秉鴻, 張耀文, 黃福助, and 劉典岳), *半導體晶片、巨集擺置的方法、多向密集堆積巨集擺置器與多尺寸混合擺置設計方法*, 中華民國專利, I390707, TWI390707B, March 21, 2013 (MediaTek)

8. Yao-Wen Chang and Chin-Hsiung Hsu (張耀文, 許欽雄), *Method for concurrent migration and decomposition of integrated circuit layout*, TW201102848A, January 16, 2011